

A single 3.3 V 2.4–2.5 GHz high linearity PHEMT MMIC power amplifier using an Mesa-etched layer as the self-biased resistor

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A mesa-etched layer at the source port, which serves as a resistor for self-biasing, is incorporated to simplify the fabrication processes and to provide a single bias in a PHEMT MMIC. The mesa-etched layer is also implemented in a two-stage 2.4GHz–2.5GHz, 3.3V, 23.5dBm self-biased AlGaAs/InGaAs/GaAs PHEMT MMIC as high gain and high linearity power amplifiers for wireless local-area network applications.

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1. Introduction

The AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistors (PHEMTs) have the advantages of possessing high power densities with high gains, which are ideal for microwave and optoelectronic applications requiring high efficiency, high power, broadband, and small dimensions. Depletion-mode PHEMTs (D-PHEMTs) are widely used in high frequency monolithic microwave integrated circuits (MMIC) amplifiers. However, it requires not only a positive voltage but also a negative voltage for gate biases, which is not convenient for system application due to the need of an additional DC-to-DC converter. Therefore, a single-bias MMIC power amplifier is more attractive for implementations. The enhancement-mode PHEMTs (E-PHEMTs) can easily serve as single-power-supply power amplifiers. However, gate fabrication processes are very crucial to well-functioned E-PHEMTs. With the advantages of less process dependence, D-PHEMTs are still very promising for single bias system applications [1]–[6]. To achieve the goal of a single-bias, the self-bias configuration is employed by adding a bypass capacitor and a resistor to the source port [7]–[8]. Thin film resistors are most commonly used for this purpose. However, additional processes are required and make the processes even more complicated.

In this work, an alternative for self-bias resistors is proposed by etching the epilayer of the source port. By trimming the resistors to have the required bias currents results in the following advantages: 1) an accurate pinch-off voltage is not necessary, 2) the process is simplified. Moreover, the related circuit can further be simplified to reduce fabrication cost. To verify the potential of the mesa-etched layer as the self-bias resistor in

MMIC applications, the implementation in a 3.3 V single voltage self-biased two-stage MMIC power amplifier using AlGaAs/InGaAs/GaAs D-PHEMTs for ISM band applications will be demonstrated.

2. PHEMT process

MMIC power amplifiers were fabricated on AlGaAs/InGaAs/GaAs PHEMT structure using the conventional photolithography technique. The PHEMT structure, as shown in Fig. 1, was grown on a 4-inch GaAs(100) semi-insulating substrate by molecular beam epitaxy including an undoped $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ channel layer sandwiched between an undoped $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ spacer and an n-type Si-doped ($3 \times 10^{18} \text{ cm}^{-3}$) $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ donor layer, and a cap layer of $\text{n}^+\text{-GaAs}$ on the top of the donor layer. The mobility is $4000 \text{ cm}^2/\text{V}\cdot\text{s}$ at room temperature, corresponding to the two-dimensional electron gas of $2.7 \times 10^{12} \text{ cm}^{-2}$. At the front-side process, the active region was isolated first by a mesa etching solution which is an $\text{HF}/\text{H}_2\text{O}_2$ solution diluted in DI water. Then, the AuGe/Ni/Au for ohmic contact was deposited and alloyed at 405°C for 30 s. The Ti/Pt/Au was deposited for the Schottky gate by a lift-off process after double recess etching. Finally, silicon nitride was deposited by PECVD as a passivated film.

A typical I-V curve for a $0.4 \mu\text{m} \times 3.6 \text{ mm}$ PHEMT is shown in Fig. 2. Typical dc characteristics of the saturated drain current, transconductance, breakdown voltage and pinch-off voltage are 280 mA/mm, 250 mS/mm, 15 V and -1.6V, respectively. The typical cutoff frequency is 30GHz and the maximum oscillation frequency is about 60GHz.

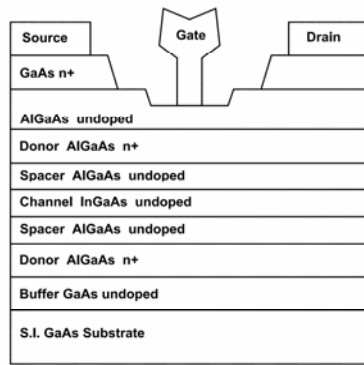


Fig. 1. PHEMT structure for MMIC application.

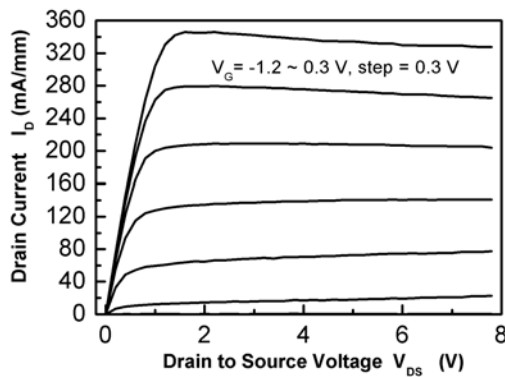
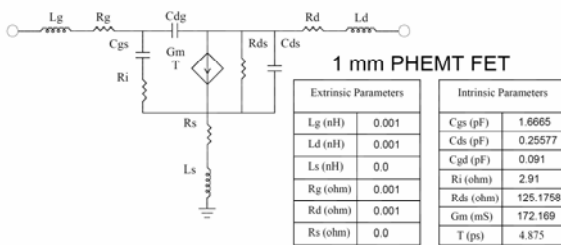
Fig. 2. Typical I-V characteristics for a $0.4 \mu\text{m} \times 3.6 \text{ mm}$ PHEMT.

Fig. 3. Small signal model of 1 mm PHEMTs.

3. Circuit design

The device model was de-embedded from the two-port S-parameters of the 1 mm PHEMT measured by a HP8510C vector network analyzer. The extraction of the parasitic parameters was done by cold-FET method and the intrinsic parameters by hot-FET method [9]-[10]. The small signal model for the 1 mm PHEMT is shown in Fig. 2. After optimizing these extracted parameters, the simulated S-parameters from the equivalent model were fitted into the measured data. The models for 1 mm and 3.6 mm PHEMT were scaled up from the 1 mm PHEMT model for circuit simulation and optimization [11].

Fig. 4 shows the circuit diagram and the corresponding

photograph of the fabricated MMIC for a complete amplifier, including the first driver stage and the second power stage. To meet the requirement of a single-power supply, a resistor is embedded into the source port for self-biasing. The first matching network of the power amplifier is designed to transfer the maximum output power from the FET to the 50Ω system. According to the Cripps method, the required optimum large-signal load impedance, $Z_{opt,Q2}$, is composed of $R_{opt,Q2}$ and $C_{ds,Q2}$. The $R_{opt,Q2}$ is calculated from the biased voltage V_{ds} and the current I_{ds} , which are determined to be half of the maximum channel current for class A operation. The parameter $C_{ds,Q2}$ is obtained from the small-signal model. The calculated $R_{opt,Q1}$ and $R_{opt,Q2}$ are 3.9Ω and 2Ω , respectively. The corresponding $C_{opt,Q1}$ and $C_{opt,Q2}$ are 0.2558 pF and 0.9208 pF . The output power matching network was designed to transfer the $Z_{opt,Q2}$ to 50Ω . The output matching network comprises a shunt inductance series with a bypass capacitor that provides a DC path, a low-pass L-section transformer and a series block capacitor. The inter-stage matching network was designed to reduce the mismatch loss. The power matching for the $R_{opt,Q1}$ and $C_{ds,Q1}$ that maximizes the output power is also considered. Lossy matching is implemented in the gate resistor in each stage to improve the stability. Then the circuit stability is further confirmed by the simulation of K and Δ factor.

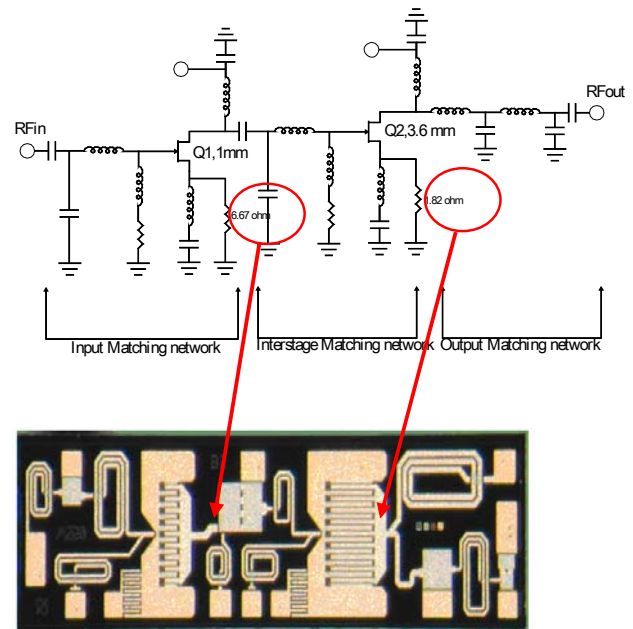


Fig. 4. Circuit diagram and photograph of the fabricated self-biased PHEMT MMIC power amplifier.

Finally, the input network was designed to smooth the small signal gain and to improve impedance match for a better input return loss. Then, the width of the micro-strip line was simply defined by the design rule and the current-density limitation. Based on these essential matching networks, an optimization and EM simulation were performed to achieve the required circuit performance

and the minimized chip dimension.

4. MMIC fabrication

The fabrication of this self-biased MMIC process is similar to that of the PHEMT process as described previously. The gate length is $0.4 \mu\text{m}$ long and the gate width are 1 mm and 3.6 mm for Q_1 and Q_2 , respectively. After the PHEMTs fabrication, mesa-etching epilayers for self-bias source resistors as indicated in the Fig. 4 were processed. Based on the required bias current, the gate bias voltage, V_G , of the PHEMT is determined to obtain the estimated source resistance (R_s). The source self-bias resistance has been designed to fit the required self-bias current using the sheet resistance of $400 \Omega/\square$. However, the real sheet resistance of a wafer ranges from 200 to $220 \Omega/\square$. The resistance trimming process is used to adjust the desired self-bias current by monitoring the current directly. The resistance trimmed by an $\text{HF:H}_2\text{O}_2:\text{H}_2\text{O}$ etching solution will compensate the non-accurate pinch-off voltage during processing to achieve the required bias current. Finally, devices were passivated by Si_3N_4 prepared by PECVD for measurement. For Q_2 , the bias current is $I_{D2}=220 \text{ mA}$. The corresponding V_G is around 0.4 V for a 3.6 mm PHEMT. The estimated R_{S2} is equal to 1.82Ω . Similarly, R_{S1} is equal to 6.67Ω . In the layout, a small area near the source region is reserved for R_s . There are eight mesa regions in parallel with each dimension of $30 \mu\text{m} \times 4 \mu\text{m}$ for Q_1 stage and also eleven mesa regions in parallel with each dimension of $80 \mu\text{m} \times 4 \mu\text{m}$ for Q_2 stage.

This approach can effectively eliminate the use of the masks required to fabricate thin film resistors. The chip area of the fabricated MMIC shown in Fig. 4 is as small as $2.5 \times 0.68 \text{ mm}^2$. A bonding wire is used to make the ground connection; the inductance of the wire is 0.25 nH at the output port. The fabricated MMIC has the following characteristics: 1). A mesa-etched layer is fabricated at the source port, rather than a thin film resistor, to serve as the resistor for single voltage self-bias configuration and to simplify the fabrication processes. 2). A bonding wire, instead of a via-hole, is used for grounding and for source capacitance on the chip. The inductance of the bonding wire is estimated about 0.15 nH at the source port. Moreover, it works well with an automatic surface mounting technology (SMT) machine and eliminates the alignment problem of the via-hole on the power device. 3). The chip dimensions can be reduced as well as fabrication costs. 4). The device reliability can also be enhanced.

5. Results and discussion

The bias conditions for the MMIC are $V_d=3.3 \text{ V}$ and $I_{ds}=280 \text{ mA}$, including 60 mA for the driver stage and 220 mA for the power stage. Fig. 5 shows the measured small signal gain and input/output return loss of the MMIC from 2.35 to 2.55 GHz . The small signal gain is 30.4 dB at 2.45 GHz . The input/output return loss is better than $15 \text{ dB}/5 \text{ dB}$ from 2.4 to 2.5 GHz , respectively.

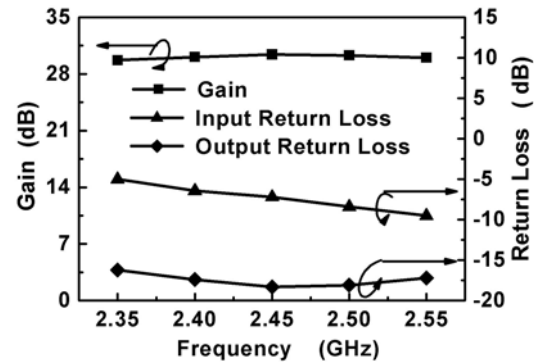


Fig. 5. Small signal gain, input and output return loss versus frequency.

The output power and power added efficiency (PAE) as a function of frequency is shown in Fig. 6. From 2.4 to 2.5 GHz , 1-dB gain compression power, $P_{1\text{dB}}$, is more than 23 dBm and PAE is more than 23.5% , respectively. The output power, gain and PAE as a function of input power for the MMIC measured at 2.45 GHz are shown in Fig. 7. It is shown that $P_{1\text{dB}}$ is 23.5 dBm with PAE of 24.2% , while the associated gain is 29.4 dB . The saturated output power is 23.8 dBm .

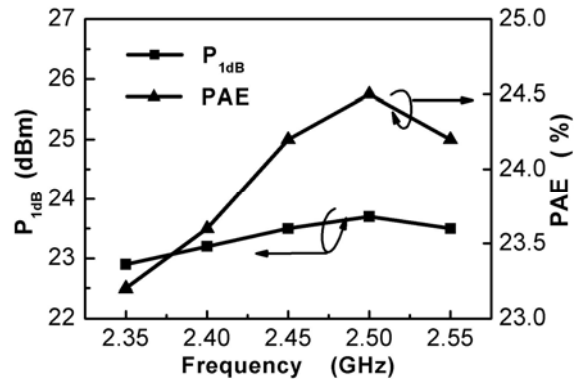


Fig. 6. Output power versus frequency at 25°C .

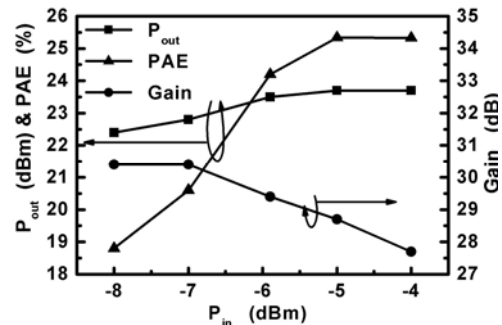


Fig. 7. Output power and PAE as functions of input power at 2.45 GHz .

The two-tone inter-modulation powers, as shown in Fig. 8, were measured at a frequency of 2.45 GHz and a 3 dB back-off point with a carrier interval of 5 MHz . The

3rd order inter-modulation distortion is 49.2 dBc, corresponding to an OIP3 of 37.6 dBm with the single carrier output power level of 13 dBm, which meets the need for high linearity with the specifications of 30 dB high gain, a 1-dB compression gain output power of 23.5 dBm and 37.2 dBm high linearity.

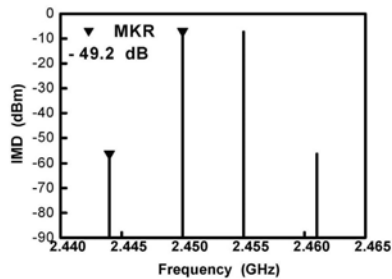


Fig. 8. 37.6dBc of 3rd order IMD @ $P_{out} = 13$ dBm for the output stage power amplifier.

The temperature-dependence of the MMIC performance, ranging from -45°C and $+65^{\circ}\text{C}$, is also investigated, as shown in Fig. 9. At 65°C , the corresponding gain, P_{1dB} , PAE and the current at 2.45 GHz are 29.4 dB, 23.2 dBm, 23.4 % and 271 mA, respectively. At -45°C , the corresponding values at 2.45 GHz are 31.6 dB, 24.1 dBm, 26.5% and 297 mA. The signal gain variation over temperature from -45°C to 65°C is as small as $0.02\text{dB}/^{\circ}\text{C}$, which is better than the reported high power amplifiers without self-bias resistors. This is partially due to the negative feedback of the self-bias resistor. These results reveal that the fabricated MMIC with the mesa-etched resistor for single-voltage self-bias can be stably operated in a wide temperature range.

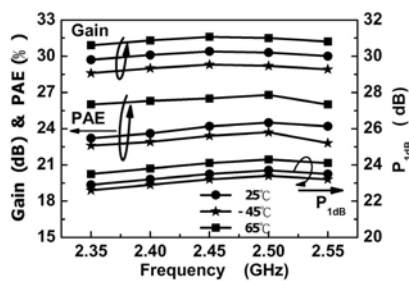


Fig. 9. Small signal gain, PAE and 1-dB gain compression power at different temperatures stage power amplifier.

6. Conclusions

The implementation of an etched Mesa layer is demonstrated to serve as the self-bias resistor for a single voltage circuit configuration instead of the thin film resistor and to simplify the PHEMT amplifier fabrication processes. Moreover, the integration of the etched mesa epilayer into a 2.4 GHz – 2.5 GHz self-biased PHEMT two-stage MMIC

power amplifier operated by a single 3.3 V drain voltage is also presented. The demonstrated MMIC with a P_{1dB} of 23.5 dBm, power-added efficiency of 24.2 %, a small-signal gain of 30.4 dB, an input/output return loss better than 15 dB/5dB and a third-order intercept point better than 37.6 dBm can be achieved. In addition, it is also more stable in temperature-dependent properties as compared to the power amplifiers without using self-bias resistors. The proposed method can be applied to the power device fabrication.

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