A comparative study of the dielectric properties of Al/p-Si structures with 50 and 826 Å SiO_2 interfacial layer

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Dielectric properties and ac electrical conductivity (σ_{ac}) of Al/p-Si structures with 50 Å (MIS) and 826 Å (MOS) interfacial insulator layer (SiO_2) have been investigated in the frequency range of 10 kHz-2 MHz using the capacitance–voltage (*C–V*) and conductance–voltage (*G/ω–V*) measurements at room temperature. SiO_2 layer was grown on p-Si by thermal oxidation method. Experimental results show that the dielectric constant (ε'), dielectric loss (ε''), loss tangent (tanδ), ac electrical conductivity (σ_{ac}) and the real and imaginary parts of electric modulus (M' and M'') are strong functions of frequency in depletion region. Accordingly, it has been found that as the frequency increases, ε' values decrease while an increase is observed in σ_{ac} and the electric modulus for two samples. On the other hand, the values of ε'' and tanδ decrease with the increasing frequency for MIS and MOS structures at low frequencies while, at high frequencies, the values of ε'' and tanδ increase with the increasing frequency for two structures. As a result, the interfacial polarization can more easily occur at low frequencies and/or the number of interface states (N_{ss}) localized at SiO_2/Si interface, consequently contributed to the improvement of dielectric properties and ac electrical conductivity of these structures.

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1. Introduction

Silicon is still dominating material in the semiconductor technology because of the excellent properties of its oxide and the silicon-silicon dioxide (Si/SiO_2) interface. Used in semiconductor technology, Si is a source amply found in nature; moreover, one another important characteristic of Si is that it allows the formation of an insulator layer (SiO_2) on the crystal surface. The preparation of clean Si surfaces and growth of the insulator or oxide on this surface to device fabrication are more important. Metal-semiconductor (MS), metal-oxide-semiconductor (MOS) and metal-insulator-semiconductor (MIS) structures occupy a very significant position in today's technology. MIS or MOS type structures can be produced by coating either artificially or naturally an oxide layer upon the metal/semiconductor interface [1-5]. The most important characteristics of the oxide layer coated between the metal and the semiconductor are its resistance to low electrical resistivity, high optic permeability, high dielectric coefficient and environmental conditions. With regard to the dielectric property of the coated oxide layer, MOS and MIS structures are analogous to parallel-plate capacitors. In the studies conducted so far, between the metal and the semiconductor, oxide layers of various types have been coated, the most important of which are SiO_2 and SnO_2 [4,6]. The formation of an insulator layer on Si by traditional ways of oxidation or deposition cannot completely passivate the active dangling bonds at the Si surface. The study of dielectric properties produces valuable information on the behavior of localized electric charge carriers leading to greater understanding of the mechanism of dielectric polarization in the studied such as MOS and MIS structures. Nevertheless satisfactory understanding in all details has still not been achieved. At high frequencies ω (such that the carrier life time τ is much larger than 1/ω) the charges at the interface states cannot follow an ac signal. On the contrary, at low frequencies the charges can easily follow an ac signal and the capability of following the ac signal increases with the decreasing frequency. Therefore, the frequency dependent electrical and dielectric characteristics of these devices with different thickness interfacial insulator layer are very important considering the accuracy and reliability results [7-13].

In this article, dielectric properties of Al/p-Si structures with 50 Å SiO_2 interfacial layer (MIS) and 826 Å SiO_2 interfacial insulator layer (MOS) were compared. Dielectric properties of Al/SiO_2/p-Si MIS and MOS structures have been studied by C-V and G/ω-V measurements technique in the frequency range of 10 kHz-2 MHz at room temperature. To determine the dielectric constant (ε'), dielectric loss (ε''), loss tangent (tanδ), the ac electrical conductivity (σ_{ac}) and the electric modulus (M' and M'') of these structures, the admittance technique was used [12,13].

2. Experimental procedure

The Al/SiO_2/p-Si structures were fabricated using p-type (boron-doped) single crystal silicon wafer with <100> surface orientation, having thickness of 350 μm, 2" diameter and 1 Ω.cm resistivity. For the fabrication process, Si wafers were degreased in organic solutions of CHCl CCl_2, CH_3COCH_3 and CH_3OH, then etched in a sequence of H_2SO_4 and H_2O_2, 20% HF, a solution of $6HNO_3$: 1HF: $35H_2O$, 20% HF and finally quenched in de-ionized water with resistivity of 18 MΩ-cm for 10 minutes. The oxidation procedure was carried in a resistance heated furnace in dry oxygen with a flow rate of 1.5 lt/min. The oxide layers thickness values of 50 Å and 826 Å were grown at the temperatures of 750 ^oC for 1.5 hours and 900 ^oC for 4 hours, respectively. These oxide thicknesses were determined from the measurements of the capacitances in the strong accumulation regan. Following oxidation, circular dots of 1.2 mm diameter high purity (99.999 %) Al with a thickness of ~2000 Å were deposited in order to form the rectifier contacts on the oxidized surface of the wafer through a Cu shadow mask in a liquid nitrogen trapped vacuum system with ~ $2x10^{-6}$ Torr vacuum pressure. Finally, Al with a thickness of ~2000 Å is also thermally evaporated on the whole back surface of the wafer after etching away the oxide layer (SiO_2) from the back surface in HF in order to form ohmic/back contacts. The thickness of metal layers and the deposition rates were monitored with the help of quartz crystal thickness monitor. In order to C-V and G/ω-V measurements, the electrical contacts are made on to the upper electrode on the oxide with the help of fine phosphor-bronze spring probe. The measurements were carried out at room temperature in electrically shielded metal box.

The *C-V* and *G/ω-V* measurements have been performed using a computerized HP 4192A LF impedance analyzer (5 Hz-13 MHz). The capacitance and conductance values as a uction of the applied bias voltage have been measured at room temperature in the frequency range of 10 kHz -2 MHz, where small sinusoidal signal of 40 mV peak to peak from the external pulse generator is applied to the sample in order to meet the requirement [3]. All measurements were carried out with the help of a microcomputer through an IEEE-488 AC/DC converter card.

3. Results and discussions

The frequency dependence of dielectric constant (ε'), dielectric loss (ε"), loss tangent (tanδ), ac electrical conductivity (σ_{ac}), the resistivity (ρ_{ac}) and the real and imaginary parts of electric modulus (M' and M") of Al/p-Si structures with 50 Å (MIS) and 826 Å (MOS) interfacial insulator layer (SiO_2)have been investigated in the frequency range of 10 kHz-2 MHz . The complex permittivity of dielectric can be defined in the following complex form [14,15],

$$\varepsilon^* = \varepsilon' - j\varepsilon'' \tag{1}$$

where ε' and ε" are the real and the imaginary parts of complex permittivity, and j is the imaginary root of -1. The complex permittivity formalism has been employed to describe the electrical and dielectric properties. In the ε* formalism, in the case of admittance measurements which consists of C and G/w, the following relation holds:

$$\varepsilon^* = \frac{Y^*}{j\omega C_o} = \frac{C}{C_o} - j\frac{G}{\omega C_o} \tag{2}$$

where Y^* is the measured admittance, C and G its real and imaginary parts, and ω is the angular frequency ($\omega=2\pi f$) of the applied electric field [16]. The real part of the complex permittivity, the dielectric constant (ε'), at the various frequencies is calculated using the measured capacitance values in the strong accumulation region from the relation [17,18],

$$\varepsilon' = \frac{d}{\varepsilon_o A}C = \frac{C}{C_o} \tag{3}$$

where C_o is capacitance of an empty capacitor, $C_o = \varepsilon_o(A/d)$, where A is the rectifier contact area in cm^2, d is the interfacial insulator layer thickness and ε_o is the permittivity of free space charge (ε_o = $8.85x10^{-14}$ F/cm). In the strong accumulation region, the maximal capacitance of MIS Schottky diode corresponds to the insulator capacitance (C_{ox}) ($C_{ac} = C_{ox} = \varepsilon'\varepsilon_o A/d$). The imaginary part of the complex permittivity, the dielectric loss (ε"), at the various frequencies is calculated using the measured conductance values from the relation,

$$\varepsilon'' = \frac{d}{\varepsilon_o A\omega}G = \frac{G}{\omega C_o} \tag{4}$$

The loss tangent (tanδ) can be expressed as follows [15-18],

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} \tag{5}$$

The AC electrical conductivity (σ_{ac}) of the dielectric material can be given by the following equation [14,19,20],

$$\sigma_{ac} = \omega C \tan\delta(d/A) = \varepsilon''\omega\varepsilon_o \tag{6}$$

The complex impedance (Z^*) and complex electric modulus (M^*) formalisms were discussed by various authors with regard to the analysis of dielectric materials [17,19]. Analysis of the complex permittivity (ε^*) data within the Z^* formalism ($Z^*=1/Y^*=1/i\omega C_o\varepsilon^*$) is commonly used to separate the bulk and the surface phenomena and

to determine the bulk dc conductivity of the material [16,20]. The complex impedance or the complex permittivity ($\varepsilon^*=1/M^*$) data were transformed into the M^* formalism using the following relation [16,17,19]

$$M^* = \frac{1}{\varepsilon^*} = M' + jM'' = \frac{\varepsilon'}{\varepsilon'^2 + \varepsilon''^2} + j\frac{\varepsilon''}{\varepsilon'^2 + \varepsilon''^2} \quad (7)$$

The real (M') and the imaginary (M'') components of the complex electric modulus (M*) were calculated from the ε' and ε'' values.

The frequency dependence of ε', ε'', tanδ at room temperature for MIS and MOS structures are shown in Fig. 1(a), (b) and (c), respectively. The values of ε', ε'' and tan δ were found to be strong functions of frequency. As can be seen from these Fig. 1 (a), ε' decrease with an increase in frequency for MIS and MOS structures. This is the normal behavior of a dielectric material. In principle, at low frequencies, all the four types of polarization processes, such as, the electronic, ionic, dipolar, and interfacial or surface polarization contribute to the value of ε' [16-19]. With increasing frequency, the contributions of the interfacial, dipolar or the ionic polarization become ineffective by leaving behind only the electronic part. Furthermore, the decrease in ε' an increase in frequency is explained by the fact that as the frequency is raised, the interfacial dipoles have less time to orient themselves in the direction of the alternating field [21-25]. The ε' values of MIS and MOS structures have values of 2.73, 3.60 at room temperature, respectively. This result shows that the strong low-frequency dispersion that characterizes the frequency dependence of ε' of MIS and MOS structures (in Fig. 1(a)) has not been clearly understood. But in general, four possible mechanisms; electrode interface, ac conductivity, dipole-orientation and charge carriers may contribute to below-frequency dielectric behavior of MIS and MOS structures [16-19,22,24–26]. Especially, in the high frequency range, the values of ε' become closer to the values of ε. This behavior of ε' may be due to the interface states which cannot follow the ac signal at high frequencies since the carrier lifetime of interface trapped charges (τ) are much larger than 1/ω at very high frequency (ω). Such this behavior was also observed by several authors [27-29]. Fig. 1 (b) and (c) show the variation of ε'' and tanδ with frequency at room temperature. If the electric polarization in a dielectric is unable to follow the varying electric field, dielectric loss occurs. An applied field will alter this energy difference by producing a net polarization, which lags behind the applied field because the tunneling transition rates are finite. This part of the polarization, which is not in phase with the applied field, is termed as dielectric loss [30]. As shown in Fig. 1 (b) and (c) for MIS structure, in the frequency range from 10 to 200 kHz the values of ε'' and tanδ decrease with the increasing frequency, but approximately in the frequency range from 200 kHz to 2 MHz the values ε'' and tanδ increase with the increasing frequency.

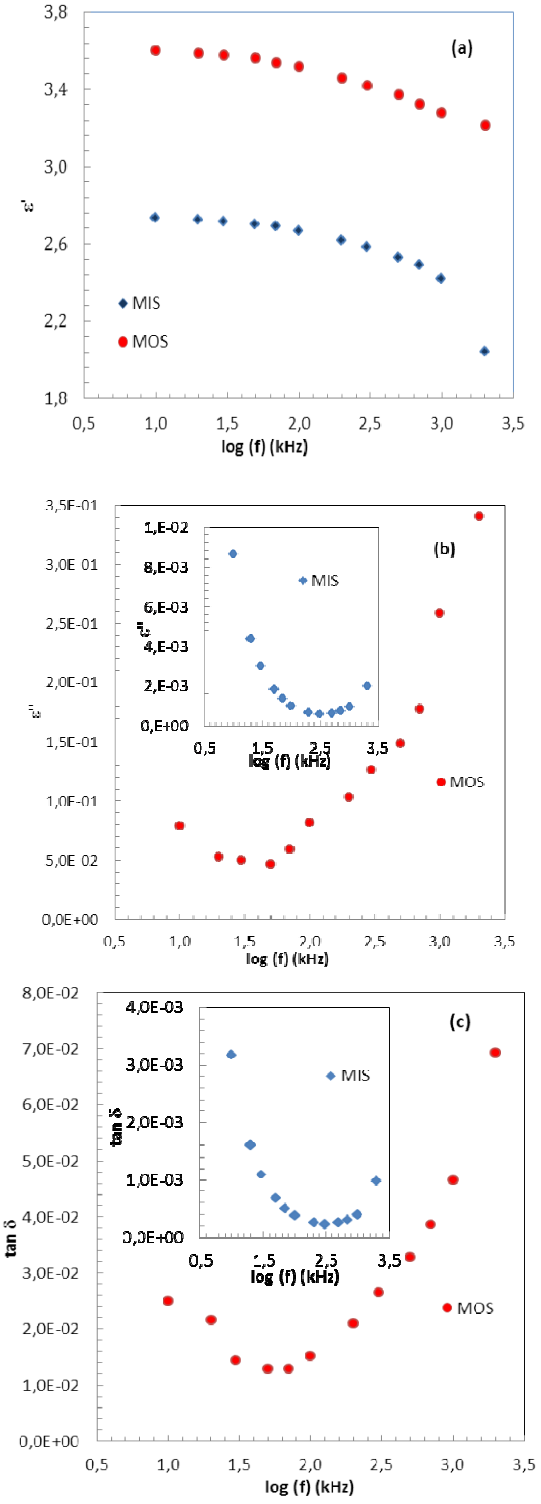

Fig. 1. Frequency dependence of the (a) ε', (b) ε'' and (c) tanδ at room temperature for MIS and MOS structures.

Also, as shown in Fig. 1 (b) and (c) for MOS structure, in the frequency range from 10 to 50 kHz the values of ε'' and tanδ decrease with the increasing

frequency, but approximately in the frequency range from 50 kHz to 2 MHz the values of ε'' and tanδ increase with the increasing frequency. It is clear that ε'' and tanδ are in close relation with the conductivity. The increase in the conductivity σ is accompanied by an increase in the eddy current. Fig. 2 depicts the variation of the ac conductivity σ_{ac} with frequency (in the frequency range 10 kHz–2 MHz) at room temperature for MIS and MOS structures, respectively. It is noticed that the values σ_{ac} decrease with the decreasing frequency.

This behavior is typical for these structures and can be ascribed to the space charge polarization. As the frequency decreases, more and more charge accumulation occurs at the insulator semiconductor interface, which leads to a drop in the conductivity at low frequencies. Similar behavior was also observed in the literature [23,26,31,32].

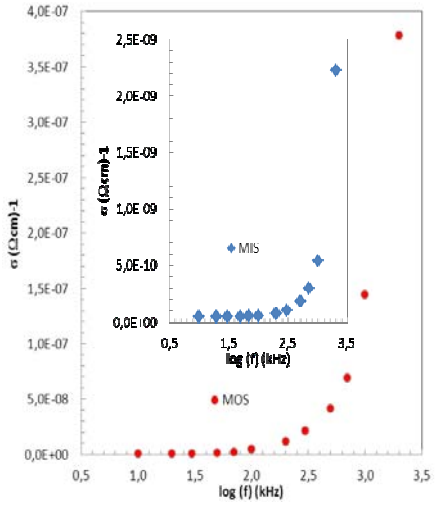

Fig. 2. Frequency dependence of ac electrical conductivity (σ_{ac}) at room temperature for MIS and MOS structures.

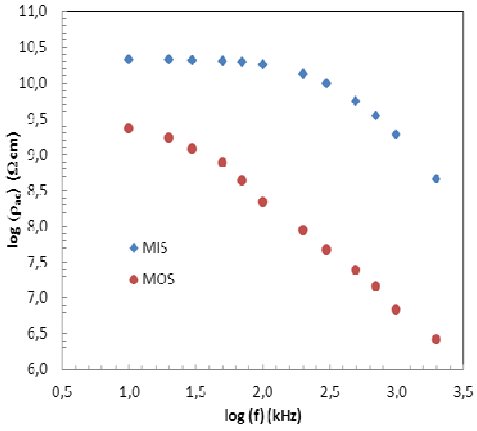

Fig. 3. Plot of log ρ_{ac} vs. log f for MIS and MOS structures at room temperature.

In addition, Fig. 3 shows the variation of log resistivity (log ρ_{ac}) with log frequency of MIS and MOS structures at room temperature. Both of the structures show a decrease in ρ_{ac} with the increase in frequency from 10 kHz to 2 MHz. The increase in frequency of applied field enhances the hopping of the charge carriers, resulting an increase in conductivity and decrease in resistivity. At higher frequencies ac resistivity decreases and remains constant because of the fact that hopping frequency can no longer follow the frequency of the applied external field leading to lower values of ac resistivity [33,34]. The complex modulus plane analysis is based on the plot of the real part of M' versus the imaginary part of M'' over a wide range of frequencies.

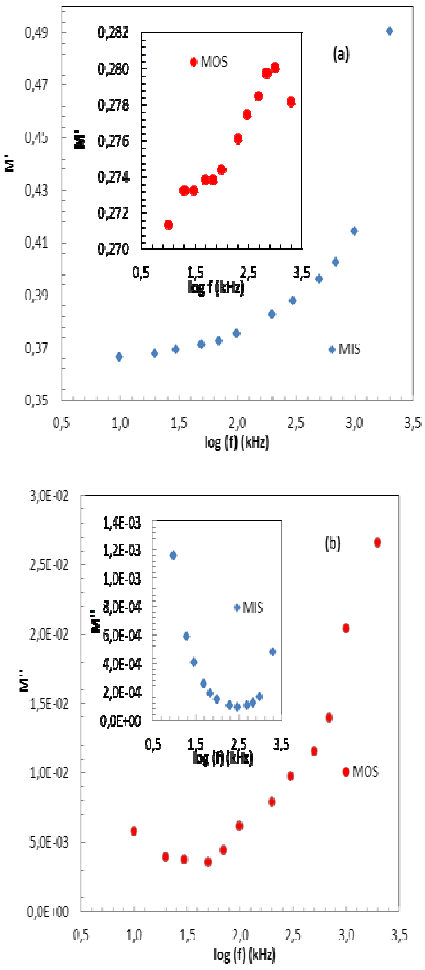

Fig. 4. (a) Real (M') and (b) imaginary (M'') parts of electric modulus M, at room temperature over a measured frequency range of 10 kHz-2 MHz for MIS and MOS structures.*

Fig.4 (a) and (b) show the M' and M'' of electric modulus M* versus frequency for MIS and MOS structures at room temperature. As can be seen from the figures, as the frequency is increased, M' increases to a maximum. Also, M' increases as the frequency is increased and there are a sharp increases especially in the M' in the frequency range between 100 kHz and 2 MHz.

As shown in Fig. 4 (b) for MIS structure, in the frequency range from 10 to 200 kHz, the values of M" decrease with the increasing frequency, but approximately in the frequency range from 200 kHz to 2 MHz the values of M" increase with the increasing frequency. Also, as shown in Fig. 4 (b) for MOS structure, in the frequency range from 10 to 50 kHz the values of M" decrease with the increasing frequency, but approximately in the frequency range from 50 kHz to 2 MHz, the values of M" increase with the increasing frequency. Similar studies have been reported in literature [31,34-39].

4. Conclusions

Frequency dependence of dielectric properties and ac electrical conductivity (σ_{ac}) of MIS and MOS structures has been studied in detail in the frequency range 10 kHz-2 MHz at room temperature. The analysis of the experimental results has shown that the values of ε' decrease with the increasing frequency for MIS and MOS structures. These behaviors are attributed to the decrease in polarization with the increasing frequency in SiO_2/p-Si interface. The observed high values of ε' at low frequencies are attributed to conductivity which is directly related to the increase in the mobility of localized charge carriers at interface states. In addition, the values of ε" and tanδ show a minimum or U shape behavior. Such behavior of these structures can be attributed to particular distribution of interface states at Si/SiO_2 interface. Also, the values of σ_{ac} decrease with the decreasing frequency because of the accumulation of charge carries at the boundaries. The high values of ε', ε" and σ_{ac} for MOS structure can be attributed to the magnitude of oxide trapped charges in the SiO_2 layer. It's clear that the behavior of dielectric properties especially depends on frequency, thickness of interfacial insulator layer, the interface traps and oxide charges.

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