A study examining the influence of various design and process parameters on the solder joint thickness of 0805 components

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This paper presents part of the results obtained after conducting an experiment designed with the help of the Design of Experiments (DoE) method. The aim of this experiment is to evaluate the dependencies between the layout design and the production quality of surface mount (SMT) boards. The DoE method was used to plan the variation of certain factors in order to see their influences on the responses. In this paper, we will focus on the interpretation of the results obtained after measuring the distance between the board surface and the bottom side of a chip component 0805.

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1. Introduction

The primary goal of this study is to analyse the quality of solder joints using the Design of Experiments method which means planning the variation of certain factors in order to see their influences on the response variables.

This type of statistical test planning allows the analysis of technical processes taking into account many factors with a minimum of test effort [1].

A test board was specially designed to allow us to vary certain factors. This board was designed in an effort to represent potential pad designs for chip components [2]. Seven different combinations of surface mount (SMT) footprint designs were created to evaluate the effects of the layout design on the quality of SMT boards [3]. The length and width of the pads as well as the spacing between the pads were modified starting from two IPC standards: IPC-SM-782 and IPC-7351 [4] [5].

The factors taken into consideration and the description of their levels are presented in table 1.

Table 1. The factors and the description of their levels.

Factor	No. of levels	Description of levels
Pad width	3	minimum, standard, maximum
Spacing	2	standard, maximum
Pad length	2	minimum, standard
Form of stencil apertures	3	rectangular, home plate and inverted home plate
Stencil thickness	2	100 μm and 150 μm
Solder paste	3	Type A, Type C and Type L
Surface finish	3	chemSn, ENIG and HASL
Thermal profile	3	Convection 230^0C, Convection 250^0C , VPS

A total of 108 test boards were assembled and 828 passive components were used to populate each board. The number of chip components size 0805 analysed on each board is 180, both resistors and capacitors.

2. Stand-off height

In mechatronics, electronics and optoelectronics, the standoff is defined as being a separator between two parts. In electronic technology, the stand-off or stand-off height is defined as the distance between the printed circuit board (PCB) surface and the bottom side of the chip component.

The stand-off height is hard to measure or to compute, so in order to determine it or find out some information about it (by computation or by approximations) several methods have been developed.

Fig. 1 shows the representation of a chip component soldered onto a PCB. The stand-off height is designated with 'h'.

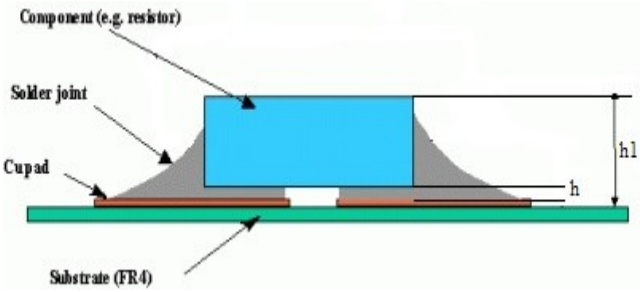

Fig. 1. Representation of a chip component soldered onto a PCB.

The stand-off achieved for a particular component will depend on:

- The design and manufacturing tolerance of leads and body;
- The combined effects of board warp and lead non-coplanarity;
- Any distortion of the component body (for example, popcorning effect);
- Any additional copper tracks or legend under the component [6];
- The thickness and variability of the solder mask.

3. Computing the stand-off height

There are several methods for computing or measuring the stand-off height:

1. Using the measurements of the components' heights we can theoretically compute the stand-off height:

$$stand\_off = h_m - h_{comp} \quad (1)$$

where h_m is the measured height and h_{comp} is the height of the component.

As simple as it is, this method gives most of the time wrong results because the height of the component may vary. The tolerance for the component's height, though specified in the component's datasheet and thus known, is usually much bigger than the stand-off height which for example may be around 50 µm.

2. Another method to find information about the stand-off height is to make the difference between the height measured after placement (h_{as}) and the height measured after soldering (h_{sold}) for the same component (fig. 2).

$$h_{as} = h_{pad} + h_{solder1} + h_{comp} \quad (2)$$

$$h_{sold} = h_{pad} + h_{solder2} + h_{comp} \quad (3)$$

where h_{pad} is the height of the pad (copper foil plus surface finish [7]), h_{comp} is the height of the component, $h_{solder1}$ is the thickness of the paste before soldering and $h_{solder2}$ is the thickness of the joint after soldering.

When we make the difference between the heights measured before and after soldering we get the difference in the height of the solder before and after soldering. Although the height of the copper foil which constitutes the pad on the PCB and the height of the component have tolerances [8], the height difference for the solder does not depend on them:

$$h_{as} - h_{sold} = h_{solder1} - h_{solder2} \quad (4)$$

This difference contains much more information than the stand-off height alone.

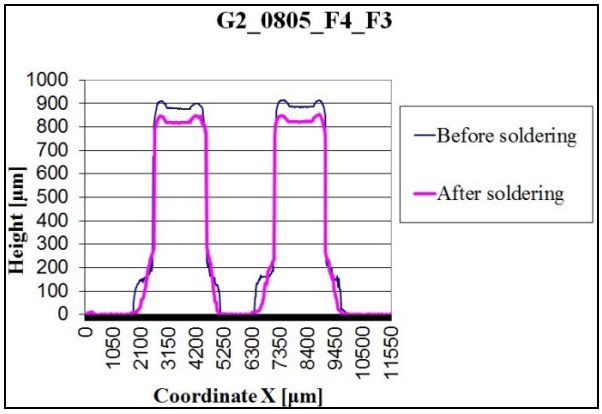

Fig. 2. The heights measured before and after reflow for the same two 0805 chip components.

3. Yet another way to measure the stand-off height is to cut a single component from the board and put it in resin. After that we can make a micro-section (cross-section) and then measure the exact thickness of the solder joint.

Although this method is the most trustworthy, we cannot use it because it means destroying the boards and not being able to do any other measurements afterwards.

4. Measuring the stand-off height

For our experiment, we have used the second method, i.e. we measured the heights of the components on the board before and after soldering. The heights of the components on the board can be measured with the help of the NanoFocus equipment named 'µScan'. The equipment has a sensor which scans the surfaces and presents the results as a graph in the program named 'NF_AutoScan'.

Fig. 3 shows a graph for one component on the test board after printing and placement but before soldering.

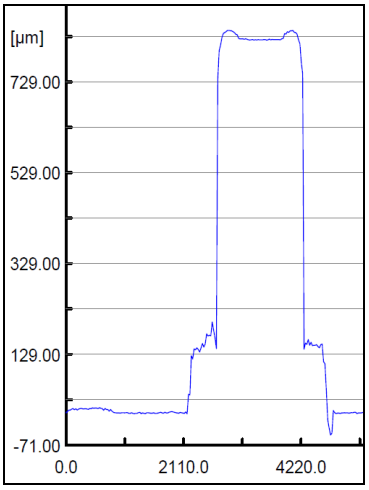

Fig. 3. Example of graph obtained for one component on the test board.

In order to compute the height of the component based on this graph, we need to establish a base level for the board. We can do this easily with the help of the 'µScan' software. We choose the most appropriate intervals for regression and then the software returns us the base level for the board.

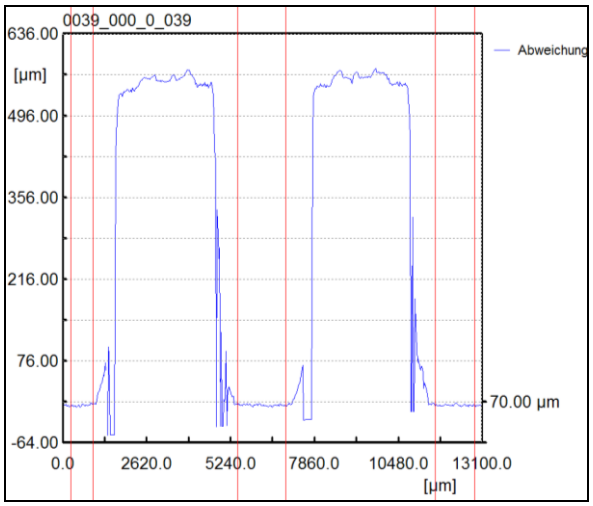

Fig. 4. The most appropriate intervals chosen for regression.

The graph in fig. 4 presents the measured results for two components. The vertical lines bound the three intervals chosen for regression. In the end, this is where the base level of the board is established.

The spikes which can be seen in the graph in fig. 4 are due to the reflection over a shiny metal surface like that of a solder joint. They are not to be taken into consideration when choosing the regression intervals when computing the base level of the board.

After the base level of the board is established, the software can compute the height of the component placed on the board (fig. 5). The height is measured in µm. In fig. 1, the height of the components on the board is designated with 'h1'.

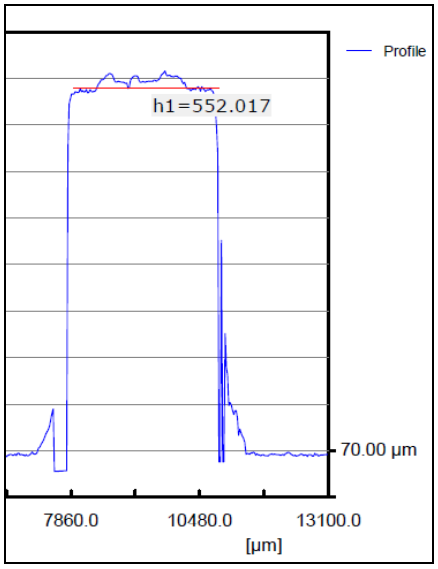

Fig. 5. The measured height for one component.

In order to scan the surface of a printed circuit board with components assembled, the sensor of the Nano Focus µScan equipment has to be positioned at a certain height over the board.

5. Results

As said above, it is hard to measure the real stand-off height thus several methods of obtaining information about it were developed. We have used the following method: we have measured the height of the component after placement on the solder deposits before soldering, we have measured the height of the component on the board after soldering and we have computed the difference between the two values obtained. This difference gives us information about the change in the real stand-off heights before and after soldering.

This experiment was designed and the results were analysed with the help of the DoE method.

The results of the computed stand-off difference were introduced in the database of a statistical software. The procedure "Analysis of Variance – Multifactor ANOVA" was performed, i.e. a multifactor analysis of variance for the stand-off difference. This procedure constructs various tests and graphs to determine which factors have a statistically significant effect on our response variable [2]. It also tests for significant interactions among the factors, given there is sufficient data. The F-tests in the ANOVA table will allow us to identify the significant factors. For each significant factor, the Multiple Range Tests will tell us which means are significantly different from which others. The Means Plot and Interaction Plot will help us interpret the significant effects. The Residual Plots will help us judge whether the assumptions underlying the analysis of variance are violated by the data.

The results obtained after the Analysis of Variance was performed are shown below as Pareto charts and graphs. A Pareto chart is usually used in statistical analysis

and other disciplines to show which factors contribute the most to a given problem [1]. In our case, the Pareto chart shows us which factors and which interactions have a statistically significant influence on the stand-off difference. In figure 6, the vertical line represents the limit from where the factors are considered significant.

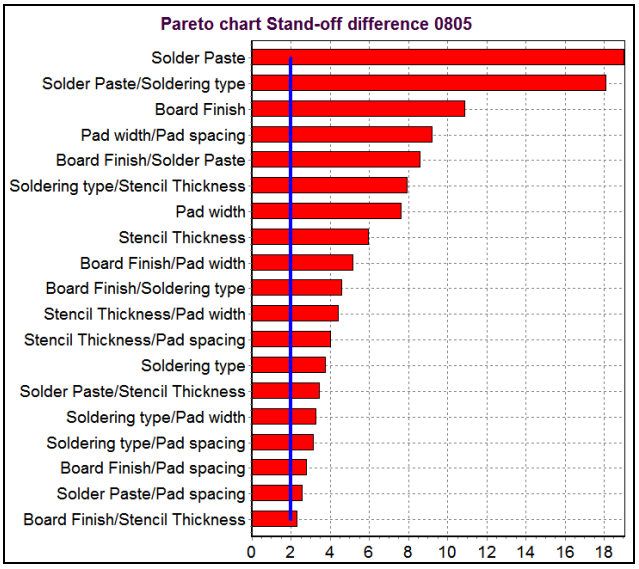

Fig. 6. The Pareto chart for the stand-off difference.

The Pareto chart in fig. 6 shows us that the interaction between the pad width and the spacing between the pads is statistically significant. The interaction plot is presented in fig. 7.

So far the analysis of the stand-off difference shows that the factors that influence it the most are: solder paste (fig. 8), surface finish, stencil thickness, soldering type and the interactions between them. After them, there come the factors related to the layout design: pad width, pad spacing, pad length, with a smaller influence but still significant.

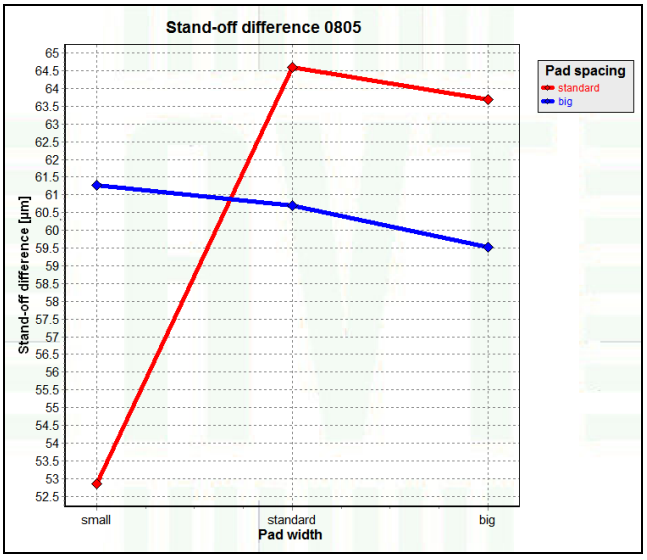

Fig. 7. The interaction plot between the pad width and pad spacing.

As we can see in figure 7, the stand-off difference is a little bit smaller when the spacing is bigger than standard for all values of the pad width. This is due to the fact that when the spacing is bigger the components stay on the pad only with their terminals which are very small. The melted alloy will spread more on the pad outside the components' body. A particular case seems to be when the pad width is smaller than standard and the spacing is standard. In this case, the difference in stand-off is quite big.

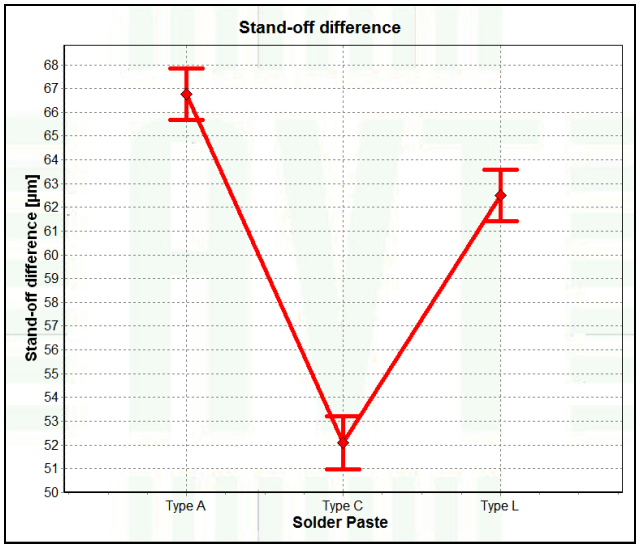

Fig. 8. The stand-off difference for the three types of solder paste.

The stand-off difference is closely related to the thickness of the solder joint under the components' terminals. It is the general belief that if this thickness has big values then the solder joint is more robust. In fig. 8 we can see that solder paste type C gives the smallest stand-off difference of the three solder pastes used in this experiment.

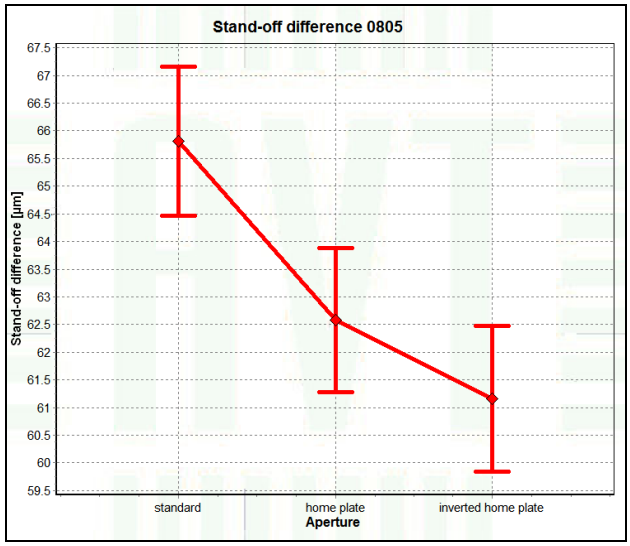

Fig. 9. The influence of the geometry of the apertures on the stand-off difference.

Fig. 9 presents the influence of the geometry of the apertures of the stencil on the stand-off difference. As shown in table 1, three designs for the apertures of the stencil were used: rectangular (standard), home plate and inverted home plate [9]. This factor does not have a significant influence on our response variable.

6. Conclusions

The results presented here were obtained in the framework of a complex study whose main goal was to evaluate the effects of the layout design and the production quality of SMT boards. For this purpose, the Design of Experiments technique was employed.

The method employed by us is not exact but it is a good way to obtain information about the real stand-off height and implicitly about the solder joint thickness.

The analysis of the values obtained for the same chip component reveals that the stand-off difference (as we defined it) has the smallest value when the pad width is smaller than standard. The pad length doesn't have a very significant influence while the pad spacing is significant only when it interacts with the other factors. When it comes to the geometry of the apertures of the stencil, there is a very small difference in the values of the stand-off for a standard rectangular aperture and "home plate" or "inverted home plate" apertures. This difference is given by the paste volume which is smaller in the case of "home plate" and "inverted home plate" designs as compared to the standard design.

References

[1] W. Sauer, M. Oppermann, G. Weigert, S. Werner, H. Wohlrabe, K.-J. Wolter, T. Zerna, Design of Experiments and Regression Analyses, Springer Publishing Company, p. 374, 2006.

[2] H. Wohlrabe, K.-J. Wolter, Practical Usage of Design of Experiments in the Production of SMT-Boards, Conference Proceedings, The 30th International Spring Seminar on Electronics Technology (ISSE 2007), Cluj-Napoca, Romania, 9-13 May, 414 (2007).

[3] A. Drumea, Magazine of Hydraulics, Pneumatics, Tribology, Ecology, Sensorics, Mechatronics, **3-4**, 54 (2012).

[4] ***, IPC-SM-782 – Surface Mount Design and Land Pattern Standard, 1993, www.ipc.org.

[5] ***, IPC-7351 – Generic Requirements for Surface Mount Design and Land Pattern Standard, 2005, www.ipc.org.

[6] D. Benea, S. Mican, I. Stanciu, A. F. Takacs, V. Pop, J. Optoelectron. Adv. M., **17**(5-6), 90 (2015).

[7] I. G. Ştefănescu, I. Ciucă, J. Optoelectron. Adv. M., **15**(7-8), 734 (2013).

[8] M. Ozayman, Y. O. Ciftci, K. Colakoglu, E. Deligoz, J. Optoelectron. Adv. M., **13**(5), 565 (2011).

[9] ***, IPC-7525A – Stencil Design Guidelines, www.ipc.org.

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