An improved SPICE model for low-voltage power MOSFET devices

A. GALADI[a*], M. M. HASSANI[b]
[a]Laboratoire Environnement et Energie Renouvelable, Faculté des Sciences, Département de Physique, Université Ibn Tofail, Kenitra, Morocco
[b]Laboratoire Electronique et Instrumentation, Faculté des Sciences, Département de Physique, Université Cadi Ayyad, Marrakech, Morocco

In this paper new SPICE power MOSFET model is presented. This model is based on physical structure of power MOSFET and describes more accurately the all operation regions of the device. The new semi-empirical model uses new expressions of the current-voltage relationship in the linear and subthreshold regions. The proposed model is validated by comparison between simulation and experimental data.

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1. Introduction

Power MOSFET is a widely used power device in low voltage power conversion energy thanks to its high switching speed, high input impedance and thermal stability. Power VDMOSFET structure (Fig. 1) contains a low-doped epitaxial drain layer N^-, called "drift region", to sustain the breakdown voltage in the off-state. The breakdown voltage depends on the thickness and the doping level of the drift region. In the case of unipolar devices like VDMOSFET, the drift resistance increases drastically with increase of the breakdown voltage [1]. Therefore, the classical power MOSFET was limited to moderate voltage applications. Recently, new power MOSFET configurations, like Superjunction MOSFET [2], and new high-voltage (SiC, GaN) power MOSFET devices [3] have been proposed to improve the on-resistance of power MOSFET devices.

Manufacturers give the SPICE parameters of their power MOSFETs for electrical simulations. The most manufacturers use the SPICE level 1 and SPICE level 3 MOS models to represent the active channel region of their power MOSFET. SPICE level 1 is a simplest model which doesn't take into account the drain induced barrier lowering (DIBL) and the weak inversion drain current. Therefore, the level 1 model is not appropriate for short channel power MOSFET.

SPICE level 3 MOS model is a semi-empirical model based on experimental characterization which takes into account the DIBL and the weak inversion drain current. Nevertheless, in the SPICE level 3 MOS model the drain current is not well defined in transition and saturation regions [4]. Therefore, an important mishmash can be observed when compared the simulated and experimental results in the saturation region. This phenomenon occurs generally in the low voltage, high current power MOSFET devices.

This paper focuses on new modeling of low-voltage power MOSFETs. This modeling is based on device physics and uses new expressions for the current-voltage characteristics in all operating regions of the low-voltage power MOSFET. Consequently, the new model defines more accurately all operating regions unlike the SPICE level 3 MOS model. In addition, the most model parameters are extracted using the experimental data. The new model is validated by comparing the simulated and measured static and dynamic characteristics.

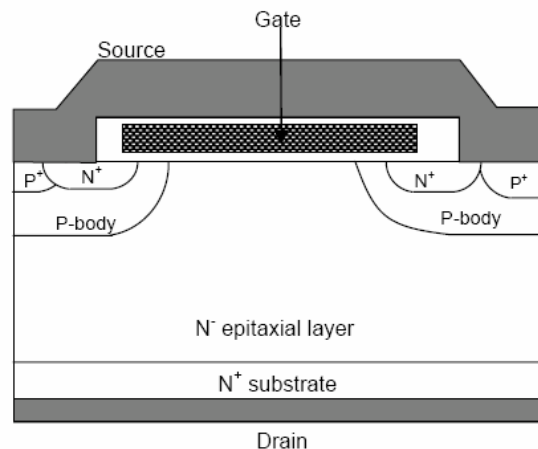

Fig. 1. Cross section of the conventional power VDMOSFET

2. Model for low voltage power MOSFET

2.1 Extraction and localization of the subcircuit elements

Fig. 2 shows a cross section of the power VDMOSFET with the different regions of the structure

and the localization of the simplified model elements. Each region of the power VDMOSFET — (1) channel, (2) access, (3) PN junctions, (4) drift and (5) substrate — is described taking into account peculiar characteristics of the power device: short channel length, channel carrier mobility roll-off, current spreading in the bulk…

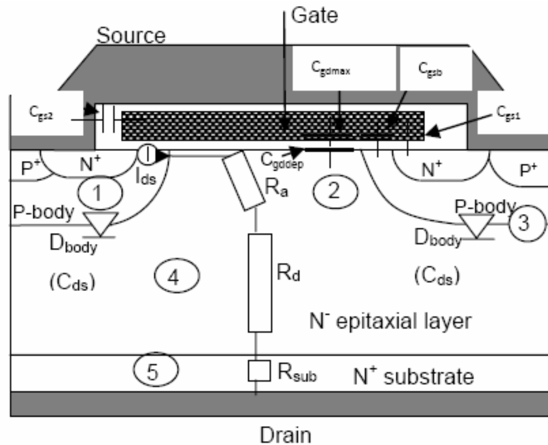

Fig. 2: Location of some items of the complete power VDMOSFET model.

The equivalent subcircuit model of the power VDMOSFET is shown in Figure 3. The short channel NMOS M1 (Fig. 3) describes the current generator I_{ds} in the channel region (Fig. 2).

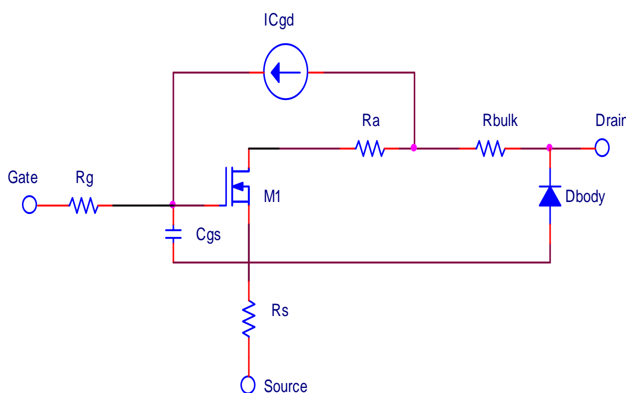

Fig. 3. Power VDMOSFET subcircuit model.

The access resistance R_a is due to the N^- accumulation region under the gate and to the JFET region between the adjacent P source diffusions, R_{bulk} is the sum of the drift and the substrate resistances (R_d and R_{sub} respectively in Fig. 2), R_s is the resistance of the N^+ source diffusion and R_g is the resistance of the polysilicon gate.

Other authors have described the quasi-saturation effect by non-linear resistances R_{bulk} and R_a [5]: this phenomenon occurs in the high voltage MOS devices when the drain current is sufficiently high for the mobile carrier density in the lightly doped drain to approach the mobile carrier density of the background doping. In the case of the low-voltage power MOSFET, where the quasi saturation effects are not important, R_a and R_{bulk} can be modeled using ordinary constant resistances.

The gate-to-source capacitance C_{gs} is the sum of three capacitances in parallel: C_{gs1}, due to the overlap of the gate electrode over the N^+ source diffusion, C_{gs2}, between source and gate electrodes, and C_{gsb}, between the gate electrode and the P-body source.

The gate-to-drain Miller capacitance C_{gd} can be represented by the series association of a constant capacitance C_{gdmax} (oxide capacitance between the gate electrode and the N^- intercellular region) and the non-linear depletion capacitance C_{gddep} (corresponding to the depletion intercellular region under the gate when V_{dg} is positive). In this paper the model proposed to describe the proper behavior of the Miller capacitance C_{gd} is the "current source model" (Fig. 3). This current source is implanted in SPICE under an analytic form by using block-diagrams in ABM modules.

The drain-to-source capacitance C_{ds} is taken into account by the transition capacitance of the Dbody diode (Fig. 3).

2.2 Power MOSFET static model

The static characteristics of the power VDMOSFET model are determined by the MOSFET transistor M1 (representing the current generator I_{ds} in Fig. 2), the accumulation resistance (R_a), the bulk resistance (R_{bulk}) and the Dbody diode (breakdown voltage and source-drain diode forward characteristics).

The power MOSFETs are used as switches to control the electric energy. Special attention should be given to the static characteristics, when the conducting MOSFET behaves like a resistance (for low V_{ds}) in linear region. At low V_{ds}, we can estimate the conduction losses. The threshold voltage, V_T, is a key parameter: it separates the on-state (above-threshold) and the off-state (sub-threshold) of the transistor.

In this paper, modeling of the subthreshold region in low-voltage power MOSFET is presented. This modeling is based on an empirical equation using extracted parameters to fit the measured data. Therefore, the proposed model will accurately estimate all operating regions of the low-voltage power MOSFET devices.

Our static behavior description of the M1 MOSFET is done by using two models. The first is the SPICE level 3 MOS model, widely used for power MOSFET models, but not very precise to describe the subthreshold and the saturation-transition regions of the MOSFET devices. The second model describes more precisely all operating regions of the MOSFET than the SPICE level 3 MOS model.

2.2.1 SPICE level 3 model

A. Linear and saturation currents

In SPICE level 3 MOS model, the drain currents in the linear and saturation regions are expressed respectively by the following relationships:

$$I_{ds} = \mu_{eff} \frac{W}{L} C_{ox} \left[\left(V_{gs} - V_{th} \right) . V_{ds} - \alpha . \frac{V_{ds}^{\ 2}}{2} \right] \quad (1)$$

$$I_{ds} = \mu_{eff} \frac{W}{L} C_{ox} \left[\left(V_{gs} - V_{th} \right) . V_{dsat} - \alpha . \frac{V_{dsat}^{\ 2}}{2} \right] \quad (2)$$

where W and L are the channel width and length respectively, C_{ox} is the gate oxide capacitance per unit area, V_{ds} is the drain-source voltage applied to the channel, V_T is the threshold voltage, V_{gs} is the gate-source voltage, V_{dsat} is the drain-source voltage at the beginning of the channel pinch-off and α is a coefficient related to short and narrow channel effects. The effective carrier mobility in the inversion layer (μ_{eff}) takes into account the carrier saturation velocity in the channel (V_{max}) and the reduction of mobility due to the high electric field:

$$\mu_{eff} = \frac{\mu_S}{1 + \frac{\mu_S . V_{ds}}{V_{max} . L}} \text{ with: } \mu_S = \frac{\mu_0}{1 + \Theta . \left(V_{gs} - V_T \right)} \quad (3)$$

where μ_S is the surface mobility in the channel inversion layer, that depends on the transverse electric field Θ — roll-off coefficient — and μ_0 is the low electric field mobility.

The SPICE parameters are extracted and specified from measurements. At low drain voltage, the transconductance parameter, K_P, can be extracted from the slope factor, β, of the transfer characteristic $I_{ds}(V_{gs})$:

$$\beta = \mu_{eff} \cdot C_{ox} \cdot \frac{W}{L} = K_P \cdot \frac{W}{L} \quad (4)$$

β is the gradient of the transfer characteristic, $I_{ds}(V_{gs})$, neighbouring the threshold voltage at low drain voltage (V_{ds}=10 mV) in the linear region. It allows calculation of the transconductance SPICE parameter "K_P". In the saturation region, the drain saturation current is determined by the carrier saturation velocity in the channel (V_{max}). Consequently, the SPICE parameter V_{max} can be obtained by adjustment of the level of the drain current in the saturation region. The SPICE parameter Θ (peculiar to SPICE level 3 model) can be specified in the .model statement to show the dependence of the mobility on the gate electric field. The mobility modulation parameter Θ depends on the oxide thickness.

For low-voltage power MOSFETs, the threshold voltage can be given by:

$$V_{th} = V_T - \sigma(ETA) \cdot V_{ds} \quad (5)$$

where σ(ETA) is a factor which expresses the dependence of the threshold voltage on V_{ds}. ETA is a SPICE level 3 MOS model parameter.

B. Subthreshold current

In SPICE level 3 MOSFET model, the transition point from weak to strong inversion regions is defined with a modified voltage V_{ON}:

$$V_{ON} = V_{th} + fast(NFS) \quad (6)$$

fast(NFS) is a voltage used to evaluate V_{ON}. This voltage depends on the SPICE MOS level 3 parameters NFS, GAMMA and PHI. GAMMA and PHI are extracted from V_{th} versus V_{SB} measurements.

The drain current in subthreshold region, $V_{th} < V_{ON}$, is given by:

$$I_{ds} = I_{ds}(V_{ON}, V_{DS}, V_{SB}) \exp^{\left(\frac{V_{gs} - V_{ON}}{fast(NFS)} \right)} \quad (7)$$

$I_{ds}(V_{ON},V_{DS},V_{SB})$ is the current given from the relation (1), with V_{GS} replaced by V_{ON}.

V_{SB} is the source-bulk voltage. In this work, V_{SB} = 0 V.

The main problems of the SPICE level 3 MOSFET model can be summarized as:

- In strong inversion, the description of the transition region – between the linear and saturation region – is not very precise when V_{gs} increases. This is due to the first derivative discontinuity in the drain current equation at $V_{ds}=V_{dsat}$. Consequently, simulation error in transition and saturation regions can be noticed.

- Level 3 MOS model not provide the subthreshold current if the NFS parameter is not specified. The transition gate-source voltage between the weak and strong inversion regions is calculated using NFS, GAMMA and PHI SPICE level 3 MOS parameters. This calculated gate-source transition voltage is not very well defined and need measurements of V_{th} versus V_{SB}. Therefore, drain-source current anomalies will usually occur in the subthreshold region.

For the first problem, we have introduced a new drain current equation in the linear region to eliminate the discontinuity problem [6].

For the second problem, an empirical equation describing the subthreshold current is added to complete the dc new low voltage power MOSFET model [6]. In power MOSFET device the source and bulk are usually connected together. Therefore we cannot extract GAMMA and PHI parameters (V_{SB}=0).

In this work, we have chosen to define the subthreshold current with a simple empirical equation using an extracted gate-source transition voltage. This transition gate-source voltage separates the subthreshold and the linear operation regions. The new model is close to SPICE level 3 model, except that the drain current equations in the subthreshold and the linear regions are modified.

2.2.2 The new SPICE model

A. Linear and saturation currents

The new drain current equation in the linear region can be written as [6]:

$$I_{ds} = \left(\beta \cdot (V_{gs} - V_{th}) - b \cdot V_{ds}\right) \cdot V_{ds} \quad (8)$$

We choose that the maximum value of this equation will correspond to the saturation current defined in the SPICE level 3 MOS model. The first derivative of the proposed equation allows the determination of the pinch-off voltage V_p ($V_p = \frac{\beta \cdot (V_{gs} - V_{th})}{2 \cdot b}$). At this voltage ($V_{ds} = V_p$), equation (8) allows the calculation of the b parameter. In conclusion, the drain currents I_{ds}, I_{dsat} and the pinch-off voltage V_p can be written as [6]:

$$I_{ds} = \beta \cdot (V_{gs} - V_{th}) \cdot \left(1 - \frac{\beta \cdot (V_{gs} - V_{th})}{4 I_{dsat}} V_{ds}\right) \cdot V_{ds} \quad (V_{ds} \le V_p) \quad (9)$$

$$I_{dsat} = \beta \cdot \left((V_{gs} - V_{th}) - \frac{V_{dsat}}{2}\right) \cdot V_{dsat} \quad (V_{ds} \ge V_p) \quad (10)$$

$$V_p = \frac{2 \cdot I_{dsat}}{\beta \cdot (V_{gs} - V_{th})} \quad (11)$$

These expressions are implanted in SPICE under an analytical form.

B. Subthreshold current

The transition between the weak and strong inversion regions is defined by an empirical voltage V_{gst}. This voltage V_{gst} is extracted from the $\ln(I_{ds})=f(V_{gs})$ experimental curve. The subthreshold current is given by the following equation when $V_{gs0} < V_{gs} < V_{gst}$:

$$I_{ds} = I_{ds0} \exp\left(\frac{V_{gs} - V_{gs0}}{nU_T}\right) \quad (12)$$

Where V_{gs0} is the empirically-determined gate voltage at the beginning of the linear curve $\ln(I_{ds})=f(V_{gs})$ in subthreshold region, I_{ds0} is the drain current at $V_{gs} = V_{gs0}$ and $\frac{1}{nU_T}$ is the slope factor of the experimental curve $\ln(I_{ds})=f(V_{gs})$.

The n parameter can be extracted from the slope factor of the $\ln(I_{ds})=f(V_{gs})$ experimental curve.

2.3 VDMOSFET dynamic model

The dynamic model is based on the static model which is completed by the interelectrode capacitances.

2.3.1 Gate-to-source capacitance

As a first approximation, we consider that the gate-to-source capacitance C_{gs} is constant. C_{gs} is actually the sum of three capacitances (C_{gs1}, C_{gs2} and C_{gsb}). The oxide capacitances C_{gs1} and C_{gs2} are constant capacitances while C_{gsb} is a capacitance depending on the channel state (OFF: $C_{gsb} = 0$, ON: $C_{gsb} \neq 0$).

2.3.2 Drain-to-source capacitance

The non-linear behavior of C_{ds} as a direct function of V_{ds} is described by equation (13): as it can be seen in Figure 3, C_{ds} is modeled by the transition capacitance of the SPICE diode model ("Dbody" diode). This diode also takes into account the breakdown voltage of the power VDMOSFET (with the "BV" parameter, which is the reverse breakdown voltage in the SPICE model of the diode) and the drain-to-source capacitance variations versus drain-source voltage.

$$C_j = \frac{C_{j0}}{\left[1 - \frac{V_a}{V_j}\right]^m} \quad (13)$$

V_a is equal to the applied drain-source voltage (V_{ds}), C_{j0} is the zero bias capacitance, m is the grading coefficient and V_j is the diffusion voltage. C_{j0}, m and V_j are parameters of the SPICE diode model.

2.3.3 Gate-to-drain capacitance

The gate-to-drain Miller capacitance is a key parameter of the SPICE models for power MOSFETs. This Miller capacitance provides a feedback loop between the output and the input of the circuit limiting the frequency response of the transistor.

There is a large variety of SPICE MOSFET capacitance models to represent the non-linear capacitance C_{gd}. The gate-to-drain capacitance is modeled by a constant oxide capacitance C_{gdmax} when $V_{dg} \le 0$ V and by the series association of a constant oxide capacitance C_{gdmax} and a depletion capacitance C_{gddep} when $V_{dg} > 0$ V. Then the following expressions are used:

$$C_{gd} = C_{gd\max} \quad \text{for} \quad V_{dg} \le 0$$

$$C_{gd} = \frac{C_{gd\max} . C_{gddep}}{C_{gd\max} + C_{gddep}} \quad \text{for} \quad V_{dg} > 0 \quad (14)$$

where C_{gdmax}, corresponding to the gate oxide capacitance, is kept constant. The non-linear behavior of the depletion

capacitance C_{gddep} can be described by the transition capacitance of the SPICE diode model.

In this paper, the gate-to-drain capacitance is represented by a controlled current source formalism based on the "Analog Behavioural Model" module of SPICE (IC_{gd} — see Fig. 3 —). The delivered current is equal to:

$$I_{dg} = \frac{C_{j0}}{\left(1 + \frac{V_{dg}}{V_j}\right)^m} \cdot \frac{dV_{dg}}{dt} \tag{15}$$

3. Validation of the model

The measured and simulated output characteristics $I_{ds}(V_{ds})$ of the low voltage power MOSFET, called "FLIMOSFET", are shown in Figure 4 [6]. We can note that the SPICE level 3 and our model give identical results in the linear region. This is due to the fact that in the linear region (low V_{ds}), the drain current equations (1) and (9) have the same slope β. On the other hand, our model gives more accurate results in saturation region than the SPICE level 3 MOS model. The transfer characteristics $I_{ds}(V_{gs})$, given in Figure 5, confirm that our model fits correctly with experimental curves, validating the new formalism of the current in the saturation region of the device.

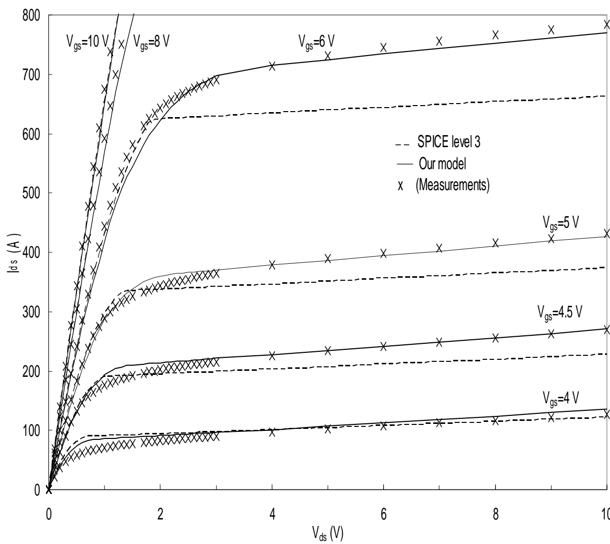

Fig. 4. VDMOSFET output characteristics.

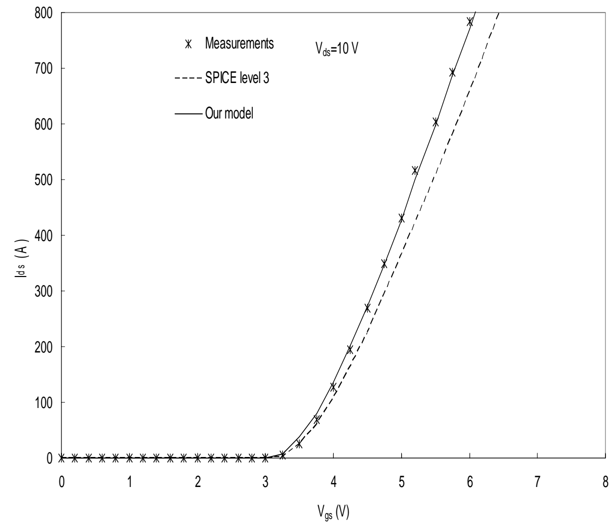

Fig. 5. VDMOSFET transfer characteristics.

Fig. 6 shows the simulated and measured subthreshold drain current characteristics $\ln(I_{ds})=f(V_{gs})$ of the low-voltage power FLIMOSFET. In the subthreshold region, the new model adequately fits the experimental data. On the other hand, the SPICE level 3 MOS model simulations and experimental measurements are not in good accordance. In SPICE simulation, the NFS SPICE level 3 MOS parameter was taken equal to 7×10^{11} cm^{-2}, which is a typical value of NFS.

Figs. 7 and 8 show the simulated and measured parasitic C_{ds} and C_{gd} capacitances. The agreement obtained is good. Finally, the good agreement between simulation and experimental results in the new model confirms the validity of the proposed model parameters.

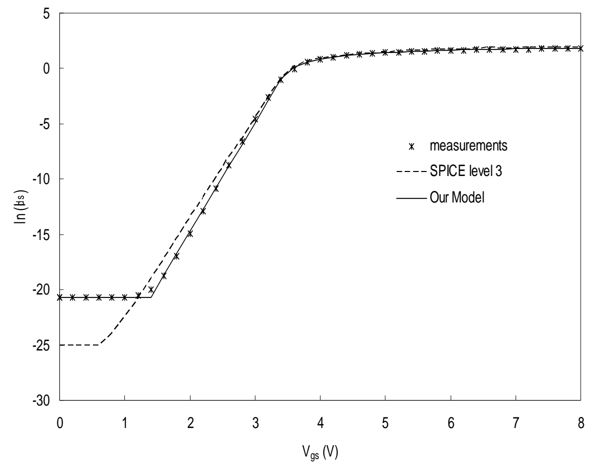

Fig. 6. VDMOSFET Subthreshold drain current versus V_{gs}.

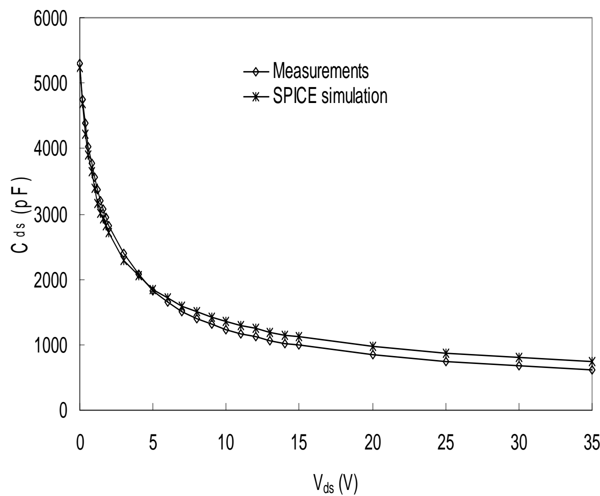

Fig. 7. Measured and SPICE simulated C_{ds} variations versus V_{ds}.

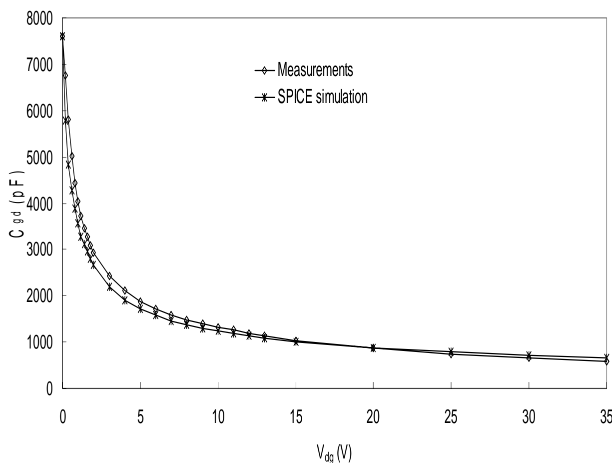

Fig. 8. Measured and SPICE simulated C_{gd} variations versus V_{dg}.

4. Conclusion

This study proposes a new SPICE model for the low-voltage power MOSFET taking into account the subthreshold current. This model is based on a new equation of the drain current in the linear region and uses an empirical equation for the subthreshold current modeling. Consequently, the new model describes more accurately all operating regions of the power MOSFET. This new model uses identical SPICE parameters as those of the SPICE level 3 MOS model in the linear and saturation regions. However, the subthreshold model parameters are empirical.

This proposed model gives better simulation in transition and saturation regions for high current low voltage power MOSFET devices.

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*Corresponding author:
GALADI-Abdelghafour@univ-ibntofail.ac.ma