Analysis of current-voltage characteristics of Au/n-GaAs (MS) Schottky diodes

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The current-voltage (I-V) characteristics of Au/n-GaAs (MS) Schottky diodes were investigated in the temperature range of 300-400 K. By using the thermionic emission (TE) theory, the forward bias I-V characteristics are analyzed to estimate the MS Schottky diode parameters. The estimated zero-bias barrier height (Φ_{Bo}) and ideality factor (n) considering TE theory show strong temperature dependence. While the n decreases, the Φ_{Bo} increases with the increasing temperature. The values of the n and Φ_{Bo} vary from 1.30 and 0.57 eV at 300 K to 1.12 and 0.66 eV at 400 K, respectively. Furthermore, the temperature dependence of energy distribution of interface states (N_{ss}) was obtained from the forward bias I-V measurements by taking the bias dependence effective barrier height (Φ_e) into account. The N_{ss} decreases with the increasing temperature. In addition, the values of series resistance (R_s) were determined using Cheung's method. The results show the presence of thin interfacial insulator layer between the metal and semiconductor.

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1. Introduction

Metal-semiconductor (MS) contacts are commonly known as the Schottky diodes. They are sometimes called as the surface barrier diode. Semiconductor devices are the basic components of integrated circuits and are responsible for the startling rapid growth of electronics industry [1-3]. Gallium arsenide (GaAs) is one of the advantageous semiconductors for high-speed and low-power devices. However, the performance of GaAs-based devices, including metal-semiconductor field effect transistors and heterostructure bipolar transistors, depends on the surface and interface defect density (N_{ss}) [4].

Metal-semiconductor interfaces have been the focus of extensive theoretical and experimental studies [5-13]. The interfaces between metal and semiconductor are very complex regions and their physical properties depend on surface preparation conditions. The interfaces play an important role on determination of barrier height and other characteristic parameters. These parameters can affect the performance, stability and reliability of the semiconductor device. [1,5,14]. Furthermore, electronic properties of a Schottky diode are characterized by its barrier height and ideality factor parameters.

It is well known that, unless specially fabricated, a Schottky diode possesses a thin interfacial native oxide layer between the metal and the semiconductor. The existence of such an insulating layer can have a strong influence on the diode characteristics as well as the interface states [5,15,16]. Therefore, the interfacial layer and the interface states play an important role in the determination of the barrier height. Consequently, it has been concluded that the barrier height determined from the current-voltage (I-V) characteristics controlled by the interface states energy distribution in equilibrium with the semiconductor and the applied voltage under forward bias condition.

In this study, the forward and reverse bias I-V characteristics of Au/n-GaAs (MS) Schottky diodes were measured in the temperature range of 300-400 K. The temperature dependence of electrical parameters such as ideality factor, barrier height and series resistance were extracted from forward bias I-V measurements. Also, the density of interface state as a function of E_c-E_{ss} was obtained from I-V measurements.

2. Experimental Detail

The Schottky diodes have been prepared using cleaned and polished n-GaAs (as received from the manufactured) with <100> orientation and $5x10^{17}$ cm^{-3} carrier concentration. Before making the contacts, the n-GaAs wafer were dipped in $5H_2SO_4+H_2O_2+H_2O$ solution for 1.0 min to remove surface damage layer and undesirable impurities and then in H_2O+HCl solution and then followed by a rinse in de-ionized water of 18 MΩ. The wafer dried with high-purity nitrogen and inserted into the deposition chamber immediately after the etching process. Au-Ge (88% and 12%) for ohmic contacts was evaporated on the back of the wafer in a vacuum-coating unit of 10^{-6} Torr. Then low-resistance ohmic contacts were formed by thermal annealing at 450 ^oC for 3 min in flowing N_2 in a quartz tube furnace. Then, the wafer was inserted into the evaporation chamber for forming the reference Schottky contacts. The Schottky contact was formed by evaporating Au as dots with diameter of about 1 mm onto all of n-GaAs surfaces.

The current-voltage (I-V) measurements were performed by the use of a Keithley 220 programmable constant current source, a Keithley 614 electrometer in the temperature range of 300-400 K using a temperature-controlled Janes vpf-475 cryostat. The sample temperature was always monitored by using a copper-constant an thermocouple close to the sample and measured with a dmm/scanner Keithley model 199 and a Lake Shore model 321 auto-tuning temperature controllers with sensitivity better than ± 0.1 K. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. Results and discussion

According to the thermionic emission (TE) theory, the forward bias I-V characteristics of MS Schottky diodes for V≥3kT/q can simply be expressed as [1,5]

$$I = I_o \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{q(V)}{kT}\right)\right] \qquad (1)$$

where I_o is the saturation current derived from the ln(I)-V plot as the straight line intercept of the ln(I) axis at zero bias, V is the applied voltage across to rectifier contact, n is the ideality factor, T is the absolute temperature in K, q is the electronic charge and k is the Boltzmann constant. The ideality factor n is introduced to take the deviation of the experimental I-V data from the ideal thermionic model into account, and the value of ideality factor should be one for an ideal contact. The saturation current I_o is given by

$$I_o = AA^*T^2\exp\left(-\frac{q\Phi_{Bo}}{kT}\right) \qquad (2)$$

where A is the diode area, A* is the effective Richardson constant of 8.16 $Acm^{-2}K^{-2}$ for n-type GaAs and Φ_{Bo} ($kT/q\ln[AA^*T^2/I_o]$) is the zero-bias barrier height. The ideality factor is a measure of the conformity of the diode current to be pure thermionic emission, and it is calculated from the slope of the linear region of the forward bias ln(I)-V plot according to Eq.(1)

$$n = \frac{q}{kT}\frac{dV}{d\ln(I)} \qquad (3)$$

where dV/dln(I) is the slope of linear region of ln(I) vs. V plots.

Fig. 1 shows the forward and reverse bias semi-logarithmic I-V characteristics of the MS Schottky diode measured as a function of temperature. As can be seen, it shows good rectifying behavior. However, the soft or slightly non-saturating behavior was observed as a function of bias in the reverse bias branch, which may be explained in terms of the image force lowering of Schottky barrier height [17,18] and the presence of the interfacial layer between the metal and semiconductor. As can be seen in Fig. 1, the semi-logarithmic I-V plots are linear at low forward bias voltage but deviate considerably from linearity due to some factors (such as R_s, N_{ss}, etc.) at high voltages.

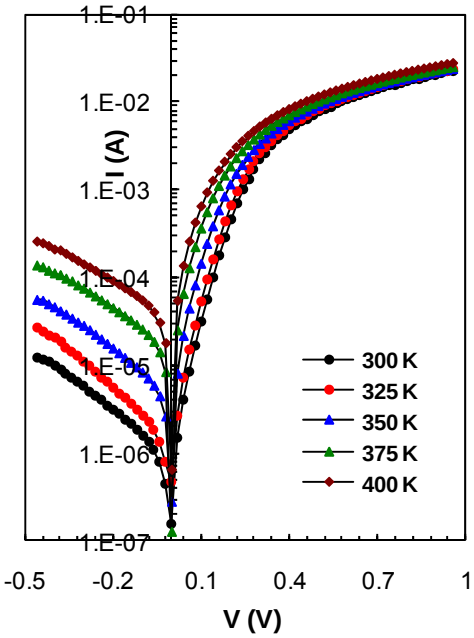

Fig. 1. Forward and reverse bias semi-logarithmic current-voltage (I-V) characteristics of the MS Schottky diode as a function of temperature.

The saturation current I_o obtained by extrapolating the linear intermediate voltage region part of linear curve to zero applied bias voltage and the experimental values of n and Φ_{Bo} determined from Eqs. (2) and (3), respectively, at each temperature are given in Fig. 2. Both parameters depend strongly on temperature. This feature can be connected either with the lateral inhomogeneity of barrier height or with the domination of the current with thermionic field emission [19]. The experimental values of n and Φ_{Bo} for the MS Schottky diode change from 1.30 and 0.57 eV at 300 K to 1.12 and 0.66 eV at 400 K, respectively. As seen in Fig. 2, the values of n increases with a decrease in temperature. Such behavior of ideality factor has been attributed to particular distribution of interface states between metal and semiconductor [13,15,20-22]. The values of barrier height have shown an unusual behavior that it increases with the increasing temperature. Such temperature dependence is an obvious disagreement with the reported negative temperature coefficient of the Schottky barrier height. As explained in the references [7,13,22-25], electrons at low temperatures are able to surmount the lower barriers since the current transport across the metal-semiconductor interface is a temperature activated process. In other words, more and more electrons have sufficient energy to overcome the higher barrier build up with the increasing temperature and bias voltage. Therefore, the current transport will be dominated by the current flowing through the patches of

lower Schottky barrier height, leading to a larger ideality factor.

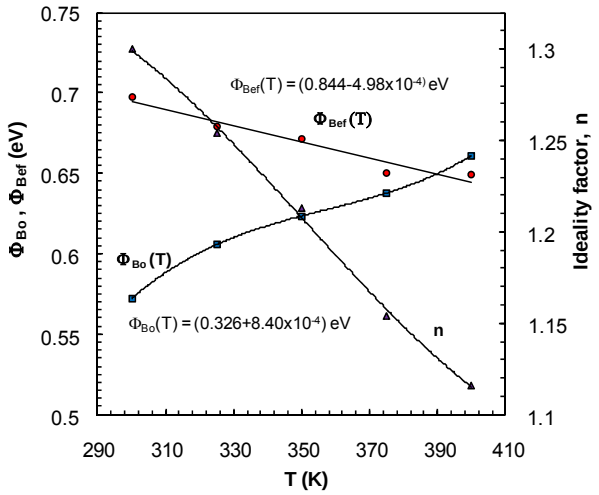

Fig. 2. Temperature dependence of ideality factor and barrier height of the MS Schottky diode.

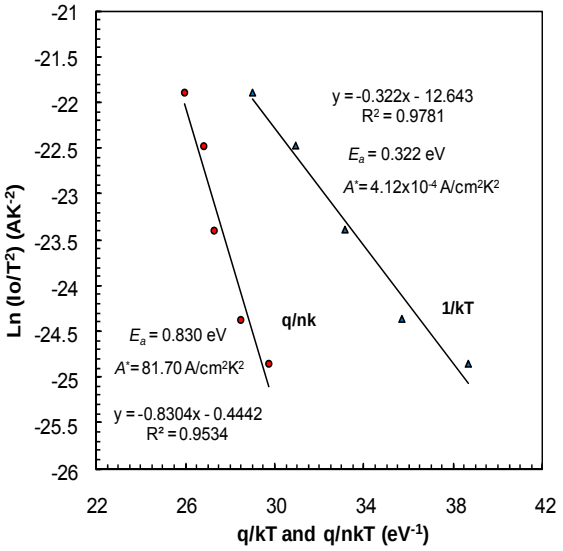

Fig. 3. The Richardson plots of ln (I_o/T^2) vs q/(kT) and q/(nkT) of the MS Schottky diode.

For the evaluation of barrier height, one may also make use of the Richardson plot of the saturation current Eq. (2) can rewritten as

$$Ln(\frac{I_o}{T^2}) = \ln(AA^*) - \frac{q\Phi_{Bo}}{kT} \tag{4}$$

As shown in Fig. 3, ln (I_o/T^2) versus q/(nkT) is more linear than ln (I_o/T^2) versus q/(kT) plot for the Au/n-GaAs Schottky diode in the measured temperature range. This behaviour of the conventional ln (I_o/T^2) versus q/(kT) is explained by the temperature dependence of the barrier height and ideality factor. Similar results also have been found by several authors [26,27]. Then, the reverse saturation current I_o can be written as

$$I_o = AA^*T^2 \exp(\frac{-q\Phi_{Bef}}{nkT}) \exp(\alpha\chi^{1/2}\delta) \tag{5}$$

The term of $\exp(\alpha\chi^{1/2}\delta)$ is commonly known as the transmission coefficient across the insulator layer. In Eq. (5), A is the diode area, A* is the effective Richardson constant, Φ_{Bef} is the flat-band barrier height, $\alpha = \left(\frac{4\pi}{h}\right)\left(2m_e^*\right)^{1/2}$ is the constant that depends on the tunneling electron effective mass m_e^*, h is the Planck's constant, δ is the thickness of the interfacial insulator layer (SiO_2) and the term of $\alpha\chi^{1/2}\delta$ is the hole tunneling factor. The corresponding effective barrier height Φ_{Bef} calculated from modified reverse saturation current expression can be expressed as;

$$\Phi_{Bef} = n\frac{kT}{q}\left[Ln(\frac{AA^*T^2}{I_o}) - \alpha\chi^{1/2}\delta\right] \tag{6}$$

It is valid only for forward bias V > 3kT/q since the contribution of reverse current has been neglected. For the interfacial insulator layer thickness δ= 27 A°, the tunneling factor ($\alpha\chi^{1/2}\delta$) was calculated as 2.3 [28]. The temperature dependent barrier height Φ_{Bef} was obtained using Eq. (6) for each temperature and listed in Table 1. The values of Φ_{Bef} are also shown in Fig. 2 as a function of temperature. As can be seen from it, Φ_{Bef} varies almost linearly with temperature as

$$\Phi_{Bef} = \Phi_{Bo}(0K) - \alpha T \tag{7}$$

where Φ_{Bo}(0 K) is the barrier height at zero temperature and α is the negative temperature coefficient of the barrier height obtained from Eq. (7) as -4.98x10^{-4} eV/K and is very close to the negative temperature coefficient of GaAs band gap(5.405x10^{-4} eV/K). Furthermore, the calculated barrier height is close to 0.844 eV and it is about the half of forbidden band gap energy (1.519 eV) of GaAs at 0 K [1]. Also, these results are in good agreement with few studies [28-30]. In addition, Richardson plot is also a useful tool for accurate calculation of tunneling factor ($\alpha\chi^{1/2}\delta$) and effective barrier height (Φ_{Bef}) by using Eqs. (4) and (5) as:

$$\ln\left(\frac{I_o}{T^2}\right) = \frac{-q\Phi_{Bef}}{nkT} - \alpha\chi^{1/2}\delta + \ln(nAA^*) \tag{8}$$

The tunneling factor was determined from the extrapolation of the plot as 2.3. The ln (I_o/T^2) versus

q/(nkT) gives a straight line with an activation energy of 0.83 eV.

The interface states for electrons or holes must not necessarily introduce energy levels in the band gap; i.e., only the density of states in the valence and conduction bands may be affected. The non-linearity of I-V characteristics of the MS Schottky diode at high bias values indicates a continuum of interface states, which are in equilibrium with the semiconductor [15]. Nevertheless, the structures exhibit excellent rectification characteristics with a relatively low leakage current density. The effective barrier height Φ_e is assumed to be bias-dependent due to the presence of an interfacial insulator layer and interface states located at the metal-semiconductor interface. The applied voltage dependence of the barrier height can be written as

$$\frac{d\Phi_e}{dV} = \beta = 1 - \frac{1}{n(V)} \tag{9}$$

where β is the voltage coefficient of the effective barrier height Φ_e and is given by [15,25,26,31]

$$\Phi_e = \Phi_{BO} + \beta V = \Phi_{BO} + (1 - \frac{1}{n(V)})V \tag{10}$$

For MS Schottky diodes having interface states N_{ss} in equilibrium with semiconductor, the ideality factor becomes greater than unity and is given by

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \tag{11}$$

This expression of voltage dependent ideality factor is identical to Eq. (18) of Card and Rhoderick [15]. For the MIS type Schottky diode with interface states entirely governed by semiconductor, the expression for the density of interface states as deduced Card and Schroder [15,32] is reduced as

$$N_{SS}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \tag{12}$$

where n(V) can be obtained from Eq.(1) by including R_s as $n(V)=q(V-IR_s)/(kTlnI/I_o)$, ε_s and ε_i are permittivity of the semiconductor and the interfacial insulator layer, respectively, δ is the thickness of the interfacial insulator layer and W_D is the width of the space charge region. For each temperature level, the values of N_{ss} were obtained from Eq.(12) by substituting δ = 27 Å [13], $\varepsilon_s = 13.1\varepsilon_o$ [1] and $\varepsilon_i = 3.9\varepsilon_o$. The thickness of interfacial insulator layer δ was obtained from high frequency C-V measurement (1 MHz) using the equation $C_{ox} = \varepsilon_i\varepsilon_o A/\delta$, where C_{ox} is the capacitance of the interfacial layer.

Communication of the interface states with the metal by tunnelling decreases with the increasing interfacial layer thickness. Thus, if there is an adequately thick interface insulator layer between metal and semiconductor, the change in occupancy of the interface states in equilibrium with the semiconductor is determined by the change in energy of the state relative to the Fermi energy in the semiconductor. Furthermore, in n-type semiconductors, the energy of interface states E_{ss} with respect to the bottom of the conduction band, E_c, at the surface of semiconductor is given as [5,26,33-35].

$$E_c - E_{ss} = q(\Phi_e - V) \tag{13}$$

The energy distribution profile of N_{ss} was obtained from Eq. (12) for each temperature level and is given in Fig. 4. As can be seen in Fig. 4, the increase in the N_{ss} from the mid-gap towards the bottom of the conduction band is very apparent. Similar results have been reported in the literature [24,36,37]. On the other hand, the mean values of N_{ss} obtained from the linear part of ln I-V plot and is given in Table 1 and their values decrease with the increasing temperature. However, as shown in Fig. 4, the energy or applied bias voltage dependent values of N_{ss} obtained from Eq. (12) increase with the increasing temperature near to bottom of conductance band and the change in N_{ss} is different from region to region. For example, near the forbidden band-gap the values of N_{ss} decrease with the increasing temperature as the mean values of N_{ss}. That is the effect of temperature on interface states is probably due to the thermal restructuring and reordering of the semiconductor-metal interface and their special distribution in forbidden band gap. In addition, the energy position near the bottom of conductance band, the calculated N_{ss} values, obtained without taking the series resistance (R_s) of the devices into account are about one order lower than N_{ss} values obtained by taking R_s values into account. Therefore, the R_s values should be taken into account in determining the interface state density distribution profiles.

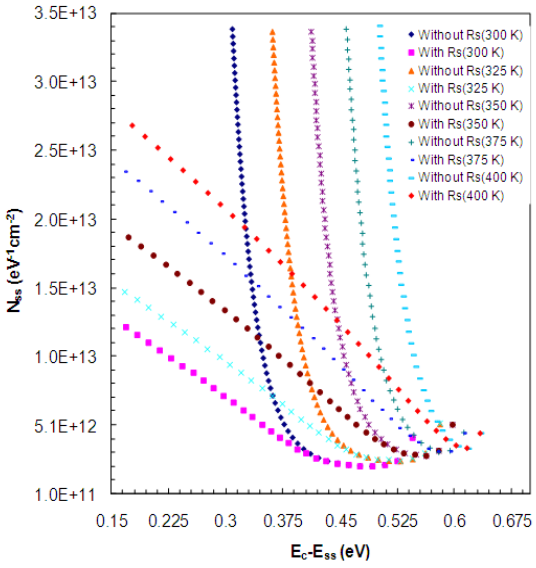

Fig. 4. The density of interface states (N_{ss}) as a function E_c-E_{ss} obtained from the forward bias I-V data at various temperatures of the MS Schottky diode.

The series resistance is a very important parameter of MS Schottky diode. The resistance of the Schottky diode is the sum total resistance value of the resistors in series and resistance in semiconductor device in the direction of current flow. Therefore, the series resistances were evaluated from the forward bias I-V data using methods developed both by Cheung [38]. The forward bias current-voltage characteristics due to thermionic emission of a Schottky contact with the series resistance can be expressed as [1,5] Cheung's functions:

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right) \tag{14}$$

and

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^{*}T^{2}}\right) = n\Phi_B + IR_s \tag{15}$$

should give a straight line for the data of downward curvature region in the forward bias I-V characteristics. In Figs. 5(a) and (b), experimental H(I) vs. I and dV/dln(I) vs. I plots are presented at different temperatures for MS Schottky diode, respectively. Eq. (14) should give straight line for the data of downward curvature region in the forward bias I-V characteristics. Thus, a plot of dV/dln(I) vs I will give R_s as the slope and n(kT/q) as the y-axis intercept. Using the n value determined from Eq. (15), a plots of H(I) vs. I will also give a straight line (as shown in Fig. 5(a)) with y-axis intercept equal to $n\Phi_B$. The slope of these plots also provides a second determination of R_s, which can be used to check the consistency of Cheung's approach. The obtained values of n will be greater than those obtained from the linear part of semi-logarithmic I-V plots. This is inevitable case, because the linear part of semi-logarithmic I-V plots corresponds low bias region. However, Cheung's functions correspond to the downward curvature in the I-V plots. Thus, only the values of n obtained from the linear part of semi-logarithmic I-V plots are given in Table 1.

As can be seen in Table 1, the values of R_s obtained from dV/dln(I)-I and H(I)-I plots are in good agreement with each other [36,39]. Also, the difference in the values of ideality factor obtained from Eqs. (3) and (14) is the result of the effect of existence of series resistance, thickness of interfacial layer and the presence of interface states [40]. The last two factors affect the Schottky barrier height, which also depends on the applied bias (throughout reloading processes of interface states).

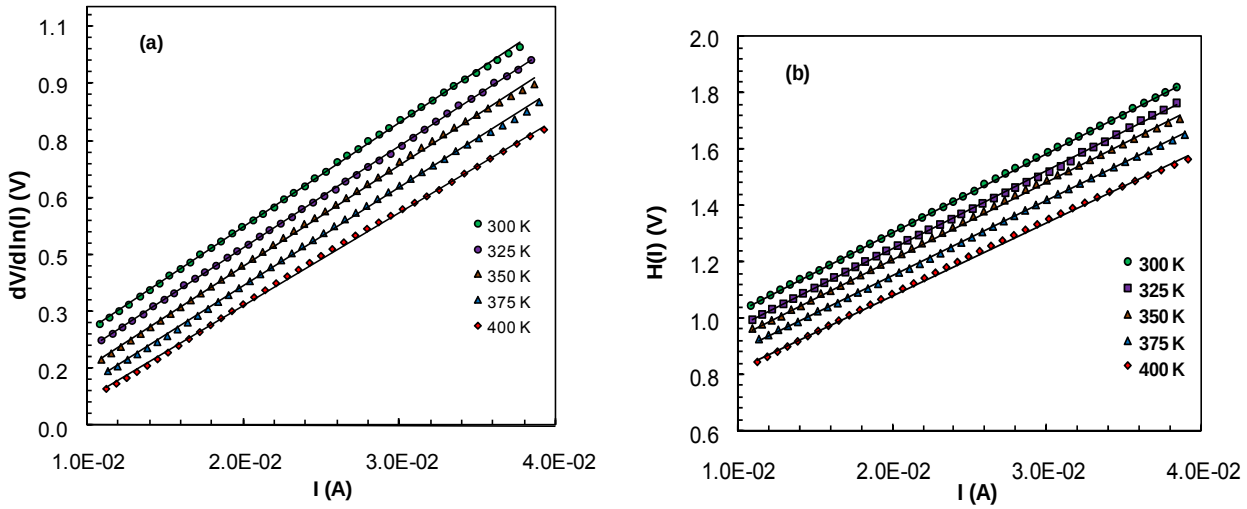

Fig. 5. The characteristics of the MS Schottky diode obtained from the forward bias I-V data at various temperatures (a) dV/dln(I) vs I and (b) H(I) vs I.

Table 1. Temperature dependent of various parameters determined from forward bias I-V characteristics of MS Schottky diode.

Temperature (K)	Io (A)	n	Φ_{Bo} (eV)	$\Phi_{Bef.}$ (eV)
300	1.44×10^{-6}	1.30	0.57	0.70
325	2.75×10^{-6}	1.25	0.61	0.68
350	8.46×10^{-6}	1.21	0.62	0.67
375	2.43×10^{-5}	1.15	0.64	0.65
400	4.93×10^{-5}	1.12	0.66	0.64

Temperature (K)	R_s(dV/d(lnI)) (Ω)	R_s(H(I)) (Ω)	N_{ss} ($eV^{-1}cm^{-2}$)
300	27.42	28.18	2.39×10^{12}
325	26.81	27.79	2.05×10^{12}
350	26.59	27.40	1.67×10^{12}
375	25.91	26.80	1.22×10^{12}
400	24.60	25.98	8.50×10^{11}

4. Conclusion

The forward and reverse bias I-V characteristics of Au/n-GaAs (MS) Schottky diodes were measured in the temperature range of 300-400 K. The barrier height (Φ_{Bo}) increases, while the ideality factor (n) decreases with the increasing temperature. It was shown that the characteristics of Au/n-GaAs Schottky diodes can be interpreted on the basis of the thermionic emission (TE) mechanism. At the same time, the density of interface states distribution profile as a function of E_c-E_{ss}, obtained from forward bias I-V measurements by taking the bias dependence of the effective barrier height into account, decreased with the increasing temperature. It was seen that a minimum and shifting appear towards the conduction band in the N_{ss} curves. This behavior of N_{ss} is probably due to the thermal restructuring and reordering of the metal-semiconductor interface. Also, the values of the series resistance (R_s) were calculated from high voltage region of the structure by using Cheung functions. It is seen that there is a good agreement between the values of the series resistance obtained from two Cheung plots.

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