# Analytical model of CNT FET current-voltage characteristics

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In this paper, one of the most promising electron devices – carbon nanotube field effect transistor (CNT FET) is investigated. At the beginning, the carbon nanotube properties are presented. The main contribution of this paper is the new analytical model of CNT FET current – voltage characteristics. Developed model describes behavior of CNT FET in very good manner and, at the same time, the model is relatively simple. Using the developed model, simulations were performed. The results obtained by using proposed model are in very good agreement with already known and published ones.

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*Keywords*: CNT FET, Current - voltage characteristics, Analytical model

## 1. Introduction

The semiconductor electron devices can be generally divided up based on the type of material used. Each material has its own advantages (and disadvantages), but some of them are not known yet and should be investigated. Implementation of new materials and structures are one of the solutions required for improving electron device characteristics. Trends in microelectronics are directed towards increasing the packaging density of chip components, thus increasing the speed of a device and simultaneously ensure the capability to perform a number complex functions [1, 2].

A very good new solution is the use of silicon carbide (SiC) [3-7]. Benefits of using carbide doped silicon, instead of standard pure silicon, for electron components, are reflected in higher operating temperatures, better heat dissipation, wide margins (in the SiC based unipolar devices in the power switching area), smaller sizes (nearly twenty times smaller than correspondingly rated silicon based devices) etc. It is important to say that SiC can be thermally oxidized to produce $SiO_2$. This makes it possible to fabricate a variety of FET (Field Effect Transistor) structures in the material.

At the other hand, heterostructure Field Effect Transistor (HFET) has better (and even new) characteristics in comparison with standard silicon FET, especially high operating speed. Like other heterostructure devices, HFET consists of very thin layers of different semiconductor materials. Differences in band gap values as well as in dopant concentrations of each layer, results with the quantum well appearance. Carriers confined in a quantum well, forming a Two-Dimensional Electron Gas (2DEG), which is usually recognized as a HFET's channel, can be controlled by the gate voltage. [8, 9].

Next step of carbide implementation in silicon based nanoelectronic components, led to the beginning of using carbon nanotubes (CNTs), as the material for the realization of FET's active area. Introducing carbon nanotubes into the silicon transistor, some kind of a heterostructure device (in fact heterostructure active area) can be recognized.

More than a decade, nanomaterials (nowadays including carbon nanotubes) have been investigated in physics and electronics. Their further development should obtain commercial applications.

Because of very good electrical, thermal and mechanical characteristics and wide range of potential applications, carbon nanotubes attract much attention today.

## 2. Carbon nanotubes

CNTs are cylindrical molecules formed from hexagonal structures of hybridized carbon atoms. They belong to the family of fullerenes, allotropic forms of carbon [10, 11]. CNTs are described as hollow cylinders arising from rolling individual or multiple layers of graphene in a joint less cylinders (Fig. 1).

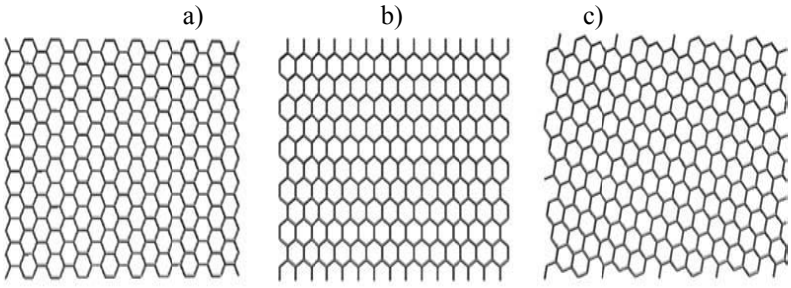


*Fig. 1. Graphene sheets that shows the orientation of graphene hexagons a) chair b) zig-zag, c) chiral*

There are two types of nanotubes: single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs), which are built of few concentric cylinders of SWCNTs (Figure 2). MWCNTs are less stable nanostructures with common structural defects. Thus SWCNTs are more suitable for practical applications.

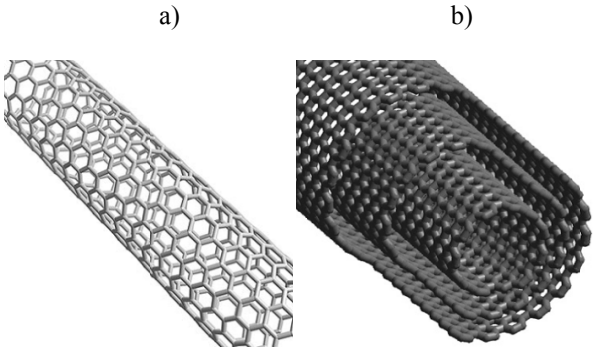


*Fig. 2. Structure of carbon nanotubes: a) SWCNT, b) MWCNT*

Control of high quality grown CNTs is very important. Cleanliness, defects, diameter and length of the nanotube directly affects its characteristics. Production of high quality CNTs remains a problem that has to be solved. But, some special techniques have been developed to produce nanotubes. CNTs obtained by different techniques have different physical properties. Quality, quantity and type of nanotubes depend on the method used for their synthesis.

## 3. CNT FET

Carbon nanotubes have a band gap that scales inversely with a tube diameter d, Eg≈0.84/d[eV/ nm] [12]. Conduction through the nanotubes is dependent on the exact position of the Fermi level with respect to the band edges.

The conductivity dependence on the potential in CNT can be used to make a device that will operate like a switch. It would conduct current when the potential on capacitively coupled gate moves the Fermi level in valence band or conductive zone, and behave as an insulator when Fermi level is in the band gap. Such device is well known in semiconductor industry as a transistor.

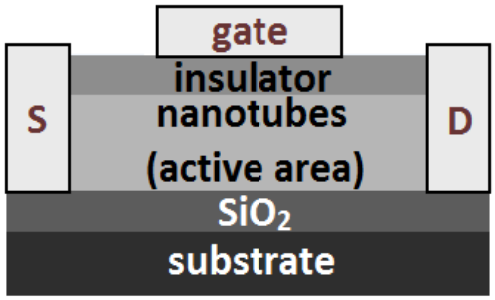


*Fig. 3. CNT FET cross section*

In order to improve the characteristics of standard Si transistor, active silicon area can be replaced with CNT. A few of implemented nanotubes that are connected, at the same time, with source and drain area would form transistor's channel. Cross section view of a CNT FET is shown in figure 3. The first carbon nanotube based field effect transistors were demonstrated in 1998. at the University of Delft and at IBM.

## 4. Modeling of current-voltage characteristics of CNT FETs

Due to the existence of electric field (occurs as a result of voltages applied to the device electrodes), as well as the differences in the concentration of carriers within the electron device, electric current is obtained. For modeling mentioned phenomena, drift-diffusion model is most commonly used. New models of microelectronic devices, which are accurate and relatively simple, can be developed by using this approach [4],[6],[13-16]. Same approach can be applied to nanoelectronic devices, in compliance with appropriate specificities.

To merge simplicity and accuracy in modeling of current-voltage characteristics of CNT FETs, an analogy between classic and CNT FETs can be established. In this case, layer of nanotubes, which forms the active area, is observed as a conductive channel. Width of the formed channel is W and length is L. Starting from the well known equation for the current density of electrons $J_n$:

$$J_n = Q_e \cdot n \cdot \mu_n \cdot E + Q_e \cdot D_n \cdot \frac{dn}{dx} \qquad (1)$$

where $Q_e$ is the electron charge, n is the concentration of electrons, $\mu_n$ is the electron mobility, E is the electric field, $D_n$ is the constatnt and x is the direction of the current flow (the lateral direction in a plain transistor), the expression for the elementary drain current of CNT FET can be written similarly as in [3],[4],[8]:

$$dI_D = Q \cdot n\left(x,y,E_{CNT}(x,y),T\right) \cdot \mu_{CNT}\left(x,y,E_{CNT}(x,y),T\right) \cdot \cdot E_{CNT}(x,y) \cdot W \cdot dx + Q_e \cdot D_n \cdot \frac{\partial n_{CNT}\left(x,y,E_{CNT}(x,y),T\right)}{\partial x} \quad (2)$$

In equation (2) $E_{CNT}$ is the electric field in CNT (channel), $\mu_{CNT}$ is the carriers mobility in CNT, T is the temperature and y is the vertical coordinate.

Total drain current can be determined by integrating over the vertical axis:

$$I_D = Q_e \cdot \frac{dV(x)}{dx} \cdot \cdot \int_0^{y_{max}} \left( \begin{array}{l} n\left(x,y,E_{CNT}(x,y),T\right) \cdot \\ \cdot \mu_{CNT}\left(x,y,E_{CNT}(x,y),T\right) \cdot W \end{array} \right) \cdot dy + + Q_e \cdot D_n \cdot \int_0^{y_{max}} \frac{\partial n\left(x,y,E_{CNT}(x,y),T\right)}{\partial x} \cdot dy \quad (3)$$

In equation (3), well known relation between the field E and potential V is used: $E_x = -dV/dx$. It is assumed that the variations of the electric field over the vertical axis, within the channel, are very small. It is a realistic assumption in microelectronic, especially nanoelectronic devices domain.

Depending on the model for carriers mobility μ(x, y, E, T) and carriers concentration n(x, y, E, T), integral of a certain level of complexity is obtained. Assuming that mobility and carriers concentration in all parts of active area has the same averaged value, equation (3) can easily be solved:

$$I_D = Q_e \cdot n\left(E_{CNT}(x),T\right) \cdot \cdot \mu_{CNT}\left(E_{CNT}(x),T\right) \cdot \frac{dV}{dx} \cdot W \quad (4)$$

or:

$$I_D \cdot dx = Q_e \cdot n\left(E_{CNT}(x),T\right) \cdot \cdot \mu_{CNT}\left(E_{CNT}(x),T\right) \cdot dV \cdot W \quad (5)$$

Integrating (5) along the channel, it is obtained:

$$I_D \cdot L = Q_e \cdot n\left(E_{CNTaver},T\right) \cdot \cdot \mu_{CNT}\left(E_{CNTaver},T\right) \cdot W \cdot \int_{V_S}^{V_D} dV \quad (6)$$

In equation (6) L is the length of the CNT (channel), $E_{CNTaver}$ is the average electric field in CNT's channel, $V_S$ – source potential and $V_D$ – drain potential. Using elementary transformations, similar like in [6], the expression for drain current can be determined.

In linear mode, drain current is:

$$I_D = \frac{\mu_{CNT}\left(E_{CNTaver},T\right) \cdot C_{ox} \cdot W}{L} \cdot \cdot \left( V_{GS} - V_{Th} - \frac{V_{DS}}{2} \right) \cdot V_{DS} \quad (7)$$

In saturation regime, drain current is:

$$I_D = \frac{1}{2} \frac{\mu_{CNT}\left(E_{CNTaver},T\right) \cdot C_{ox} \cdot W}{L} \cdot \left(V_{GS} - V_{Th}\right)^2 \quad (8)$$

In expressions (7) and (8) $V_{GS}$ is the gate to source voltage, $V_{th}$ - threshold voltage, $V_{DS}$ – drain to source voltage and $C_{ox}$ is the oxide capacitance per unit area.

Among other factors, temperature and electric field are significantly affecting on charge carriers mobility. Mobility of carriers can be described by well known expression:

$$\mu(T) = \mu(T_a) \cdot \left(\frac{T_a}{T}\right)^{\alpha} \quad (9)$$

In equation (9) $T_a$ is the ambient temperature, T - temperature of the active area of CNT FET and $\alpha$=1.5.

According to the results of investigations, for the carbon and SiC based MOSFET (operating in the linear regime), as well as for the short channel transistor and the transistor with low drain to source voltages, the carrier mobility dependence on electric field is given by [5]:

$$\mu(E) = \frac{\mu_0}{1 + \left| \frac{E}{E_{crit}} \right|^{\lambda}} \quad (10)$$

where $\mu_0$ is the mobility for the low intensity electric fields, E is the electric field in a channel, $E_{crit}$ is the critical value of the electric field and λ is the constant witch is different for electrons and for holes (for electrons: λ=1.6, for holes: λ=1.1).

Considering only the vertical component of the electric field $E_{CNTy}$, which significantly affects the degradation of carriers mobility value, equation (10) can be rewritten as:

$$\mu_{CNT}'\left(E_{CNT}\right) = \frac{\mu_0}{1 + \left| \frac{E_{CNTy}}{E_{ycrit}} \right|^{\lambda}} \quad (11)$$

In equation (11) $E_{ycrit}$ is the critical value of the electric field vertical component (in SiC based electron components, for electrons: $E_{ycrit}$=0.6MV/cm and for holes

$E_{ycrit}$=0.7MV/cm). Value of the vertical electric field can be calculated as the mean value of vertical fiedls on surfaces with either side of the CNT channel.

Bearing in mind that carriers transport through CNTs, thanks to their structure, is almost strictly in lateral direction, mobility degradation caused by vertical electric field is reduced. This effect can be modeled by introducing correction coefficient ξ which depends on the orientation of graphene hexagons. Improved carriers mobility model is:

$$\mu_{CNT}\left(E_{CNT}\right)=\frac{\mu_0}{1+\left|\frac{\xi\cdot E_{CNTy}}{E_{ycrit}}\right|^{\lambda}} \tag{12}$$

For the low values of electric field, temperature has the dominant influence on the carriers mobility:

$$\mu_0=\mu_{CNT}(T)=\mu(T_a)\cdot(\frac{T_a}{T})^{\alpha} \tag{13}$$

By combining the models presented by expressions (12) and (13), analytical model for the carriers mobility gets final:

$$\mu_{CNT}\left(E_{CNT},T\right)=\frac{\mu\left(T_a\right)\cdot\left(\frac{T_a}{T}\right)^{\alpha}}{1+\left|\frac{\xi\cdot E_{CNTy}}{E_{ycrit}}\right|^{\lambda}} \tag{14}$$

Introducing (14) into (7) and (8), final CNT FET current-voltage model is obtained:

- in linear operating regime

$$I_D=\frac{\frac{\mu\left(T_a\right)\cdot\left(\frac{T_a}{T}\right)^{\alpha}}{1+\left|\frac{\xi\cdot E_{CNTy}}{E_{ycrit}}\right|^{\lambda}}\cdot C_{ox}\cdot W}{L}\cdot \left(V_{GS}-V_{Th}-\frac{V_{DS}}{2}\right)\cdot V_{DS} \tag{14}$$

- in saturation regime:

$$I_D=\frac{1}{2}\frac{\frac{\mu\left(T_a\right)\cdot\left(\frac{T_a}{T}\right)^{\alpha}}{1+\left|\frac{\xi\cdot E_{CNTy}}{E_{ycrit}}\right|^{\lambda}}\cdot C_{ox}\cdot W}{L}\cdot\left(V_{GS}-V_{Th}\right)^2 \tag{15}$$

## 5. Results and discussion

Using the proposed analytical models (14) and (15), simulations were performed. For some parameters, following values were used: capacitance per unit area $C_{ox}$=200[aF/μm$^2$], channel width W=40[nm]-70[nm], channel length L=30[nm]-50[nm], threshold voltage at room temperature $V_{th}$=0.3[V], T=320[K], $T_a$=300[K], μ($T_a$)=2000[cm$^2$/Vs], ξ=0.8, λ=1.6.

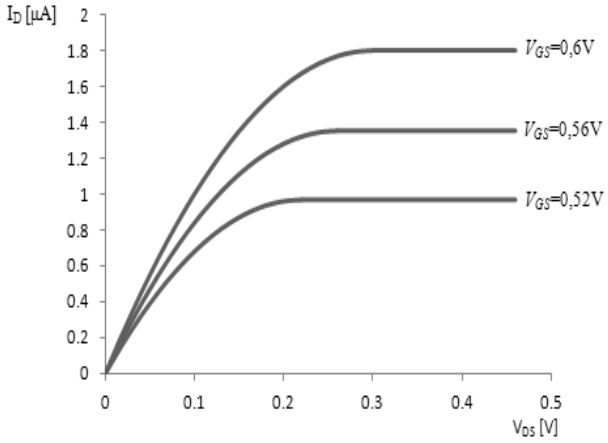


*Fig. 4. Drain current $I_D$ versus drain to source voltage $V_{DS}$, for various values of gate to source voltages $V_{GS}$ (L=30[nm], W=40[nm])*

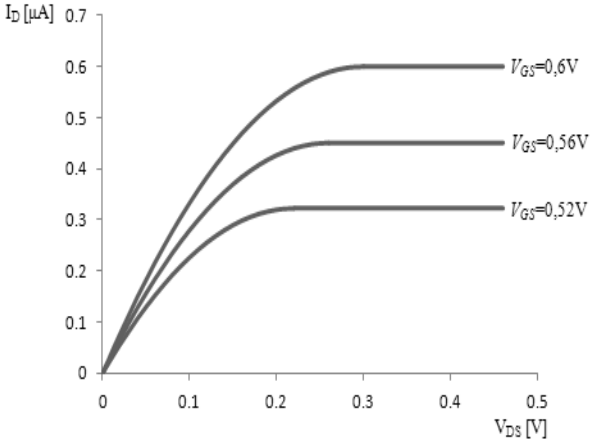


*Fig. 5. Drain current $I_D$ versus drain to source voltage $V_{DS}$, for various values of gate to source voltages $V_{GS}$ (L=50[nm], W=40[nm]).*

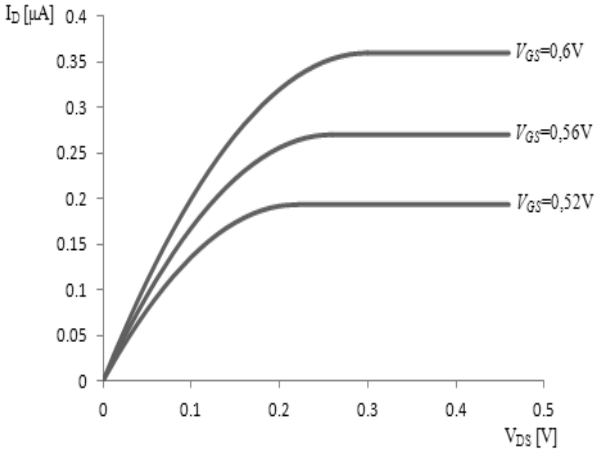


*Fig. 6. Drain current $I_D$ versus drain to source voltage $V_{DS}$, for various values of gate to source voltages $V_{GS}$ (L=70[nm], W=40[nm]).*

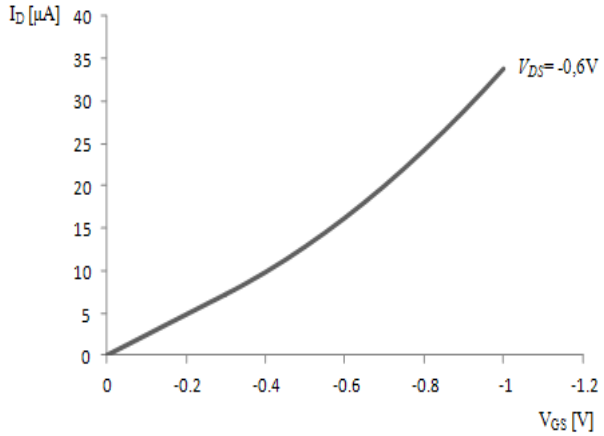


*Fig. 7. Drain current $I_D$ versus gate to source voltage $V_{GS}$ ($V_{DS}$=-0,6V, L=30nm, W=40nm).*

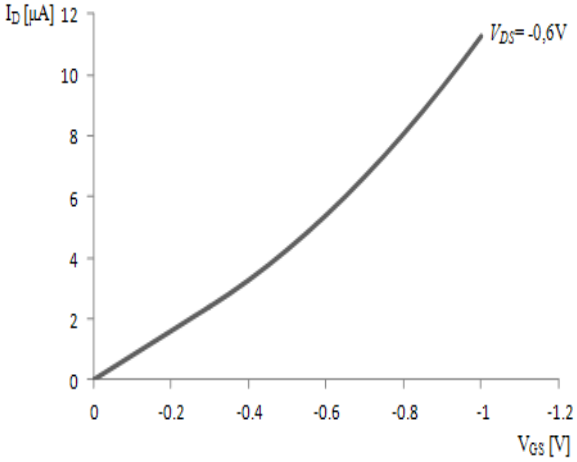


*Fig. 8. Drain current $I_D$ versus gate to source voltage $V_{GS}$ ($V_{DS}$=-0,6V, L=50nm, W=40nm).*

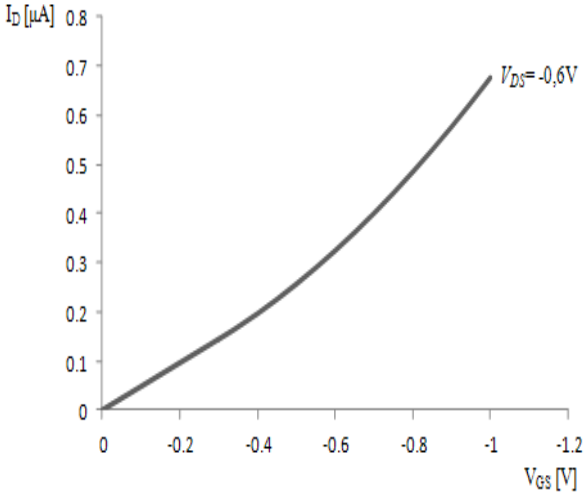


*Fig. 9. Drain current $I_D$ versus gate to source voltage $V_{GS}$ ($V_{DS}$=-0,6V, L=70nm, W=40nm).*

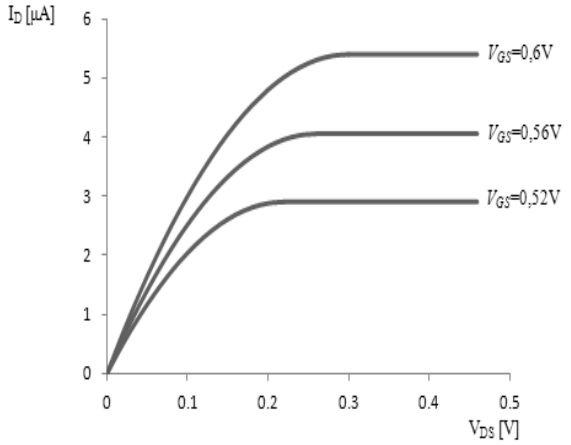


*Fig. 10. Drain current $I_D$ versus drain to source voltage $V_{DS}$, for various values of gate to source voltages $V_{GS}$, (L=30nm, W=50nm).*

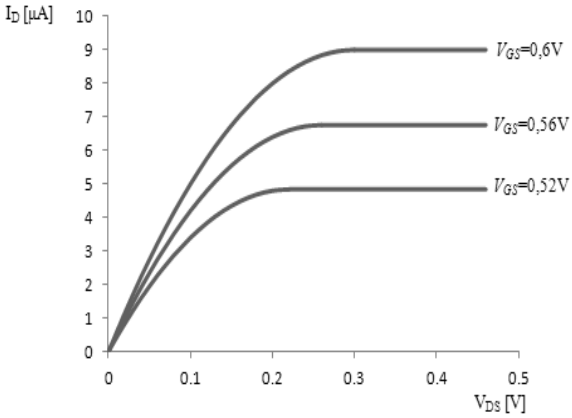


*Fig. 11. Drain current $I_D$ versus drain to source voltage $V_{DS}$, for various values of gate to source voltages $V_{GS}$ (L=30nm, W=60nm)*

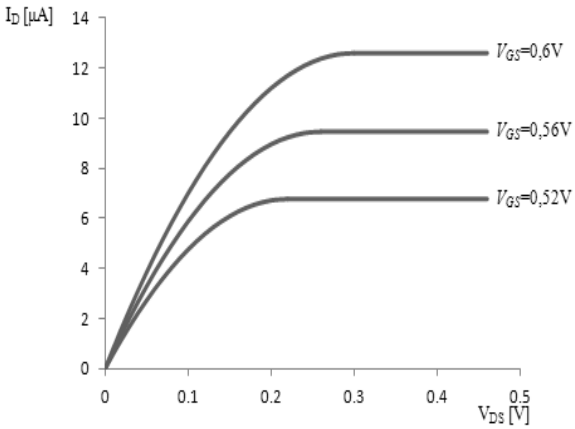


*Fig. 12. Drain current $I_D$ versus drain to source voltage $V_{DS}$, for various values of gate to source voltages $V_{GS}$ (L=30nm, W=70nm).*

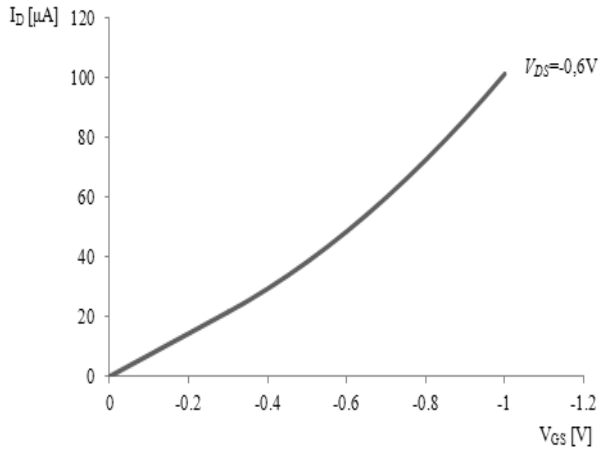


*Fig. 13. Drain current $I_D$ versus gate to source voltage $V_{GS}$ ($V_{DS}$=-0,6V, L=30nm, W=50nm)*

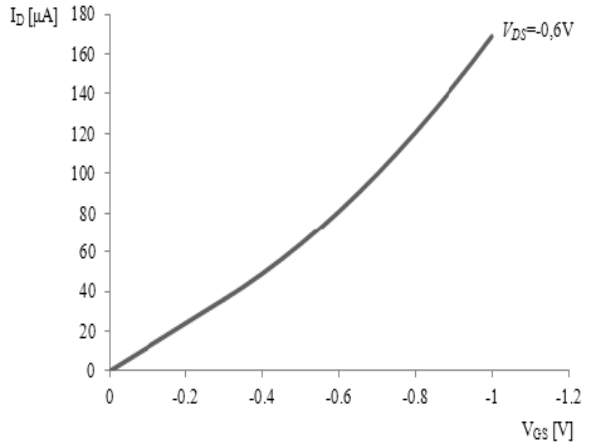


*Fig. 14. Drain current $I_D$ versus gate to source voltage $V_{GS}$ ($V_{DS}$=-0,6V, L=30nm, W=60nm)*

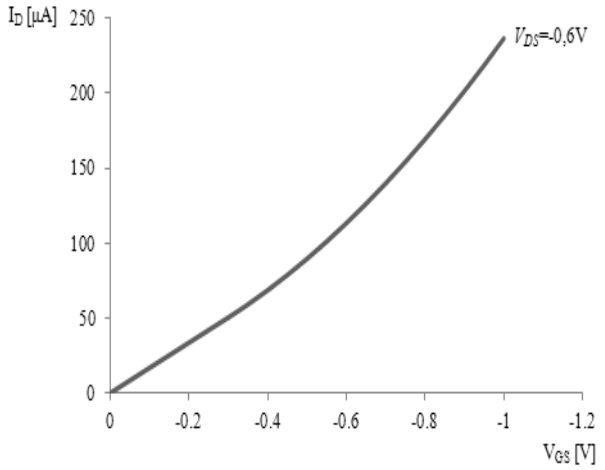


*Fig. 15. Drain current $I_D$ versus gate to source voltage $V_{GS}$ ($V_{DS}$=-0,6V, L=30nm, W=70nm)*

In Figs. 4., 5. and 6., as well as in Figs. 10., 11. and 12., dependences of the drain current $I_D$ on the drain to source voltage $V_{DS}$, where gate to source voltage $V_{GS}$ is parameter, are shown, but firstly for different channel lengths L, and secondly for different channel widths W.

In Figs. 7., 8. and 9., as well as in Figs. 13., 14. and 15., dependences of the drain current $I_D$ on the gate to source voltage $V_{GS}$, where gate to source voltage $V_{GS}$ is fixed, are shown, firstly for different channel lengths L, and secondly for different channel widths W.

Obtained curves shapes are expected and well known. Linear operating and saturation operating regime segments can be easily recognized from the figures.

In linear operating regime, CNT FET's current increases with drain to source voltage as a square function, for fixed gate to source voltage. In saturation regime, drain current is constant (the same is usually assumed and proved for the standard set of data). Drain current increases also when gate to source voltage, which is parameter, increases.

CNT FET's current increases with gate to source voltage as a square function, for fixed drain to source voltage.

Nanotubes dimensions have a significant impact on their characteristics. Thus, geometrical parameters, which are determined by nanotubes which form channel, also strongly affects current-voltage characteristics. These effects must be taken into account. The longer channel length L results in decreasing of transistor current (e.g. for the channel length L=50[nm] drain current in saturation operating regime is $I_D$=0.6[μA], and for the channel length L=70[nm] drain current in saturation operating regime is $I_D$=0.6[μA] (gate to source voltage $V_{GS}$=0.6[V]) – figures 5. and 6.). The longer channel width W results in increasing of transistor current (e.g. for the channel width W=60[nm] drain current in saturation operating regime is $I_D$=9[μA], and for the channel width W=70[nm] drain current in saturation operating regime is $I_D$=12[μA] (gate to source voltage $V_{GS}$=0.6[V]) – figures 11. and 12.).

Presented graphics indicate that voltage and current values correspond to the values known from the literature.

## 6. Conclusion

The paper first exposes advantages of using carbon nanotubes and possibility of their application in most modern electronic devices – FETs in which active silicon area can be replaced with CNT.

In central part of this paper, the new analytical model of CNT FET current-voltage characteristics is developed. Starting from the model for elementary drain current, and taking into account special channel structure which is strongly different in lateral in comparsion with vertical direction, current-voltage dependences are obtained. Special attention is paid to the dependences of carriers mobility on applied electric field and temperature. The new correction coeffitient, which describes CNT structure impact on carriers propagation through the CNT FET's channel, is introduced. Proposed model for carriers mobility is based on the conclusion that for the low values of electric field, temperature has the dominant influence on the mobility and, on the other hand, for high electric fields, such fields play the main role. Developed carriers

mobility model is incorporated into proposed CNT FET current-voltage characteristics model.

Using the proposed models, simulations were performed. The results obtained by using developed models are in very good agreement with already known and published ones.

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