Annealing effect on the electrical properties of HfO_2 based Schottky barrier diodes

SEDA BENGI, M. MAHIR BÜLBÜL*
Physics Department, Faculty of Sciences, Gazi University, 06500, Teknikokullar, Ankara, Turkey

The effect of post-annealing on the current-voltage (*I-V*), capacitance-voltage (*C-V*) and conductance-voltage (*G/ω-V*) characteristics of metal-insulator-semiconductor Al/HfO_2/p-Si (100) diode grown by Magnetron sputtering has been investigated at room temperature. The results indicate that the post-annealed sample for 2 h at 700 ^{0}C has a lower leakage current and interface states compared with the as-deposited sample. From the *I-V*, *C-V* and *G/ω-V* measurements, we also calculated the main diode parameters, including ideality factor *n*, barrier height Φ_B, interface states N_{ss}, and series resistance R_s. It was found that the annealing process has strongly influenced the electrical properties of this sample.

(Received July 24, 2012; accepted March 13, 2014)

Keywords: HfO_2, Annealing effect, Interface states, Insulator layer

1. Introduction

High dielectric constant (high-k) gate dielectric materials such as TiO_2, ZrO_2 and HfO_2 have been suggested as possible candidates to reduce leakage current and increase capacitance density [1-5]. Among them, HfO_2 appears as the best candidate for the gate oxide dielectric layer, since it has many advantages such as a high dielectric constant ($\approx$25) [6], a large band gap (5.68 eV) [7], high breakdown electric field ($\approx$ 8.5 MV/cm) [8] and thermal stability in contact with silicon substrates. However, one of the main drawbacks of this promising material is a low crystallization temperature, which promotes crystal boundaries to act as leakage paths and impurity getters during processing. It has well known that the physical and electrical properties of MIS structure strongly depend on the preparation conditions of the surface and the formation of the interfacial layer [9-17]. To grow high quality hafnium oxide on silicon substrate, a number of deposition techniques have been used [18], such as MOCVD [19], CVD [20], ALD [21], MBE [22] and sputtering [23]. The annealing process can affect the interface properties of the film, which plays a crucial role in the electrical properties of the devices [24-27].

In this work, we have investigated the post-annealing effect on the current-voltage (*I-V*), capacitance-voltage (*C-V*) and conductance-voltage (*G/ω-V*) properties of Al/HfO_2/p-Si (100) diodes grown by Magnetron sputtering. Using the results of *I-V*, *C-V* and *G/ω-V* measurements, we also obtained the main diode parameters of this device at room temperature.

2. Experimental detail

HfO_2 high-k thin film was fabricated on p-type Si (100) substrate with 2″(inch) in diameter, thickness of 300 μm and resistivity of 1-10 Ω.cm, using RF magnetron sputtering system. Prior to the deposition of the HfO_2 thin films, the Si substrate was cleaned using $CHClCCl_2$, CH_3COCH_3, and CH_3OH organic solvents, respectively. After the organic cleaning step, the Si substrate was etched in a solution of $6HNO_3$:1HF:$35H_2O$ to remove the native oxide layer and finally rinsed in de-ionized water (resistivity of 18 MΩ.cm). Latter to cleaning and etching steps, the Si substrate was mounted on the stainless steel optically heated sputtering holder and loaded in the RF magnetron sputtering system. Before the deposition of the HfO_2, Si substrate and HfO_2 target were sputter-cleaned in pure argon ambient (10^{-5} Torr pressure) with power of 20 W and 30 W for about 1 minute to ensure the removal of any residual impurities, respectively. HfO_2 thin film was deposited on Si substrate from high purity (99.95%) HfO_2 target. The flow of reactive gas Ar was maintained at 50 sccm with mass flow controller. The pressure was set to 40 mTorr and it was kept constant during the whole deposition. Thermal annealing process was carried out in the oxidation furnace for 2 h at 700 ^{0}C.

The ohmic contacts were formed by deposition of Au-Ge (100 nm) alloy and Au(50 nm) metal at 380 ^{0}C, under $3.27x10^{-7}$ mbar vacuum and the sample was annealed at 350 ^{0}C to achieve good ohmic contact behavior. After then, the dot shaped rectifier front contacts with 1 mm diameter and 110 nm thickness were formed by deposition of high purity Al (99.999%) at 80 ^{0}C.

The current-voltage (*I-V*) measurements of Al/HfO_2/p-Si structures were performed at room temperature using Keithley 2400 source-meter and micro computer through an IEEE-488 AC/DC converter card. Additionally, capacitance-voltage (*C-V*) and conductance-voltage (*G/ω-V*) measurements were performed using HP 4192 A LF impedance analyzer (5 Hz to 13 MHz) at 1 MHz.

3. Results and discussion

The current through a Schottky barrier diode (SBD) at a forward bias *V*, according to thermionic emission (TE) theory, is given by [28]

$$I = I_o \exp\left(\frac{qV - IR_s}{nkT}\right)\left[1 - \exp\left(\frac{-q(V - IR_s)}{kT}\right)\right] \quad (1)$$

where *V*, *n*, *q*, IR_S and *T* are the applied bias voltage, the ideality factor, the electronic charge, the voltage drop across series resistance of SBD, the temperature in Kelvin, respectively. I_o is the reverse saturation current extracted from the straight line intercept of ln*I*-*V* plot at zero bias and is given by

$$I_o = AA^* T^2 \exp\left(-\frac{q\Phi_{B0}}{kT}\right) \quad (2)$$

where q is the electronic charge, A^* is the effective Richardson constant and equals to 32 A cm^{-2} K^{-2} for *p*-type Si, *A* is the effective diode area, k is the Boltzmann constant, *T* is the absolute temperature, Φ_{B0} is the zero bias barrier height and *n* is the ideality factor. The ideality factor is calculated from the slope of the linear region of the forward bias *ln(I)*-*V* plot and can be written as from Eq.(1)

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \quad (3a)$$

Also, the voltage dependent ideality factor can be written from Eq.(1) as:

$$n(V) = \frac{qV}{kT\ln(I / I_0)} \quad (3b)$$

The zero-bias barrier height Φ_{B0} *(=* $\Phi_{B(I\text{-}V)}$*)* is determined from the extrapolated I_o and is given by the relation:

$$\Phi_{B0} = \frac{kT}{q}\ln\left[\frac{AA^* T^2}{I_0}\right] \quad (4)$$

Fig. 1 shows the forward and reverse bias semi-log *lnI*-*V* characteristic for the as-deposited and post annealed Al/HfO_2/p-Si (100) Schottky diodes at room temperature. From the Fig. 1, it is apparent that Al/HfO_2/p-Si (100) diodes has good rectifying properties, and the leakage current of the post annealed diode is lower more than one order of magnitude than that of the as–deposited diode at a gate voltage of 1 V, the leakage current has a saturation value of 6×10^{-8} A for the annealed diode and 1×10^{-6} A for the as-deposited diode. Tan et al. [24] shown that the improved densification of HfO_2 thin films and the formation of $HfSi_xO_y$ interfacial layer after annealing are responsible for the reduced leakage current. However, the continuous increase of annealing temperature will lead to the crystallization on the amorphous film, in which the grain boundaries serve as a high-leakage current path [29-30]. The saturation of the leakage current can mainly be attributed to the compositions of electrons which are generated from interface states, and the partial electrons are trapped and de-trapped in the HfO_2 layer.

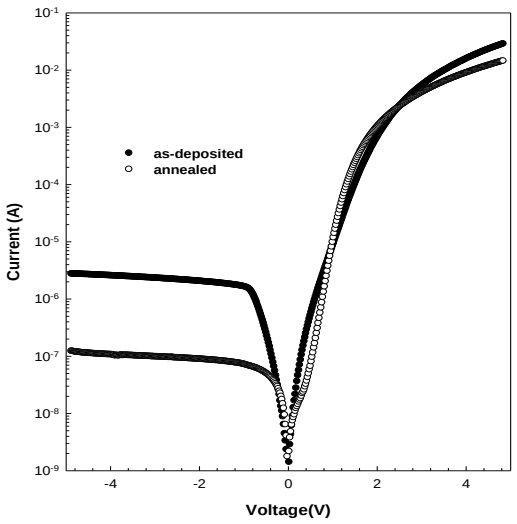

Fig. 1. Forward and reverse bias current-valtage (I-V) characteristics of the Al/HfO_2/p-Si (100) Schottky diodes."●" represents the data of the as-deposited sample and "○" represents the sample annealed at 700 ^{0}C.

The experimental values of *n* and Φ_{B0} for the as-deposited and the annealed Al/HfO_2/p-Si diodes were determined from Eq.(3a) and (4), respectively, at room temperature. The values of *n* and Φ_{B0} for the Al/HfO_2/p-Si (100) Schottky diodes are 4.43 and 0.743 eV for the as-deposited and 4.03 and 0.811 eV for the annealed diode, respectively. The decrease in the value of ideality factor can be ascribed to the occurrence of the more ordered interfacial layer after the annealing process. On the other hand, after annealing, the higher Schottky barrier height may be attributed to a comparatively homogeneous barrier height, preventing the transport of the electron through patches of the lower barrier height as in the case of inhomogenous barrier height at low temperature. Considering the temperature effect on barrier height, as explained in Tung [31] and Sullivan et al. [32], since current transport across the MS interface is a temperature activated process, electrons at low temperatures are able to surmount the lower barriers and therefore current transport will be dominated by current flowing through patches of the lower Schottky barrier height (SBH) and a larger ideality factor. As the temperature increases, more and more electrons have sufficient energy to surmount the higher barrier. As a result, the dominant barrier height will increase with the temperature and bias voltage [33].

The value of series resistance, R_s, was calculated from the forward bias *I*-*V* data using the method of Cheung and

Cheung [34]. From Eq.(1), the following functions can be rewritten as:

$$\frac{dV}{d(\ln I)} = n\left(\frac{kT}{q}\right) + IR_s \tag{5a}$$

$$H(I) = V + n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = n\Phi_{Bo} + IR_s \tag{5b}$$

Here, in Eq.(5a) and Eq. (5a) the term IR_s is the voltage drop across the series resistance of the Al/HfO_2/p-Si(100) diode. In Fig. 2a and 2b the values of *dV/d(lnI)-I* and *H(I)-I* are plotted for the as-deposited and annealed diodes, respectively. The plots, *dV/d(lnI)-I* and *H(I)-I*, will be linear in forward bias semi-logarihmic *I-V* characteristics and the slopes of plots are used to determine the R_s. The values of R_s were found to be 44.938 Ω and 57.767 Ω for the as deposited Al/HfO_2/p-Si(100) diode, and 117.65 Ω and 148.59 Ω for annealed diode.

The non-linearity of *lnI-V* characteristics at high bias values indicates a continuum of interface states in equilibrium with semiconductor [35]. Thus, the density distribution of the interface states N_{ss} can be determined from the forward bias *I–V* characteristics. The effective barrier height Φ_e is given as:

$$\Phi_e = \Phi_{B0} + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \tag{6}$$

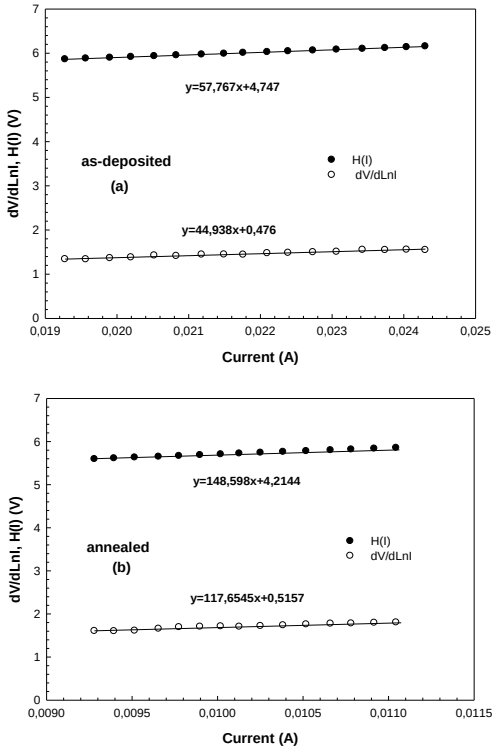

Fig. 2. The plots of dV/dLnI and H(I) vs. current of Al/HfO_2/p-Si(100) Schottky diode (a) as deposited and (b) annealed at 700 ^{0}C.

by considering the applied voltage dependence of Φ_e due to the presence of an interfacial insulator layer HfO_2 and interface states located at the HfO_2/p-Si(100) interface. For Al/HfO_2/p-Si(100) diodes, the density of interface states proposed by Card and Rhoderick can be simplified and given as [36]:

$$N_{SS}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_S}{W_D}\right] \tag{7}$$

where the permittivity of semiconductor is $\varepsilon_s = 11.8\varepsilon_o$, permittivity of insulator layer is $\varepsilon_i = 25\varepsilon_o$ [6,37-38] while ε_o (=8.85x10^{-14} F/cm) is the permittivity of free space and W_D is the width of the space charge region.

Fig. 3 depicts the density of interface states N_{ss} as a function of E_{ss}-E_v deduced from the *I-V* data at room temperature. As can be seen from Fig. 3, an exponential rise of interface state density from midgap towards the top of valance band is very apparent. We have observed then that the values of N_{ss} for the annealed diode is slightly lower compared to the as-deposited diode close to the valance band. The lower value of N_{ss} can be attributed to the occurrence of the more ordered interfacial layer after the annealing process.

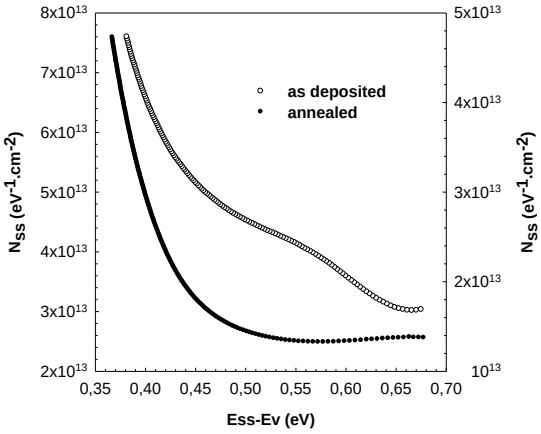

Fig. 3. Density of interface states N_{SS} as a function of E_{SS}-E_V deduced from the I-V data at room temperature.

The forward and reverse-bias capacitance-voltage measurements were carried out for the Al/HfO_2/*p*-Si (100) Schottky diodes at enough high frequency (1 MHz) by using HP 4192A LF impedance analyzer at room temperature. In Schottky diodes, the depletion layer capacitance can be expressed as [39]:

$$C^{-2} = \frac{2(V_R + V_0)}{q\varepsilon_s\varepsilon_0 A^2 N_A} \tag{8}$$

where A is the area of diode, V_R is the reverse-bias voltage, V_0 is the built-in voltage at zero-bias and N_A is the acceptor concentration of Si. The diffusion potential or built-in

potential is determined from the extrapolation of the C^{-2} vs V plot to the V axis. From the C-V characteristics, the barrier height $\Phi_B(C\text{-}V)$ is calculated using the voltage intercept V_0 of the C^{-2} vs V plot (Fig. 5) by the relation:

$$\Phi_B(C-V)=\left(V_0+\frac{kT}{q}\right)+E_F-\Delta\Phi_B=V_D+E_F-\Delta\Phi_B \quad (9)$$

where E_F is the potential difference between the Fermi level and the bottom of valance band in the neutral region of p-Si and $\Delta\Phi_B$ is the image force barrier lowering and given by [39].

$$\Delta\Phi_B=\left(\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}\right)^{1/2} \quad (10)$$

where E_m is the maximum electric field and given by

$$E_m=\left[\frac{2qN_AV_0}{\varepsilon_s\varepsilon_0}\right]^{1/2} \quad (11)$$

The experimental carrier doping density N_A values were determined from the slope of the linear part of C^{-2} vs V curves (Fig. 6) at room temperature. The values of E_F were obtained from

$$E_F=\frac{kT}{q}\ln\left(\frac{N_V}{N_A}\right) \quad (12)$$

$$N_V=4.82x10^{15}T^{\frac{3}{2}}\left(\frac{m_h^*}{m_0}\right)^{\frac{3}{2}} \quad (13)$$

where N_V is the effective density of states in Si valance band, m_h^*=0.16 m_0 the effective mass of holes [40] and m_o is the rest mass of the electron.

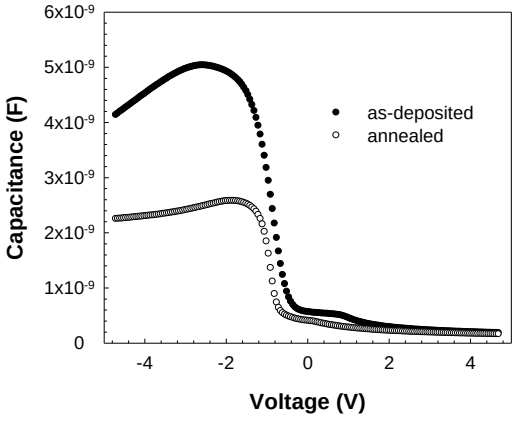

Fig. 4. Forward and reverse bias capacitance-voltage (C-V) characteristics of the Al/HfO₂/p-Si (100) Schottky diodes.

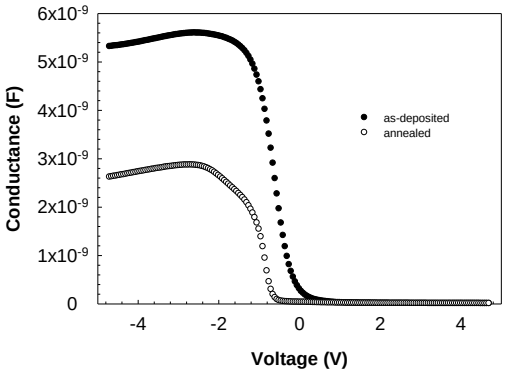

Fig. 5. Forward and reverse bias conductance-voltage (G/w-V) characteristics of the Al/HfO₂/p-Si (100) Schottky diodes.

Fig. 4 shows a comparison of the capacitance density versus gate bias characteristics for the as-deposited and annealed HfO_2 diodes measured at 1 MHz [41]. It is clear that the capacitance of the annealed diode decreases compared to the as-deposited diode due to the increase of the interlayer thickness between HfO_2 and silicon, which was confirmed on TEM measurements [42-44]. The increase in the thickness of the interfacial layer after annealing was observed for similar structures [45]. In Fig. 4, it is also observed that the flatband voltage shifted negatively upon annealing, which indicates that negative fixed charges are compensated by positive charge generated during post- annealing [46].

Fig. 5 shows the high frequency (1 MHz) conductance- voltage *(G/w-V)* characteristics upon annealing condition. It is apparent that the capacitance of the annealed diode is lower compared to the as-deposited diode because of the increase of the interlayer thickness between HfO_2 and silicon [42].

In Fig. 6, the C^{-2}-V characteristics of Al/HfO_2/p-Si (100) Schottky diodes are shown. As shown in Fig. 6, the linear behavior of the C^{-2} vs V curves can be explained by the fact the interface states (N_{ss}) and the inversion layer charge cannot follow the ac signal at 1 MHz frequency and consequently do not contribute appreciably to the diode capacitance.

The various parameters determined from C-V characteristics of Al/HfO_2/p-Si (100) Schottky diodes are given in Table 1.

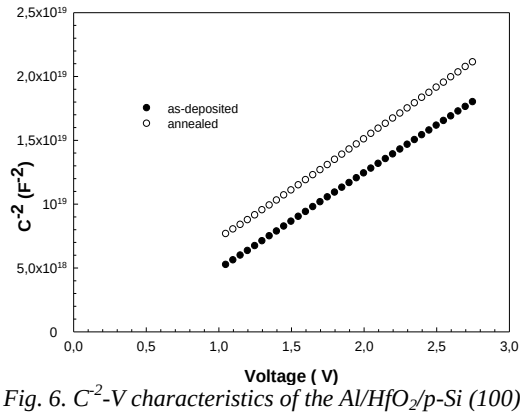

Fig. 6. C^{-2}-V characteristics of the Al/HfO₂/p-Si (100) Schottky diodes.

According to the Hill-Coleman [47], density of interface states is given by

$$N_{ss} = \frac{2}{qA}\frac{(G/\omega)_{\max}}{\left[\left((G/\omega)_{\max}/C_{ox}\right)^2 + \left(1-(C_m/C_{ox})\right)^2\right]} \quad (14)$$

where, A is the area of the diode, ω is the angular frequency, C_m and $(G_m/\omega)_{\max}$ are the measured capacitance and conductance which correspond to peak values, respectively, and C_{ox} is the capacitance of insulator layer.

From this relation, C_{ox} is obtained as

$$C_{ox} = C_{ma}\left[1+\left(\frac{G_{ma}}{\omega C_{ma}}\right)^2\right] \quad (15)$$

The HfO_2 film thicknesses were calculated from the Eq. (15), and given in Table 1.

The real series resistance of MIS devices can be subtracted from the measured capacitance (C_{ma}) and conductance (G_{ma}) values in strong accumulation region at high frequency (f≥1MHz) [39].

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \left(\omega C_{ma}\right)^2} \quad (16)$$

Fig. 7 depicts the variation of the series resistance as a function of voltage at room temperature. As shown in Fig. 7, the series resistance of the annealed diode is slightly higher compared with the as-deposited diode. It can be ascribed to the increase of the interlayer thickness between HfO_2 and silicon after annealing [42].

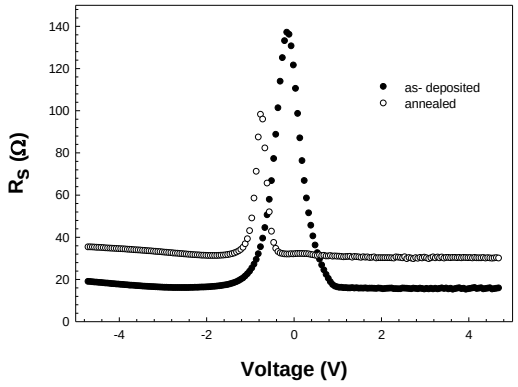

Fig. 7. The variation of the series resistance as a function of voltage at room temperature.

Table 1. The values of various parameters determined from C-V characteristics of Al/HfO_2/p-Si (100) Schottky diodes at room temperature.

.	V_d (eV)	$N_a x10^{16}$ (cm^{-3})	E_f (eV)	$\Delta\Phi_b$ (eV)	Φ_b (eV)	$W_d x10^{-5}$ (cm)	$Nss\ x10^{13}$ ($eV^{-1}cm^{-2}$)	dox (Å)
As-deposited	0,377	2.56	0.155	0.029	0.504	1.39	7.39	153
annealed	0,134	2.41	0.158	0.028	0.263	0.86	3.60	298

As shown in Table 1, the obtained mean N_{ss} values calculated from *C-V* characteristics decreases with annealing and they are in a close agreement with N_{ss} calculated from *I-V* characteristics.

4. Conclusion

In summary, the effect of annealing on the electrical properties of Al/HfO_2/*p*-Si (100) Schottky diodes was investigated at room temperature. On annealing 2 h at 700 ^{0}C, the annealed sample shows clear differences than as-deposited sample regarding mainly the leakage current and density of interface states. The annealed sample has a lower leakage current and density of interface states. It was also appeared that the capacitance of the annealed diode decreases compared with the as-deposited diode due to the increase of the interlayer thickness between HfO_2 and silicon. The flatband voltage shifted negatively upon annealing, indicating that negative fixed charges is compensated by positive charge generated during post-annealing.

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*Corresponding author: mahir@gazi.edu.tr