Au/PAr/n-CdS/ITO polymer insulated MIS structure

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In this work, we present optical, structural and electrical characterizations of Au/PAr/CdS metal interlayer semiconductor diode (MIS) structure by X-Ray diffraction (XRD), ultraviolet-visible (UV-vis) spectroscopy and curent-voltage (I-V) measurements at room temperature and in the dark. CdS was deposited onto ITO substrates by spray pyrolysing method, PAr was coated over CdS by drop-casting method and a gold metal contact was evaporated by e-beam evaporation system. The barrier height of Au/CdS (MS) structure was calculated to be 0,48eV. The barrier height of Au/PAr/CdS MIS structure was found different from that of the SBH value of Au/CdS MS structure. For the Au/PAr/CdS (MIS) structure, the barrier height, ϕ_B, and ideality factor, n, have been calculated as 0.61 eV and 2.25, respectively, from forward bias I-V measurements. The higher ideality factor attributed to the series resistance, R_s was calculated as 907.4 kΩ and 897.1 kΩ from Cheung functions. The effective barrier height, ϕ_B, and the series resistance, R_s, of the Au/PAr/CdS structure were also calculated using Norde method and found to be as 0.74 eV. and 974 kΩ respectively. The interface state density (N_{ss}) were obtained from the forward bias I–V characteristics at a region changing from $4x10^{15}$ $eV^{-1}cm^{-2}$ to $1x10^{15}$ $eV^{-1}cm^{-2}$. The charge transport mechanism of the structure were determined by the power law behaviour of the current with different exponent $I \propto V^{m+1}$ were determined and three main slopes were found.

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Keywords: Au/PAr/CdS, Schottky diode, MIS structure parameters, Density of states, Charge transport mechanism.

1. Introduction

The field of hybrid electronics structure is of particular interest since their usefulness as an active sensing elements, non-volatile memory structure, field effect transistors, microwave diodes, photo-detectors applications and displays [1, 2, 3].

In the metal-semiconductor junctions and interlayer structure properties play an important role in the electrical performance and stability of the metal insulator semiconductor (MIS) structures. The insertion of an interlayer between the metal and the semiconductor alters the electrical parameters of the MIS diodes such as Schottky barrier height (SBH), ideality factor, series resistance and interface state density [4-15].

The recently developed polyarylate (PAr) has been reported to display outstanding performance in radiation and high temperature environments [16]. The material, which has also good electrical and mechanical properties at cryogenic temperatures, has low density and moisture absorption and may be used in electrical and electronic circuit boards, solar cells, superconductors, detectors, as well as in aerospace and automotive industries [17].

In this work, an Au/PAr/n-CdS metal/insulator/ semiconductor (MIS) structure was fabricated by using spray pyrolysis for CdS and drop-casting method for PAr onto ITO substrate. The structural and optical parameters of Au/PAr/n-CdS/ITO (MIS) device were determined by XRD and UV-Vis measurements. The extraction of interface state density of Au/PAr/n-CdS/ITO (MIS) Schottky diodes using the current-voltage (I-V) characteristics were reported. The characteristic parameters such as ideality factor, barrier height, density of interface states and series resistance of Au/PAr/n-CdS/ITO (MIS) Schottky diode obtained from I-V characteristics were calculated at room temperature. In order to determine charge transport mechanism of the structure, the power law behaviour of the current with different exponent $I \propto V^{m+1}$ were determined and three main slopes were found.

2. Experimental details

The Au/PAr/CdS/ITO (MIS) Schottky diodes were fabricated on the ITO coated glass substrate with a 10mm - 15mm dimension and 2.10^{-4}Ωm resistivity. The *n*-type semiconductor CdS was produced with spray pyrolaysis (SP) method. The crystal has prefentially (101) H orientation and 2.11 μm film thickness. For the depositing process, first ITO substrates were degreased with ultrasonic bath in ethanol and distilled water solution during 20 minutes at 80°C and 15 minutes in acetone solution. Thereafter substrates were rinsed in distilled water and after that cleaning procedure towelled in N_2 atmosphere. Presently, the CdS film were deposited with spray pyrolysis method. For the film deposition, 0.02M $CdCl_2$ and 0.02M $CS(NH_2)_2$ aqueous solution was prepared. The solution was stored during one day for the precipitation of impuruties. The prepared solution was sprayed on the ITO substrates at 400°C.

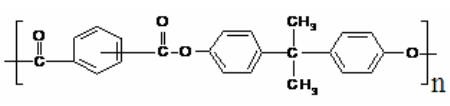


Fig. 1. Chemical structure of polyarylate.

Before the insulator film coating, CdS film was polished with 5 μm diamond paste and then 190 nm PAr layer formed on it with drop-casting method. Au metal was evaporated as the top ohmic contact. All evaporation process was carried out in 10^{-5} Torr vacuum atmosphere. The dark current-voltage (I-V) measurements of Au/PAr/n-CdS (MIS) Schottky diode were performed by using a programmable Keitley 6517A digital electrometer/ voltage source and Keithley 199 multimeter GPIB interfaced to the computer and temperature was controlled by Lakeshore Temperature Controller 331.

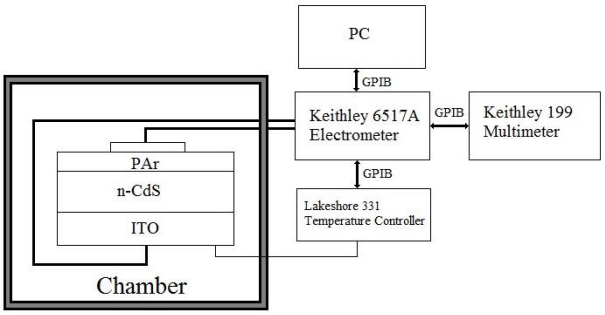


Fig. 2. Measurement set-up.

3. Results and discussion

3.1Structural and optical characterization

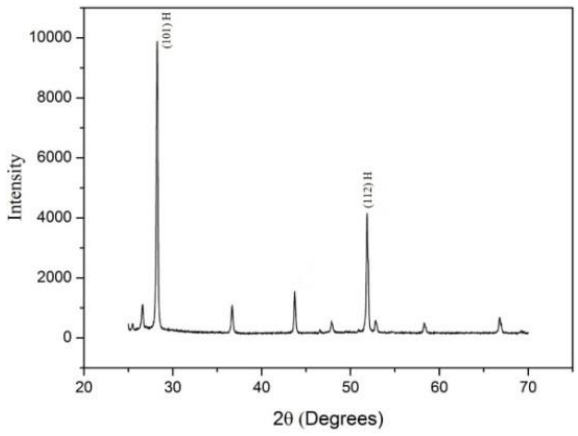
Thin film CdS showed n-type conductivity properties which was determined by the hot probe method.

X-ray diffraction of spray pyrolysed CdS films and PAr films were performed on GCA-MMA diffractometer (Fig.3a and 3b). Lattice spacings (d_{lat}), lattice constants parameters of CdS crystal were determined from the X-Ray Diffraction pattern.

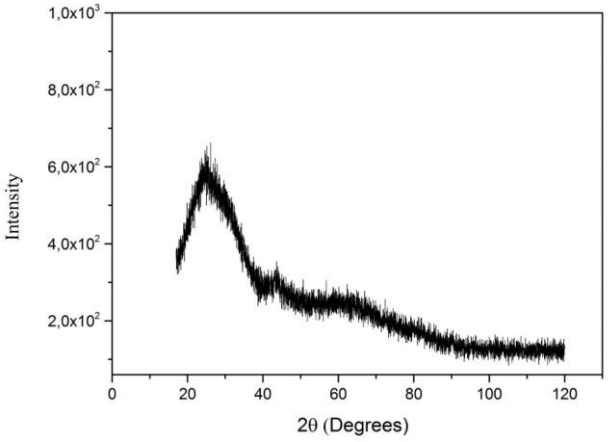
The grain size values (D) were calculated by using Debye-Scherer formula such that,

$$D = 0.94 \cdot \lambda / B \cdot cos\theta \qquad (1)$$

where λ is the wavelength of the X-ray and β is the width of the half of the X-ray diffraction pattern maximum. The major peaks were observed at 28.26^o and 51.86^o for hexagonal n-CdS film.



(a)



(b)

Fig. 3. XRD pattern of a)CdS and b) Polyarylate.

Table 1 shows the structure parameters such as lattice spacing and grain size for different crystal planes. Also the lattice constants are found to be a = 4.1A^o and c = 6.91A^o for hexagonal structure and there is good agreement with literature [18-21]. PAr thin film structure has been inverstigated in 10^o– 120^o range and amorphous behaviour was identified. The XRD pattern for the amorphous structure of PAr polymer thin film shown in Fig. 3b.

Table 1. Structural parameters of n type CdS film.

2θ (Degree)	(hkl)	d_{lat} (A)	Grain Size (nm)
28.26	(101)	3.16	42.85
51.86	(112)	1.79	46.58

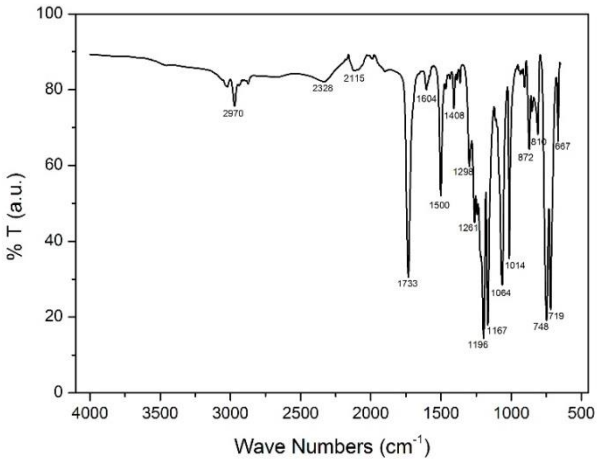


Fig. 4. FTIR spectra of Polyarylate film.

From the FTIR spectra of the Polyarylate film, peaks for aromatic ring oscillation at 2537-1960 cm^{-1} and for ester carbonyl (C=O stretch) at 1733 cm^{-1} and for ester (C-O stretch) at 1196 cm^{-1} were observed in Fig. 4. UV-VIS transmittance measurements have been carried out by Perkin-Elmer Lambda 2S spectrometer at the range of 300-100 nm. The absorption coefficient values were obtained from the transmittance–wavelength (T-λ) measurements.

For the direct band gap metarials such as CdS, the relation between the absorption coefficient (α) and the optical band gap (E_g) could be given as,

$$(\alpha h\upsilon)^2 = B\left(h\upsilon - E_g\right) \tag{2}$$

where B is a constant and $h\upsilon$ is the photon energy. The intercept point of the energy axis at $(\alpha h\upsilon)^2$ vs. $h\upsilon$ plot shown in Fig. 5, gives the band gap value and here it was calculated as 2.42 eV for CdS.

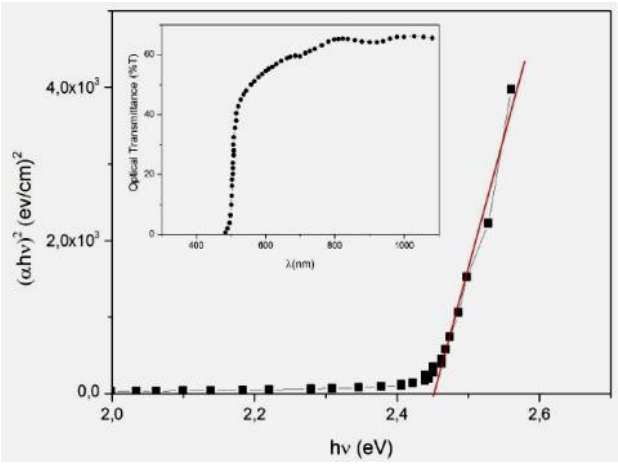


Fig. 5. Absorption spectra of CdS film.

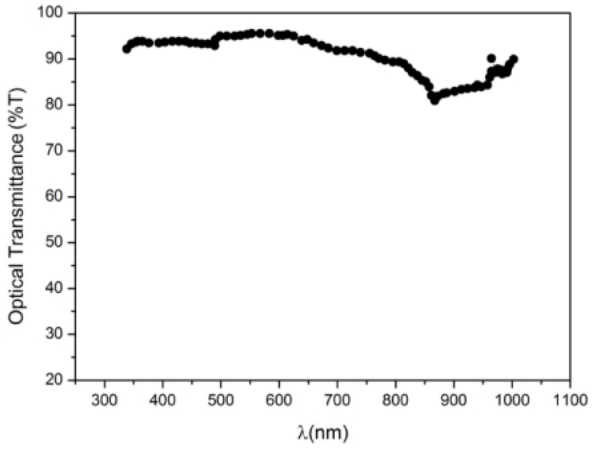


Fig. 6. Transmittance spectra of PAr film.

The transmittance measurements were also carried for PAr films and no absorption were observed at the studied wavelength range.

3.2 I – V Characteristics

For a metal-insulator-semiconductor (MIS) Schottky diode with an interfacial insulator layer, *J-V* characteristics were used with Cheung functions, to determine the most important parameters of the structure, such as barrier height ϕ_B, ideality factor (n) and series resistance (Rs). According to the thermionic emmission theory (TE), the relation between the current density through and voltage applied across a Schottky diode, is given by [22, 23]

$$J = J_o\, exp\left(\frac{q(V-IR_S)}{nkT} - 1\right) \tag{3}$$

where V is the applied voltage across the contact, n is the ideality factor, R_s is the series resistance, T is the absolute temperature in K, q is the electronic charge, k is the Boltzmann constant, J_0 is the reverse saturation current density and is expressed as

$$J_o = AA * T^2\, exp\left(\frac{-q\phi_B}{kT}\right) \tag{4}$$

where A is the effective contact area of the rectifier contact, A^* is the effective Richardson constant and equals to 25 $A\, cm^{-2}K^{-2}$ for CdS and ϕ_B is the barrier height at zero bias.

The semi-logarithmic forward and reverse bias current density voltage (J - V) characteristic of the Au/PAr/CdS MIS Schottky diode is shown in Fig. 6 having a rectifying behaviour at dark and room temperature. As can be seen from Fig. 6, the electrical current density has a curvature as the series resistance effects has become dominant at high current in the semilogarithmic ln(I)-V plot for forward bias while the series resistance effect could be neglected in the linear region of forward bias for I-V plot. An exponential increase in the forward bias current and a weak voltage dependence of the reverse bias current were observed as a characteristic rectifying interfaces behaviour property.

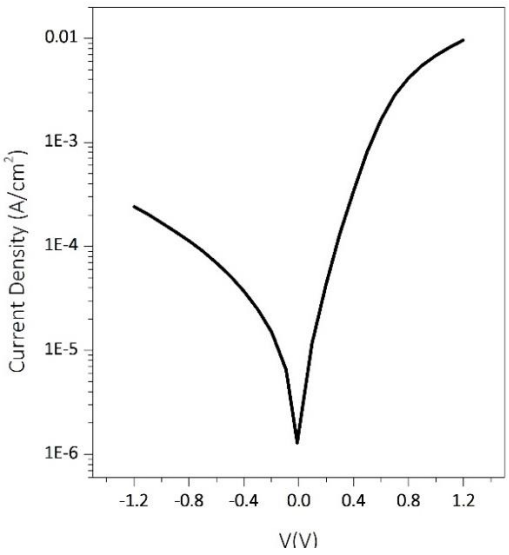


Fig. 7. Current density-voltage characteristic of Au/PAr/CdS MIS Schottky diode.

Higher ideality factor value than unity shows deviation from the ideal thermionic emission theory that the deviation was attributed to the high interface state density (N_{ss}) and high series resistance [21, 25]. The series resistance, R_s, responsible from the deviation from linearity at higher forward bias current voltage (I-V) region, and the ideality factor, n, can be determined by Cheung functions [22, 25], *(dV/dlnJ)*, extracting from the equation (3) and (4), could be expressed as

$$\frac{dV}{dln(J)} = \frac{n}{\beta} + R_s A.J \quad (5)$$

where $\beta = q/kT$ and if the *dV/dln(J)-J* graph is drawn, the slope of linear region gives the series resistance, R_s and the intercept of the line where *J=0* determines the ideality factor, n.

The series resistance (R_s) and the barrier height ϕ_B are also determined by the Cheung function *H(J)* that can be written as follows

$$H(J) = V - \frac{n}{\beta} ln\left(\frac{J}{A^*T^2}\right) \quad (6)$$

and it also can be written as

$$H(J) = n\phi_B + R_s A.J \quad (7)$$

where the slope of straight line for *H*(*J*)-*J* plot gives the series resistance, R_s and if the ideality factor is known from Eq.5, the intercept of the line where *J=0* determines the barrier height, ϕ_B. Fig. 8 shows dV/dlnJ vs J and H(J) vs J plots drawn for Au/PAr/CdS MIS Schottky diode at room temperature.

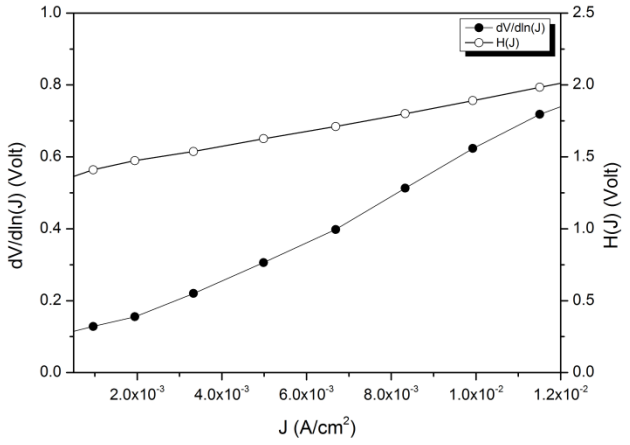


Fig. 8. dV/dlnJ vs J and H(J) vs J plots for Au/PAr/CdS MIS Schottky diode.

The barrier height of Au/CdS (MS) structure was calculated to be 0,48eV which is the same as in the literature [24]. The barrier height of Au/PAr/CdS MIS structure was found different from the SBH value of Au/CdS MS structure.

The ideality factor and the series resistance of Au/PAr/CdS diode were found from dV/dlnJ vs J plot (Fig.8) as n=2.25 and R_s = 907.4 kΩ. The barrier height and the series resistance of Schottky diode was determined from H(J) vs J plot (Fig.8) as ϕ_B = 0.62eV and R_s = 896.1 kΩ. The series resistance values, R_s, were found to be consistent with each other which were obtained by Cheung functions, dV/dlnJ–J and H(J)-J. Therefore, by using J-V measurements, and performing two plots of the J-V data, the diode parameters such as n, R_s and ϕ_B, which control the device performance, can be determined.

3.3 Norde method

Another technique, suggested by Norde [26] is used to determine the barrier height ϕ_B, and the series resistance, R_s, of the structure by using an equation,

$$F(V) = \frac{V}{\alpha} - \frac{kT}{q} \ln\left(\frac{J}{A^*T}\right) \quad (8)$$

where α is a constant greater than unity and n is ideality factor, ($1 < n < \alpha$).

From the $F(V)$ - V characteristics, the barrier height, ϕ_B, could be calculated as

$$\phi_B = F(V_o) - \frac{kT}{q} + \frac{V_o}{\alpha} \quad (9)$$

where $F(V_0)$ is the minimum value of $F(V)$ and V_0 is the corresponding voltage. $F(V)$-V characteristic of the Au/PAr/CdS structure, was shown in Fig. 9. The barrier height value, ϕ_B, was calculated from Eq.9 and found as 0.74 eV.

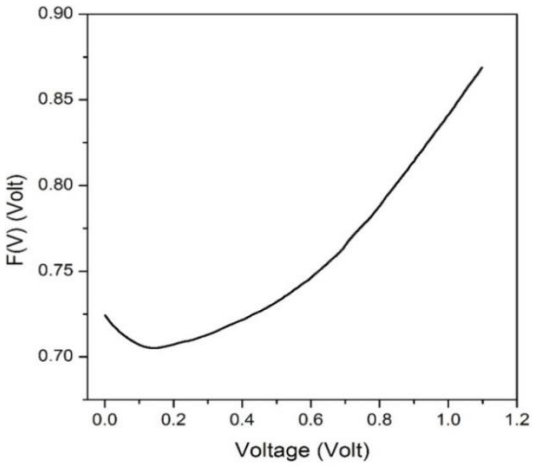


Fig. 9. F(V) – V plot of the Au/Par/CdS structure at room temperature.

By means of Norde method, the the series resistance, R_s is expressed as

$$R_s = \frac{kT}{q} \frac{(n-\alpha)}{I_o} \quad (10)$$

and the series resistance value was calculated as R_s = 974 kΩ.

The insertion of an interlayer between the metal and the semiconductor alters the electrical parameters of the MIS diodes such as Schottky barrier height (SBH), ideality factor, series resistance and interface state density [4].

As mentioned in the paper [4], the barrier height could be either increased or decreased by the interlayer. In this

work, we show that the insertion of the PAr increased the barier height of the Au/CdS structure from 0,48 eV to that of the Au/PAr/CdS of 0,62eV or to 0,74eV founded by Cheung's method and by Norde's method.

3.4 Interface state density distribution

The interface state profile of diodes is known as significant factor for their performance and characteristic parameters. The interface between semiconductor and insulator layer effecs the density of states of the surface levels of the semiconductor which means that just for electron and holes, density of states in the valance and conduction band can be effected by the interface transition. The nonlinearity of the I-V characteristics of the MIS structure especially at high voltages denotes the interface states with continium behaviour.

Due to the presence of the interface states in equilibrium with the semiconductor and also ideality factor is greater than unity, the effective barrier height is assumed to be bias-dependent [7, 8]. The effective barrier height ϕ_e is written as

$$\phi_e = \phi_B + \left(1 - \frac{1}{n(V)}\right).(V - IR_s) \qquad (12)$$

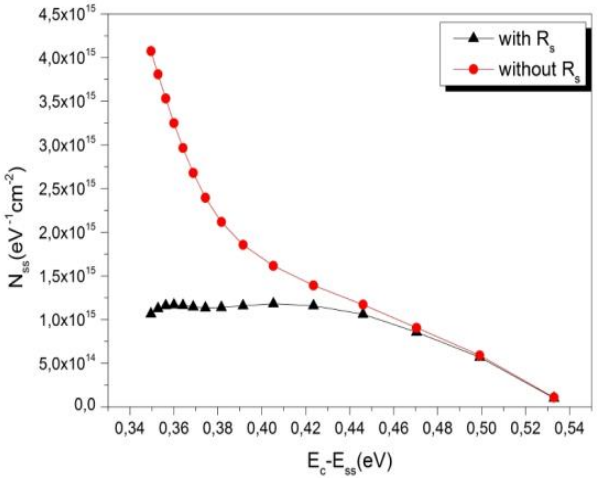


Fig. 10. Interface state density distribution of Au/Par/CdS.

The energy difference between the bottom of the conduction band at the surface of *n*-type semiconductor (E_c) and the energy of the interface states (N_{ss}) is given by

$$E_c - E_{ss} = q.(\phi_e - (V - IR_s)) \qquad (13)$$

The relation between the interface state density (N_{ss}) and the effective ideality factor $n(V)$ is expressed as

$$N_{ss} = \frac{1}{q}\left[\frac{\epsilon_i}{d}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \qquad (14)$$

where d is the thickness of the semiconductor film, W_D is the depletion layer length, ε_i and ε_s are permitivity of insulator and semiconductor, respectively. The interface energy states distribution profile N_{ss} was obtained from the forward bias *I-V* data by with and without taking series resistance, R_s, into account, and the N_{ss} values were calculated from Eq. 12, with the voltage-dependent $n(V)$ values.

Fig. 10 shows the density of interface states (N_{ss}) distribution profiles as a function E_c - E_{ss} in eV for the Au/Par/CdS structure room temperature. It shows that the series resistance is an important parameter for determining the interface state density (N_{ss}) distribution. An exponential increase of density of the interface states from the mid-gap to the bottom of the conduction band and also decrease of density of the interface states depending on increasing applied voltage was observed.

It can be seen from Fig. 10, the magnitude of the N_{ss}, with and without the R_s, has changed from 1×10^{15} eV^{-1} cm^{-2} to 4×10^{15} eV^{-1} cm^{-2} at E_c-0.35(eV) for the structure, respectively. The energy values of the density distribution of the interface states of the SBD is in the range E_c-0.35 and E_c-0.54 eV.

The values of N_{ss} obtained by taking into account the R_s were found to be lower than those of without the R_s. As a result, the R_s value should be considered in determining the interface state density distribution profiles. Similar results have been reported in the literature [27-30].

3.5 The charge transport mechanism

In order to determine charge transport mechanism of the structure, double log graphics of current v.s. voltage were drawn. The power law behaviour of the current with different exponent $I \propto V^{m+1}$ were determined. There are three main slopes in the graph. At the first region the slope is 1.89, the second region the slope is 3.65 and the last region the slope is 2.09.

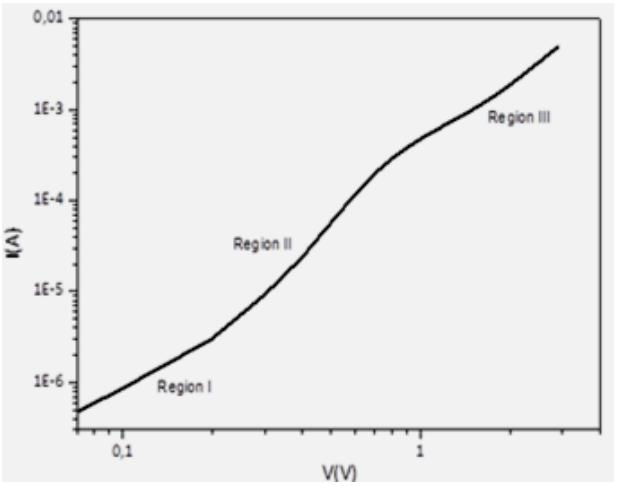


Fig. 11. Double-logarithmic I-V plot of the Au/PAr/CdS (MIS) SBD at room temperature.

In the first region, conductivity mechanism showed ohmic behaviour. In the second region, the power factor is greater than two which means that conduction mechanism is controlled by trapped-charge limited current (TCLC) with an exponential trap distribution. Here the carriers were injected from CdS which have lower than moderate charge carries (N_d=1.974.10^8 cm^{-3}) to the notably resistive PAr polymer due to the lower carrier concentration than CdS results in trap-charge-limited-current at voltage of

interest. Impurities, disorders, discontinuities of transition between semiconductor and polymer surface and dangling bonds are the cause of the traps. In the last region conductivity mechanism is SCLC. If the density of injected free carriers comparably is much larger than the thermally generated free charge carriers, the SCLC dominates the conductivity of the carriers through the device [31-33].

4. Conclusions

In this study, An Au/PAr/CdS sandwich MIS diode has been fabricated and optical, structural and electrical characterizations were realized and diode parameters were calculated. The electrical properties of Au/PAr/CdS (MIS) Schottky diodes have been analyzed by using the current-voltage (I-V) characteristics at room temperature. It was observed that the structure has a rectifying behaviour. As a characteristic rectifying interfaces behaviour property, the exponential increase of the forward bias current and a weak voltage dependence of the reverse bias current were observed. The nonideal forward bias J-V behaviour observed in the structure is attributed to a change in the metal/semiconductor barrier height due to the interface states, the interfacial insulator layer and series resistance.

The insertion of an interlayer between the metal and the semiconductor alters the electrical parameters of the MIS diodes such as Schottky barrier height (SBH), ideality factor, series resistance and interface state density. As mentioned in the literature, the barrier height could be either increased or decreased by the interlayer. In this work, we show that the insertion of the PAr increased the barier height of the Au/CdS structure from 0,48 eV to that of the Au/PAr/CdS of 0,62eV or to 0,74eV founded by Cheung's method and by Norde's method.

The values of ideality factor and barrier height have been calculated as 2.25 and 0.62 eV, respectively, from forward bias *J-V* measurements. The ideality factor value obtained from *J-V* characteristics are higher than unity attributed to the presence of a thin interfacial insulator layer between the metal and semiconductor. Then, the higher ideality factor attributed to the series resistance (R_s) was calculated as 907.4 kΩ and 897.1 kΩ by using Cheung functions and the interface state density (N_{ss}) were obtained from the forward bias I–V characteristics at a region changing from 4×10^{15} $eV^{-1}cm^{-2}$ to 1×10^{15} $eV^{-1}cm^{-2}$. Effective barrier height ϕ_B and the series resistance (R_s) of the Au/PAr/CdS structure were calculated also using Norde method and found to be 0.74 eV and 974 kΩ respectively. As seen in the both methods, the barrier height of Au/PAr/CdS MIS structure is different from the value of 0,48eV which was calculated for the SBH of Au/CdS structure as found in the literature.

The charge transport mechanism of the structure were also determined. The power law behaviour of the current with different exponent $I \propto V^{m+1}$ were determined and three main slopes were found.

In summary, in the present study, we conclude that the prepared MIS Schottky diodes have been controlled by the interfacial insulator layer and interface states, which are responsible for the nonideal behaviour of *J-V* characteristics.

Acknowledgements

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