Characterization of Au/PS/p-Si heterojunction

ISSAM M. IBRAHIM, ESTABRAQ. T. ABDULLAH, YOUSIF ABID AL SHAABANI[a], ASMIET RAMIZY[b,*]
Department of Physics, College of Science/University of Baghdad, Iraq
[a]*Open Education Collage Iraq*
[b]*Physics Department, College of Sciences, University of Anbar-Iraq*

The porous silicon (PS) layers were formed on p-type silicon (Si) wafer. The samples were anodized electrically with 50 mA/cm^2 fixed current density for different etching times. The structural properties of porous silicon on silicon substrates were investigated by photoluminescence (PL). The band gap of the samples was measured through the photoluminescence (PL) peak. It shows that band gap value increases by raising the porosity. Photodiodes of the Au/PS/p-Si/Al was performed. I-V characteristics shows that the maximum efficiency of this system is at etching time=30min (η =0.32) while at 10min the efficiency drop (0.08). The C-V characteristics were measured, and it was found within the range V_{bi}= 0.2-1.5 Volt at different frequencies and etching time. The results show a strong influence of the etching time parameters on kinetic changes of the device's electrical properties.

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1. Introduction

When crystalline silicon (c-Si) wafers are electrochemically etched in hydrofluoric acid (HF) at specific current densities, pores are formed, which is known as a porous silicon (PS) layer [1]. This is an interesting material due to its unique and unusual optical and electrical properties compared to bulk Si substrate. Structurally, PS is very complicated [2]. Some published papers indicate that PS layers consist of Si columns and pores or isolated nanocrystallites [3]. On the other hand, PS may be considered as a system of interconnected quantum wells, the so-called quantum sponge [4]. Nevertheless, the properties of PS, such as porosity, thickness, pore diameter and, microstructure of silicon, have been reported to depend on anodisation conditions, including the electrolyte, current density, wafer type and resistivity, etching time, and temperature [5]. The first report of room temperature visible photoluminescence (PL) from PS structures has attracted wide interest in the scientific community [6,7]. The mechanism of light emission in porous silicon is not fully understood. One popular hypothesis is that luminescence is due to quantum confinement of charge carriers in narrow crystalline silicon walls separating the pores [7]. The increase in the band gap of PS is possible by reducing the size of the nanocrystallites [8]. Another hypothesis asserts the existence of luminescent surface species trapped on the inner pore walls as the source of light emission [9]. Another concludes that the origin of luminescence can be traced to the presence of surface-confined molecular emitters, such as siloxene ($Si_6O_3H_6$) derivative, present in porous silicon [10].

The use of PS as an efficient material in optoelectronics, optical interconnections and electroluminescent devices leads to ultra-large-scale-integrated (ULSI) applications. Also this PS is being used in micromachining, in which it acts as sacrificial layer and biomaterial in different applications. PS is a candidate for silicon-based optoelectronic applications, such as light-emitting devices, solar cells, and sensing devices [11-14]. PS is attractive in solar cell applications because it is efficient as antireflection coating (ARC) and other properties, such as band gap broadening, wide absorption spectrum, and wide optical transition range (700–1000 nm). It can also be used for surface passivation, texturization, and removal of the dead layer diffused region. Moreover, PS can convert higher-energy solar radiation into spectrum light, which is absorbed more efficiently by PS than by bulk Si [16-21].

The aim of this study is to prepare porous silicon by electrochemical etching and study the characterization of Au/PS/p-Si/Al schottky heterojunction for solar cell applications.

2. Experimental

An electrochemical cell was used to fabricate the PS. P-type Si wafer (1cm^2) with <111> orientation, 0.75 Ω.cm resistivity and 283 μm thickness was used. Prior to the etching process, the Si substrate was cleaned by immersed in HF acid for 2 min to remove the native oxide. The electrochemical cell has two-electrode with a Si wafer anode and platinum cathode (Fig. 1). The electrolytes used were of HF:C_2H_5OH (ratio of 1:1), with current density of 50 mA/cm^2 and etching times of 10, 20, and 30 min. After

the process, the PS samples were dried under a nitrogen shower. The entire samples were prepared at room temperature (RT).To obtain the solid evidence for the existence of nanostructures, the atomic force microscopy (AFM) was used to study the surface morphology of semiconductor nanostructure layers. Furthermore, photoluminescence (PL) is also performed at room temperature by using He-Cd laser (λ=325 nm*)*. To fabricate the solar cell, the top surface area of the wafer was coated by 50nm Au (Gold) by means of thermal evaporation methods, using Edward coating unit (model 606) under high vacuum (10^{-5}m bar). In addition, aluminum evaporation was used for back metal contact. The fabricated device was analyzed using current–voltage (I–V) measurement with illumination (intensity= 69.1954 mW/cm^2). Capacitance-Voltage (C-V) characteristics of Au/PS/c-Si/Al heterojunction were measured using A multi–frequency LRC meters (model HP-R2C 4274A) operated in the 100Hz to 400 KHz frequency range.

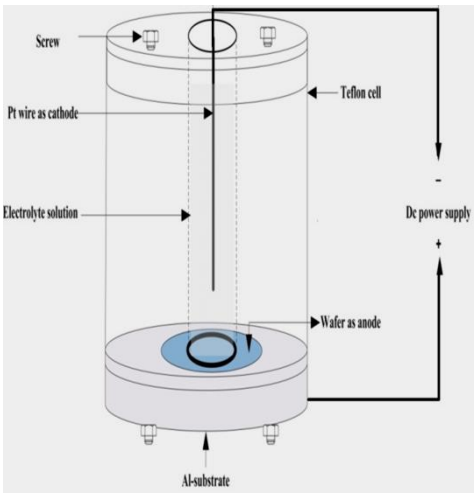

Fig. 1. Schematic of the designed porous silicon fabrication system.

3. Results and discussion

The surface morphology images of the PS prepared by the electrochemical etching process are shown in Fig. 2. The surface of the porous silicon consists of discrete pores with spherical, square-like, and elongated shapes. The surface morphology of the PS semiconductors is known to be very complicated and strongly depends on fabrication conditions. Therefore, the current density and etching time can be used to control the size and shape of the final structures. This technique of etching was adopted to synthesize Si nanostructures. From Fig. 2, the values of (PS) porosity increase with increasing of etching time. These results are attributed to increase the number and width of the pores with increasing of etching time [21]. For the formed (PS) layers on silicon substrates, when the etching time increases, the dissolution of silicon will increase leading to increase the porosity. The etching rate of (EC) etching process has attracted a great attention since it describes the etching process speed [22]. The etching rate depends on the formation parameters and is governed by the diffusion rate and drift velocities of holes to the surface [23].

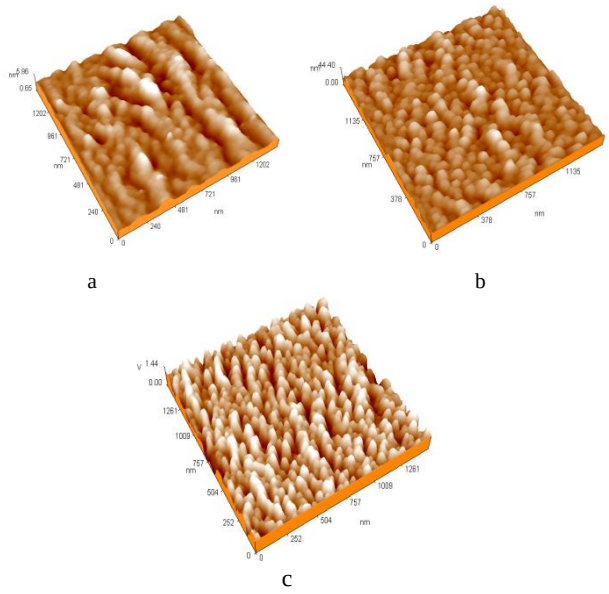

Fig. 2. 3D AFM images of the nanostructures porous silicon samples with etching time(a) 10 min (b)20min and (c) 30min.

The average of the pores size is about 59.3nm, this means that the pore diameter and nanostructure size are dependent on anodization conditions such as HF:ethanol concentration, etching time, temperature, and current density. More homogeneous and uniform distributions of pores have been shown clearly in our sample when it is compared with other samples, prepared in different electrolyte composition [24].

Photoluminescence emission spectra of PS layer prepared with a constant current density (50 mA/cm^2) by three various etching times of (10, 20 min, and 30 min) were investigated. In case of PS produced by a (30min) etching time, the obtained PL spectrum has a peak wavelength position of (727 nm) and energy peak position of (1.7 eV) compared to other cases as shown in Fig. 3 since the photo energy is larger than the band gap energy of the produced nanocrystallites. Therefore, efficient absorption could be taken place leading to contribute a wide range of crystallites sizes with the PS layer. Changes of PL peak position for the etching time of (20min), where it is blue shifted towards wavelength peak position of (4nm) and hence the energy peak is about (1.69 and 1.684 eV) for etching time 20 and 10 min respectively. This duration (10min) appears to be sufficient to break the bonding of silicon atoms from the wafer during the chemical reaction, resulting in increase on the etching rate. This leads to extension of the porous region during this duration of etching which results a thinner wall between the pores formation on the PS surface over a larger exposed area, thereby increasing the observed PL intensity.

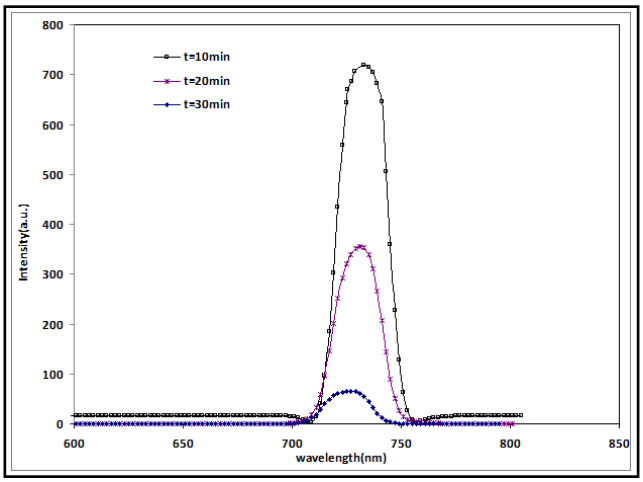

Fig. 3. PL spectra of porous Silicon prepared by electrochemical etching.

Fig. 4 shows the I–V characteristics of the metal/PS/silicon (MPS) photodiode in the dark and under irradiation. A rectifying behavior can be seen from the 0.2V curve of the as-prepared sample (Fig. 4.a), which suggests a Schottky-like junction. The reverse bias current depends very strongly on the presence of light, the open-circuit voltage V_{oc}, short-circuits current I_{sc}, maximum voltage V_m, and the maximum current I_m, which it present the prominent parameters to calculate the solar cell efficiency. The efficiency ηof the cell at the maximum power pointcan be calculated as follows:

$$\eta = P_m / P_{in} = I_m V_m / P_{in} \quad (1)$$

The fill factor (FF) is

$$F.F = I_m V_m / I_{sc} V_{oc} \quad (2)$$

where, P_m is an output power, P_{in} is an incident power. The increasing efficiency of solar cell fabricated with Au/PS/p-Si/Al attributed to increasing the open circuit voltage without losing in the short circuit current of solar cells, as shown in the Table 1. The porous surface texturing properties could enhance and increase the conversion efficiency of silicon solar cells. The results also showed that the efficiency resulting from this procedure without any doping processes more promising compared with other solar cells, fabricated under similar conditions.

Table 1. Calculation of fill factor (F.F) and efficiency to Au/Ps/P-Si/Al.

Etching time (min)	V_{oc} (V)	J_{sc} (mA/cm^2)	V_{max} (V)	J_{max} (mA/cm^2)	η%	F.F
10	0.148	0.207	0.07	0.084	0.08	0.19
20	0.157	0.219	0.078	0.095	0.12	0.21
30	0.2	0.448	0.091	0.246	0.32	0.24

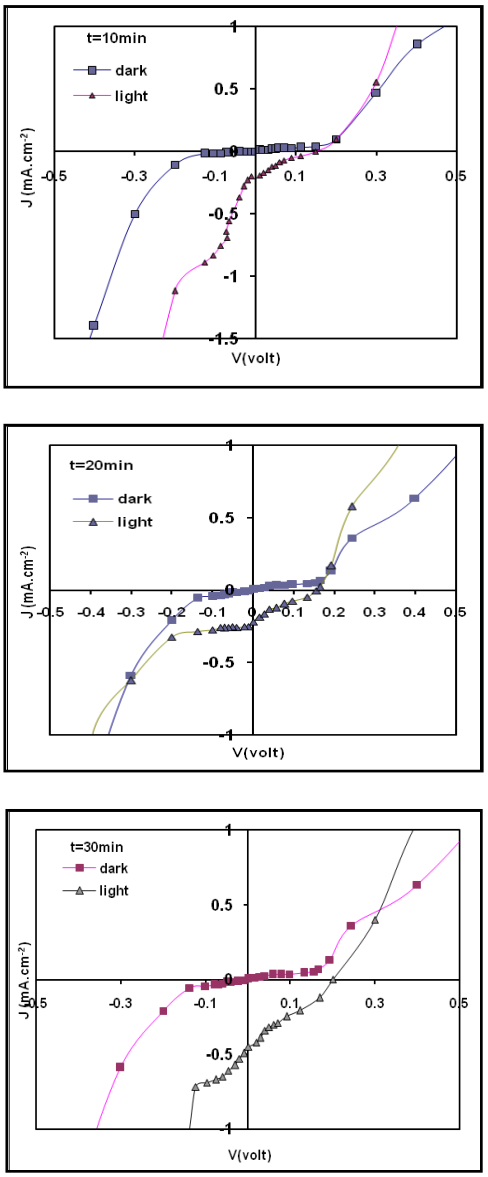

Fig. 4. The J-V characteristics of (Au/PS/p-Si/Al) at different etching time: (a) 10 min (b) 20 min (c) 30 min.

C-V measurements were made and are plotted in Fig. (5) as graphs of $1/C^2$ versus V(Volt).Due to nonlinearity of the slopes, calculations are made in the selected voltage

range of 0-1 V. The built-in potential is obtained from the intersection of the $f(V)=1/C^2$ According to C-V measurements, drawing $1/C^2$ versus V does not give a straight line (Fig. 5). This means that the depletion layer and the barrier height are not constant with frequency. From the results shown in Table 2 it can be seen that increasing the frequency leads to decrease the built in voltage. These phenomena can be explained by not only the diffusion mechanism but also by the tunneling mechanism [25].

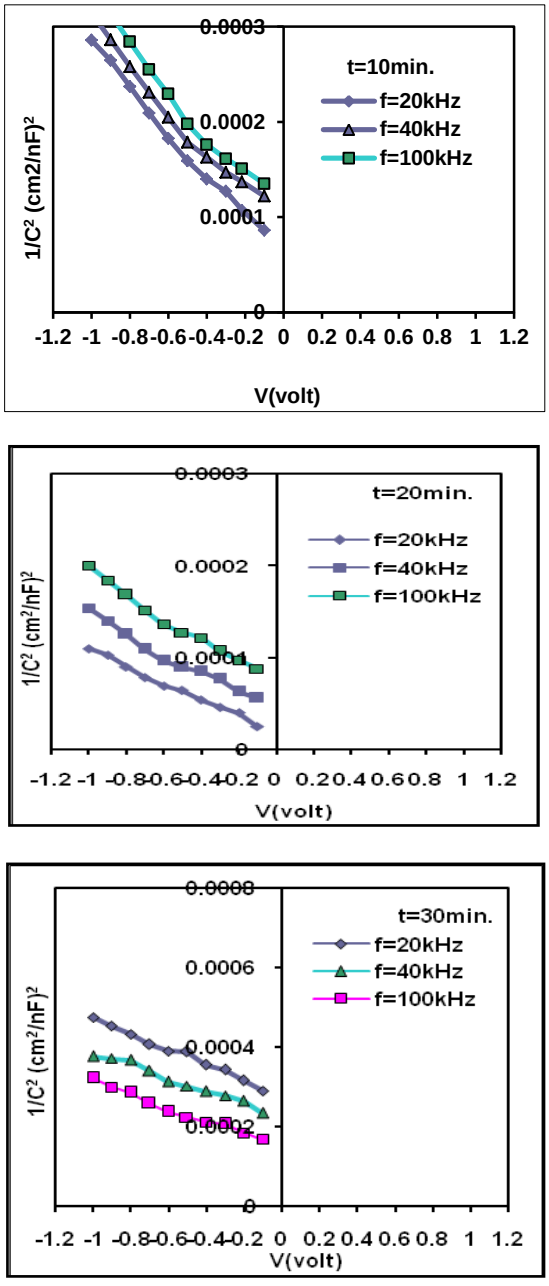

Fig. 5. The capacitance-Voltage characteristics of Au/PS/p-Si/Al which prepared at fixed current density of 50 mA/cm^2 and different etching time (a) 10 min (b)20min. (c) 30min and different frequencies.

Table 2. Built in voltage(v_{bi}) at different frequencies (f) for au/ps/p-si/al.

Etching time (min)	V_{bi}at F=100kHz	V_{bi} at F= 40kHz	V_{bi} at F=20kHz
10	0.21	0.305	0.375
20	0.20	0.30	0.40
30	0.8	1.0	1.15

4. Conclusion

Electrochemical etching is a successful method to prepare porous silicon. It is a simple, low cost and controllable. The morphological properties of PS sample show a increasing in pore width and porosity with increasing the etching time. J-V characteristics reveal strong depend on etching time and we get the efficiency from 0.08-0.32, reduction in optical losses and decrease the recombination losses on surface which causes the increment of photocurrent and efficiency. The goal of achieving photovoltaic conversion efficiencies of is desirable not only as a scientific achievement and aids in specialized applications, but can also reduce the cost of large-scale solar electric generation using the electrochemical etching which demonstrate a suitable technique for solar cell manufacturing. The built-in voltage reveals decreasing in V_{bi} with increasing frequencies.

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*Corresponding author: asmat_hadithi@yahoo.com
asmathadithi@gmail.com