Current- and capacitance- voltage analysis as a function of temperature in Au/GaN Schottky diodes

M. A. BENAMARA[*a], A.TALBI[a], B. AKKAL[a], Z. BENAMARA[a], A. BABA AHMED[b], B. GRUZZA[c], C. ROBERT-GOUMET[c]

[a] *Laboratoire de Micro-électronique Appliquée. Université DjillaliLiabès de Sidi Bel Abbès. 22000- Sidi Bel Abbès. Algeria*

[b] *Département de Médecine Faculté de Médecine de Tlemcen, Université de Tlemcen-13000-Tlemcen. Algeria*

[c] *Laboratoire des Sciences des Matériaux pour l'Electronique et d'Automatique, Université Blaise Pascal de Clermont II. Les Cézeaux 63177. Aubière. France*

Current-voltage and capacitance-voltage characteristics of Au/n-GaNSchottky diode have been measured over the temperature range from 80 to 300°K. I(V) analysis versus different temperatures gives the saturation current variation I_s (2.96×10^{-29} A - 1.91×10^{-11} A), the mean ideality factor (1.85 - 1.18), the barrier height (0.48 V - 0.86 V), and finally the serial resistance R_s variations (1050 Ω - 65 Ω). The doping concentration N_d and the diffusion voltage V_d are calculated using the C(V) characteristics. The concentration N_d is evaluated to 4.14×10^{16} cm^{-3} at 125 °K and increases with the thermal activation to 8.32×10^{16} cm^{-3}at 300 K. Nevertheless, the diffusion voltage V_d is reversibly proportional to the doping concentration N_d and decreases from 0.75 V to 0.56 V. The mean interfacial state density N_{ss}decreases with the temperature increasing, from 4.6×10^{12} cm^{-2} eV^{-1} to 1.9×10^{12} $cm^{-2}.eV^{-1}$. This improvement is the result of the molecular restructuring and the reordering at the Au/GaN interface.

(Received April 17, 2013; accepted June 12, 2013)

Keywords: Schottky diodes, Au/n─GaN, Interfacial State density, Barrier height

1. Introduction

The GaN is a promising semiconductor for high-temperature, high-frequency, and high-power device applications. The study of Schottky barrier contacts on GaN has great importance for these applications. Intensive activities over the recent years have made high-power, short-wavelength (bleu, violet light emitting diodes (LEDs) a commercial reality [1]. Other devices that have been demonstrated so far include high electron mobility transistors [2], metal semiconductor field effect transistors [3], photodetectors [4], visible light emitting diodes [5] and heterojunction bipolar transistors [6].

Lately, several studies of the metal/GaN interface have been done [7] [8]. In fact, the contacts on GaN offer a strong technological interest to design fast components and allow usthe comprehension of Schottky barrier formation phenomena. The barrier height and the various parameters depend on technological conditions of preparation.

It is known that the presence of a large density of dislocations in GaNpresents a major problem, it is necessary to understand the electrical activity of these defects and to find ways to control them.

In this work, we have studied the effect of temperature on the electrical properties of Au/n-GaNSchottky diodes. The structures are characterized electrically using $C(V_G)$ and $I(V_G)$ measurements. These ones are used and analysed through different models.

2. Technological part

The GaN samples used in this work consisted of a 4 μm thick epitaxial layer grown by metal-organic chemical vapor deposition on (0001) sapphire substrates. The films were n-type with a carrier concentration of about 10^{17} cm^{-3} and a mobility of 250 $cm^2V^{-1}s^{-1}$ at room temperature. Before metallization, the GaN film was cleaned usingtricholorethylene, acetone, methanol and isopropyl alcohol batheach for 10 min with ultrasonic agitation. The metal contacts were deposited in vacuum evaporation (Pressure 2×10^{-6}Torr).

To realize a metallic gate, we have used a molybdenum mask. This mask allows us to elaborate a gold gate of 0.6 mm diameter and thick layers of about 1000 Å. Thus, zones with and without deposits were created and hence the homogeneity and cleanliness studies of these deposits were possible.

The $I(V_G)$ measurements were made through a set-up (two 616 electrometers), and the $C(V_G)$ ones were realized using a capacitance-voltage set-up (Princeton Applied Research) with a constant 1 MHz frequency. The sample was maintained by a pumping system on a copper support so allow electrical contact.

3. Computational model

The following equation describes the $I(V_G)$ characteristic of the Schottky diode according to the thermoionic emission theory [9].

$$I = I_s\left[1 - e^{-qV/kT}\right]e^{qV/nkT} \qquad (1)$$

Where, V is the drop of applied voltage across the semiconductor surface depletion layer, and I_s the saturation current density expressed by:

$$I_s = A^{**}T^2\exp\left(-\frac{q}{kT}\phi_{Bn}\right) \qquad (2)$$

Where, T, A^{**}, ϕ_{Bn}, are the temperature in Kelvin, the effective Richardson constant and the barrier height at zero bias respectively.

For a Schottky diode with interface states, the ideality factor n can be used to include their effect on the electrical behaviour-Nss being the effective density of interface states, it is written as follow [10]:

$$n = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{w} + qN_{ss}\right] \qquad (3)$$

$\varepsilon_i$and ε_s are the interfacial layer permittivity and the semiconductor permittivity respectively. w is the depletion zone width which is deduced from the experimental $C(V_G)$ curves.

If the current transport phenomena is controlled by the thermoionic field emission, the relation $I(V_G)$ is expressed by [11, 12]:

$$I = I_s\exp(\frac{V}{E_0}) \qquad (4)$$

with

$$E_0 = E_{00}\coth(\frac{qE_{00}}{kT}) = \frac{nkT}{q} \qquad (5)$$

where, E_{00}, E_0: are the semiconductor energies relatively to the tunneling transmission probability:

$$E_{00} = \frac{h}{4\pi}\sqrt{\frac{N_d}{m^*\varepsilon_s}} \qquad (6)$$

S. Fonash [13] has shown that when the semiconductor entirely governs the populations of the interface states and the frequency is sufficiently high that these states cannot follow the a.c modulation signal. Then, the slope of the $C^{-2}(V_G)$ curve is given by :

$$\frac{dC^{-2}}{dV} = \frac{2}{\varepsilon_s q}\left[\frac{1}{N_d(1+\alpha)}\right] \qquad (7)$$

where the parameter α is given by :

$$\alpha = \frac{qN_{ss}\delta}{\varepsilon_i} \qquad (8)$$

The diffusion potential V_d is, in this case equal to:

$$V_d = \frac{V_0}{1+\alpha} + \frac{kT}{q} \qquad (9)$$

where V_0 is the intercept of $C^{-2}(V_G)$ on the bias voltage axisand the barrier heghtϕ_{Bn} is described by the following relation:

$$\phi_{Bn} = V_d + \frac{kT}{q}Ln\frac{N_c}{N_d} \qquad (10)$$

4. Results and discussion

The direct and reverse $I(V_G)$ characteristics at room temperature, are shown in Fig. 1. The direct current varies exponentially with the voltage and the reverse bias leakage current was about 380 μA at a reverse bias voltage of –10 V.

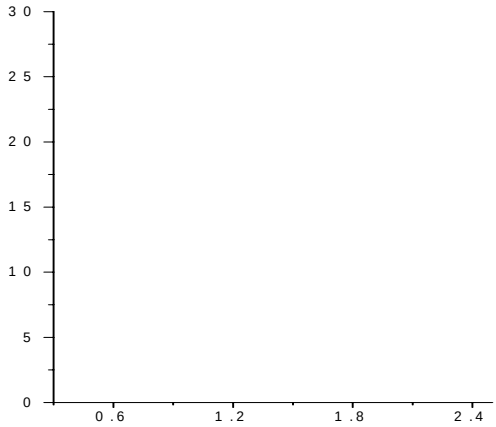

Fig. 1. Electrical characteristics $I(V_G)$obtained on Au/GaN at 300 °K.

In Fig. 2, the Ln I' = Ln $[1/(1-e^{-qV/kT})]$ versus V_G at different temperatures is plotted from 80°K to 300°K. Each characteristic presents two linear parts. The analysis of the low voltage part, between 0 and 0.53 V gives a mean value of the ideality factor n evaluated to 1.18 at room temperature and 1.85 at T= 80°K.

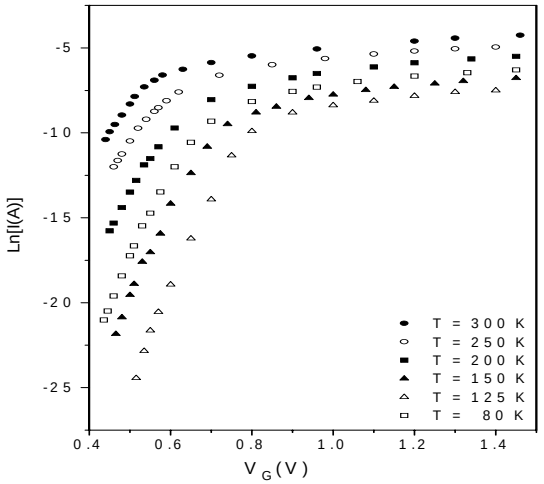

Fig. 2. lnI(V_G) obtained on Au/GaNstructure as a function of temperature.

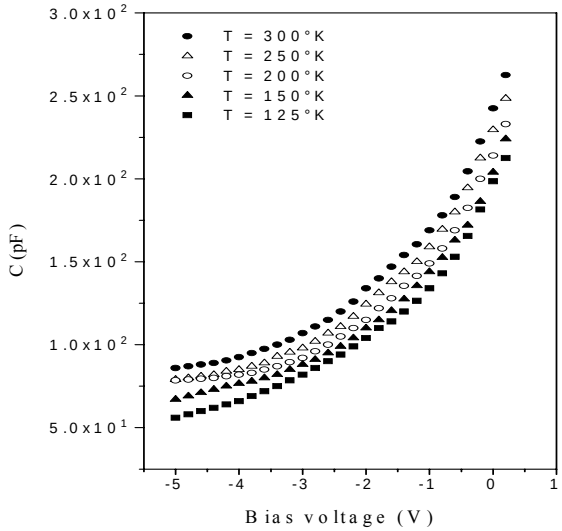

Fig. 3. Electrical characteristics C(V_G)obtained on Au/GaN structures asa function with the temperature.

The saturation current I_s, linearly extrapolated current at zero voltage on Fig. 2, appears proportional to T. It increases from 2.95×10^{-29} A at 80 K to 1.91×10^{-11} A at 300 K. Using these I_s values and the I(V) measured ones, Eq. (1) gives the fluctuation of the ideality factor n versus the bias voltage V_G.

Note that for low current, the bias voltage V_G can be considered to be equal to the voltage V applied to the GaN semiconductor depletion zone layer surface. In this particular case, one can consider only the influence of the interfacial density of states N_{ss} on the real I(V) characteristic [14]. When the current increases, this consideration is not possible and one must take in account the voltage drop of the serial resistance R_s and interfacial layer voltage V_i. In Fig. 2, we can observe clearly, for the important bias voltage, the effect of the serial resistance R_s and $V_i$voltage across interfacial layer. Considering these approximations in the second zone, the serial resistance R_s is equal to 1050 Ω at 80 K and decreases to 65 Ω at 300 K.

The electrical parameters estimated from I(V_G) curves at different temperatures are given in Table 1.

Table 1. Variation of I_s, n,ϕ_{Bn} and $R_s$as a function with temperatures.

T (K)	**I_s (A)**	**n**	**Φ_{Bn}(eV)**	**R_s(Ω)**
80	2.96×10^{-29}	1.85	0.48	1050
125	2.1×10^{-23}	1.42	0.63	635
150	4.96×10^{-21}	1.31	0.7	424
200	1.68×10^{-16}	1.27	0.76	195
250	1.96×10^{-13}	1.23	0.81	95
300	1.91×10^{-11}	1.18	0.86	65

The characteristics of the capacitance C are plotted at 1 MHz versus bias voltage at different temperatures (see in Fig. 3).

The evolution of the temperature related to the C(V_G) characteristic presents a great interest. This effect is due to the thermal activations of the carriers and consequently to the depletion zone.

Substituting in expression (4) for each temperature, the values ofideality factor n related to bias V_G andthe variation of the depletion width W(V) calculated from the C(V_G) characteristic and taking ($\varepsilon_i = 3.9 \times\varepsilon_0$ [15] and $\varepsilon_s = 9.5 \times\varepsilon_0$ [16]).We can evaluate the states density N_{ss} variation related to bias V_G. In Fig. 4, we have plotted N_{ss}=f(E_c-E_{ss}) using the following equation:

$$E_C - E_{SS} = q\cdot\left(\phi_{BN} - \Delta\phi - V_G\right) \qquad (16)$$

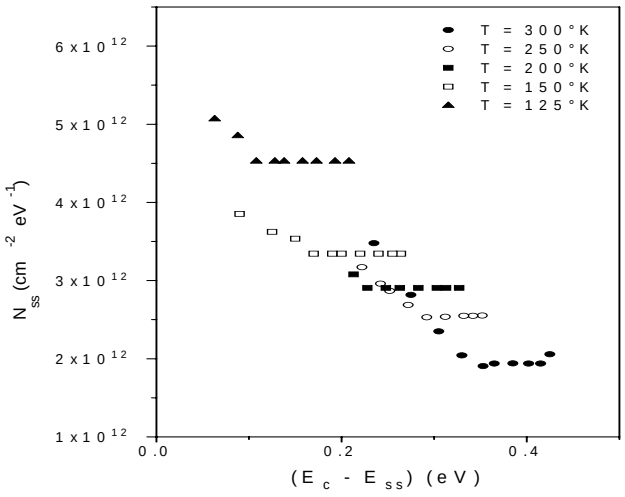

Fig. 4. Distribution of state density in theband gap of Au/GaN structure fordifferent temperatures.

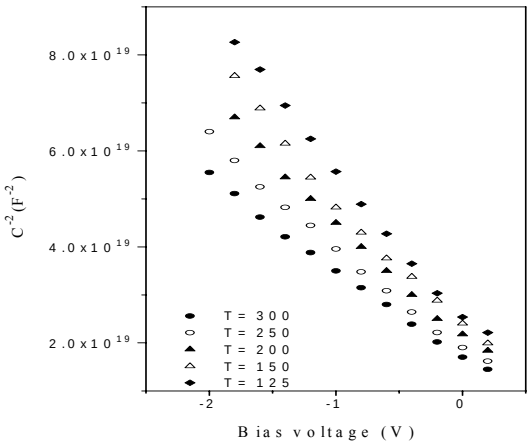

Fig. 5: Electrical characteristics $1/C^2(V_G)$ obtained on Au/GaN structure as afunction of temperature.

Then we observe,N_{ss} decreases when the temperatures increase. This improvement is due to the restructuring and the reordering of the semiconductor-metal interface under temperature effect.

The $C^{-2}(V_G)$ characteristics for each temperature illustrated in Fig. 5 are linear. Then, we can deduce that the doping concentration is uniform.

Substituting the mean interfacial states density N_{ss} equal to 1.9×10^{12} $eV^{-1}.cm^{-2}$ in expression (12), we determine the value of α which will be equal to 0.20. Taking the slope of the $dC^{-2}(V_G)/dV_G$ (Fig. 5), and the intersection with the voltage axis and using Eqs. (11) and (13), the N_d concentration and the diffusion potential V_d can be evaluated at room temperature and are equal to 8.3×10^{16} cm^{-3} and 0.75 V respectively .

The calculated values of N_d and V_d were substituted in Eq. (10) to determine the value of ϕ_{Bn} which is equal to 0.84 eV at room temperature and 0.59 at T = 125°K.

The Table (2) gives the parameters obtained from the $C(V_G)$ characteristic for each temperature.

Table 2. Electrical parameters of Au/GaN structure obtained using $C(V_G)$ characteristics

T (K)	$\mathbf{N_{ss(moy)}}$ev-^{1} cm^{-2} ($\times 10^{12}$)	$\mathbf{N_d}cm^{-3}$ ($\times 10^{16}$)	$\mathbf{V_d}$(V)	$\mathbf{\Phi_{Bn}}$**(eV)**
125	4.60	4.14	0.56	0.59
150	3.40	5.14	0.63	0.67
200	2.92	5.98	0.68	0.73
250	2.42	6.98	0.69	0.76
300	1.90	8.30	0.75	0.84

In our case, we cannot plot the electrical characteristics at the frequencies less than 100 Hz and consequently cannot study the interface state computation for slow states. This is due to the instability of the used set-up.

5. Conclusion

The ideality factor n is nearly unity, indicating current flow by thermionic emission under forward bias.

The barrier height ϕ_{Bn} was found to be 0.91 and 1.01 V from $I(V_G)$ and $C(V_G)$ measurements, respectively.

The linearity of the $C^{-2}(V_G)$ characteristic is due to the uniform distribution of the interfacial states density N_{ss} and the doping concentrationN_d in the band gap. The improvement obtained by temperature effect is probably due to the thermal restructuring and reordering of the interface.

The value of ϕ_{Bn} obtained from the analysis of $I(V_G)$ data is in good agreement with the one obtained from the $C(V_G)$ measurement plotted at height frequencies.

We note that increased temperature produces carrier thermal activation and thus, a creation in excess of free carriers $\Delta n = \Delta p$. This curve explain the increasing of parameters N_d and I_s and consequently the decrease of the serial resistance R_s.

References

[1] H. Morkoç, S. Strite, B. G. Gao, M. E. Lin, B. Sverdlov, M. Burns. J. Appl. Phys. **76**, 1363 (1994).
[2] M.A. Khan, A.R. Bhattarai, J.N. Kuznia, D.T. Olson, Appl. Phys. Lett. **63**, 1214 (1993).
[3] M.A. Khan, J.N. Kuznia, A.R. Bhattarai, D.T. Olson, Appl. Phys. Lett. **62**, 1786 (1993).
[4] M.A. Khan, J.N. Kuznia, D.T. Olson, M. Blasingame, A.R. Bhattarai, Appl. Phys. Lett. **63**, 2455 (1993).
[5] S. Nakamura, T. Mukai, M. Senoh, Appl. Phys. Lett. **64**, 28 (1994).
[6] J. Pankove, S. S. Chang, C. H. Lee, J. R. Molnar, D. T. Moustakas, B. Van Zeghbroeck, B 1994 IEDM 94-389.
[7] A.C. Schmitz, A.T. Ping, M.A. Khan, Q. Chen, J.W. Yang, I. Adesida, Semicond.Sci.Technol. **11**, 1464 (1996).
[8] Lei Wang, M. I. Nathan, Appl. Phys. Lett. **68**, 1267 (1996).
[9] A. Singh Solid state electronics, **26**, 815 (1983).
[10] H.C. Card, E. Rhoderik, J. appl. phys. **4**, 1589 (1971).
[11] F. Pandovani, R. Stratton Solid-State Electronics, **9**, 695 (1966).
[12] C. Crowel, V. Rideout Solid-State Electronics, **12**, 89 (1969).
[13] S. Fonash, J. appl. phys., **54**, 1966 (1983).
[14] I. Balberg, J. appl. Phys., **58**, 2603 (1985).
[15] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. (Wiley, New york, 1981), 245.
[16] B. B. Kosicki, R. J. Powell, J. E. Burgiel, Phys. Rev. Lett. 24, 1421 (1970).

*Corresponding author: mekki_2007@yahoo.fr