# Deep level investigation by capacitance and conductance transient spectroscopy in AlGaN/GaN/SiC HEMTs

M. GASSOUMI[a*], B. GRIMBERT[b], M. A. POISSON[c], J. FONTAINE[b], M. A. ZAIDI[a], C. GAQUIERE[b], H. MAAREF[a]
[a]*Laboratoire de Physique des Semiconducteurs et des Composants Electroniques Faculté´ des Sciences de Monastir, Avenue de l'environnement 5000 Monastir, Tunisie*
[b]*Institut d'Electronique de Microélectronique et de Nanotechnologie IEMN (TIGER), Département hyperfréquences et Semiconducteurs, Université des Sciences et Technologies de Lille, Avenue Poincaré, 59652 Villeneuve d'Ascq Cedex, France*
[c]*Alcatel-Thales III-V Lab, Route de Nozay, Marcoussis 91460, France*

Deep centers in AlGaN/GaN high electron mobility transistors (HEMTs) on SiC substrate have been characterized by capacitance deep level transient spectroscopy (DLTS) and conductance deep level transient spectroscopy (CDLTS). These measurements reveal the presence of three kinds of electron defects E1, E2 and E3 with activation energies of 0.52, 0.29 and 0.09eV, respectively and a hole-like trap HL1 with activation energy 0.905eV. The conductance DLTS using a gate pulse, shows an additional trap HL2, located at the surface. The localization and the identification of these traps are presented. Finally, these experimental results demonstrate the complementarities of these two techniques.

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*Keywords:* HEMT, DLTS, CDLTS, AlGaN/GaN, deep levels, surface traps.

## 1. Introduction

AlGaN/GaN HEMTs become the promising solid-state high power in high temperature and high frequency microwave devices thank to the high breakdown field and high carrier velocity of the GaN material[1-4]. Good results have been achieved during recent years in GaN based HEMTs[1-7]. In order to obtain the highest microwave performances of the wide band-gap devices, SiC is commonly chosen as the substrate of choice for its good thermal conductivity, small lattice mismatch and small thermal expansion coefficient difference with GaN[2,8]. Besides, a large number of layer structures and devices have been designed to improve the performance of these devices [1,8-10].

In the recent several years, the research on GaN HEMTs has attracted much attention and remarkable achievements have been made. However, there are still some problems unsolved in the production of GaN-based devices. The existence of dispersion effects observed in wide-bandgap devices has limited the initial expectations (power performances, reliability). The considerable list of advantages attributed to devices based on group-III nitrides in the last decade, due to their excellent properties, is partially limited by these negative effects.

The presence of trapping centers in AlGaN/GaN HEMTs, related to surface, material, and/or interface states, has been considered as the main cause of these effects [11, 12], already studied in other technologies. Some of the observed effects are threshold voltage shift [13,14], current collapse[15], reduction of short channel effect[14], light sensitivity[13], transconductance frequency dispersion, gate-lag and drain-lag transients[16], and limited microwave output power [16-17].

A number of research efforts have been directed toward identification and elimination of the trapping effects in AlGaN/GaN transistors. These studies have utilized several different characterization techniques, including photoionization spectroscopy[18]; drain leakage-current measurements[19], transient drain current measurements at different temperatures[20], current-mode deep level transient spectroscopy (DLTS)[21], and capacitance mode DLTS. In the present investigation, we have employed conductance and capacitance deep level transient spectroscopy modes (CDLTS and DLTS respectively).

In this paper, we summarize results obtained by Conductance (CDLTS) and (DLTS) deep level transient spectroscopy. Finally, the complementarity of these two techniques is presented.

## 2. Experimental

The layer used in this study was grown by metal-organic chemical vapour deposition (MOCVD) on SiC substrate. The epitaxial layer structure contains an AlN nucleation layer 1µm of GaN buffer, 5 nm AlGaN undoped, 20nm AlGaN Si doped $5\times10^{17} cm^{-3}$ followed by 5nm of AlGaN undoped capped by 1nm of GaN. The Al mole fraction in all AlGaN layers was nominally 22%. The device processing consisted of mesa isolation using ECR-RIE followed by ohmic and Schottky metallisations. Ohmic contacts were prepared by evaporating Ti/Al/Ni/Au multilayer and rapid-thermal annealing at 850°C in an $N_2$ atmosphere for 30 s. The ohmic contact resistance of $0.2-0.4\,\Omega\,mm$ was measured on TLM patterns. The Schottky contacts consisted of a thick Ni layer covered by Au layer and patterned by e-beam lithography. The ideality factor of this contact is 1.8 associated with a $\Phi_B$ of 0.8eV. The devices studied had gate width of $100\mu m$.

The drain source current transient was recorded using a numerical multimeter (HP 34401 A) and then, was treated numerically using the Lang method as in classical capacitance DLTS[48]. The measurements were carried out between 77K and 600K in a nitrogen cooled cryostat.

## 3. Results and discussions

### 3.1. Static measurements

Drain-source current voltage (Ids–Vds–T) measurements as a function of gate voltage and temperature have been performed. Output characteristics registered at different temperatures show several parasitic effects. The gate negative voltage Vgs was increased in order to pinch-off the channel (0to -5V) and to open (-5V to 0V). Immediately after, the measurement is done again; we observed a large decrease of the drain current for the second measurements. An example of this degradation of drain current at 250K is given in Fig. 1. We have reproduced the same measurements on the same sample for a higher temperature (450K). We have observed that drain current degradation gets progressively reduced, and it has almost disappeared (Fig. 2 and 3). This behavior confirms that we are in the case of a thermally activated effect. A possible explanation of this degradation in current is the presence of deep levels in the barrier layer under the gate metal, or deep levels at the interface and/or in the buffer layer and surface states.

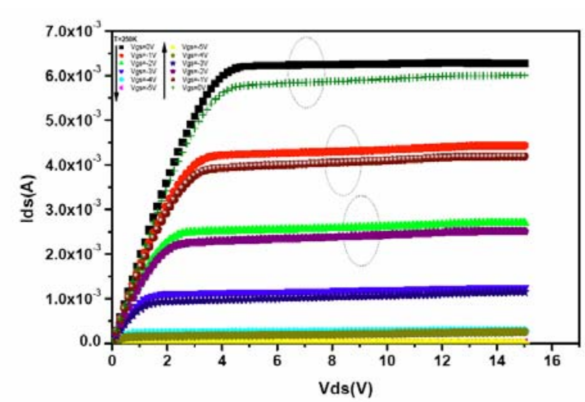


*Fig 1. Typical DC (Ids-Vds) characteristics at T=250K, the gate bias has been first increased from 0V to -5V and then decreased from -5V to 0V.*

Whereas the output characteristics at 300K are nearly ideal (Fig. 2), at 450K a spectacular variation of the output conductance is noted, known as kink effect. It consists of a rapid increase of the drain current in the saturation region for a given value of drain voltage ($V_{kink}$). This increasing in drain current induces an increase in the drain/source output conductance ($g_{ds}$) and a decrease in the microwave power gain.

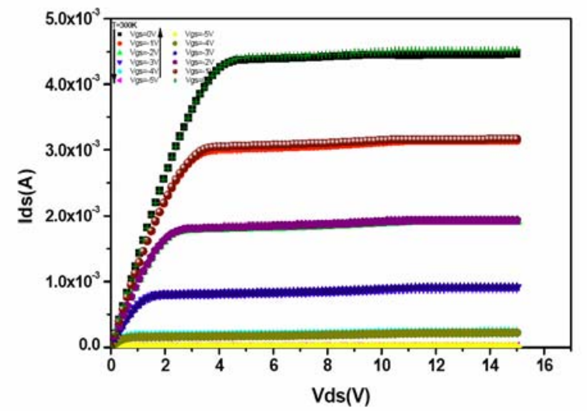


*Fig 2. Typical DC (Ids-Vds) characteristics at T=300K, the gate bias has been first increased from 0V to -5V and then decreased from -5V to 0V.*

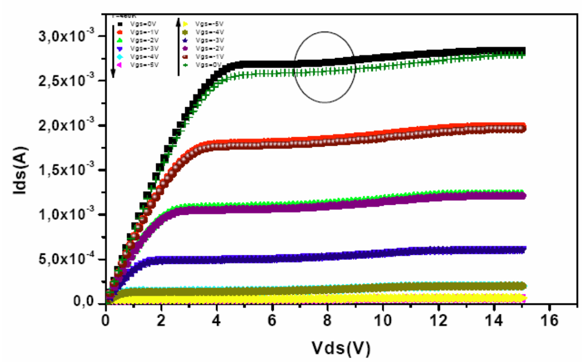


*Fig 3. Typical DC (Ids-Vds) characteristics at T=450K, the gate bias has been first increased from 0V to -5V and then decreased from -5V to 0V.*

This gives us a hint that the kink effect were attributed to impact ionization coupled either with traps in the structure[47], and trapping/detrapping phenomena on these centers change the charge density near the surface. Like on AlGaAs/GaAs HEMT and in III–V FETs, conductance dispersion is generally attributed to surface states or to deep level[22-24]. The origin of this effect, however, is not as yet clear.

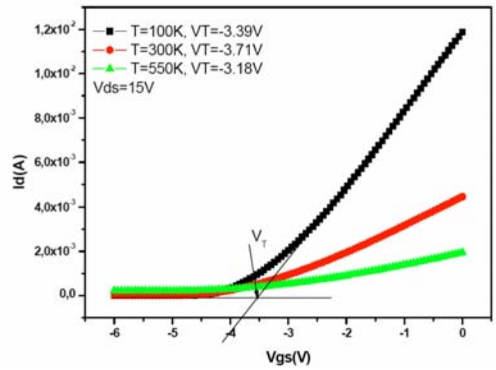


*Fig 4. Id-Vgs characteristics at T=100K, T=300K and T=550K with Vds= 15V*

As a conclusion on these first investigations, the drift on drain current characteristics presented above can be explained by the presence of deep defects near the Substrate/channel interface[25].

Another parasitic effect is the threshold voltage shift with temperature. As displayed in Fig. 4, the threshold voltage is -3.39 V at T=100K, -3.71 V at T =300K and -3.18 V at T =550K. This shift is thought to be caused by deep levels associated with electrically active defects in the heterostructures.

In order to study the origin of these different parasitic effects in the output characteristics, we have performed capacitance (DLTS) and conductance deep level transient spectroscopy (CDLTS).

### 3.2 Capacitance and conductance deep level transient spectroscopy

DLTS measurements were performed at temperature between 77K and 600K using boxcar technique. The modulation of the space charge region under the gate induced by DLTS allows to investigate the traps in the barrier layer. The capacitance DLTS spectrum (Fig.5) reveals the presence of three positive peaks, corresponding to electron emission from different traps called E1, E2 and E3, a one negative peak corresponding to hole-like trap called HL1.

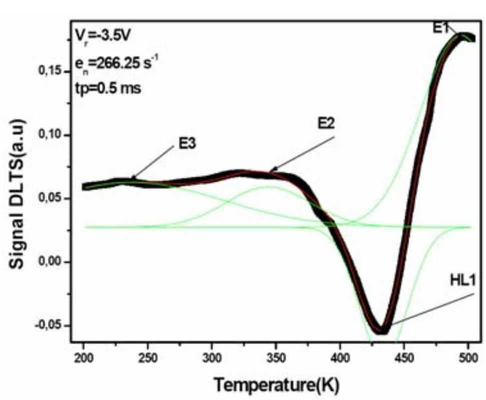


*Fig 5. A typical DLTS spectrum showing the presence of four levels.*

The apparent activation energies and capture cross-sections are deduced from the Arrhenius plot of $\ln\left(T^2/e_n\right)$ versus $1000/T$ (Fig. 6).

A comparison of the obtained an activation energies with the ones reported in the literature allows us to relate undoubtedly the electron trap E1. This trap (also labelled B, E05 or A5 in the literature) tends to be the most prominent electron trap observable by DLTS in n-type GaN[26-33]. Hacke et al.[34] and Haase et al.[35] assigned this trap to the nitrogen antisite point defect, $N_{Ga}$, on the grounds of the results of tight-binding calculations determining the deep donor level of $N_{Ga}$ at EC − 0.54 eV[36]. More recent results by Chung et al.[37], showing that the E1 trap concentration could be effectively suppressed by In doping, support this assignment since isoelectronic In atoms, occupying vacant Ga sites in the GaN crystal lattice during the growth, result in a lowering the density of Ga vacancy-related defects. However, several authors revealed that the E1 traps displayed the logarithmic capture kinetics [38] and that their concentration increased with the increase of dislocation density[39], and concluded that the traps were associated with dislocations themselves or were created during the dislocation generation process.

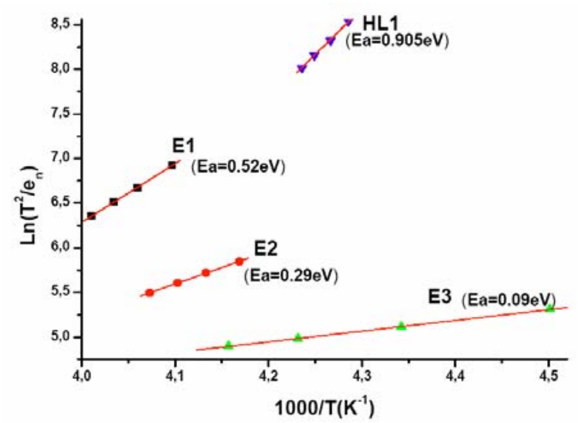


*Fig 6. Arrhenius plot for the deep levels observed in the AlGaN/GaN/SiC HEMTs.*

The hole-like trap signal HL1 appearing around $T = 432K$ has been investigated by Gassoumi et al using CDLTS under gate pulse when Vgs switching from 0V to -2V at Vds=4.5V [25] (Fig. 7 and Fig.8). Polyakov et al.[40] have shown recently the existence of hole-like traps. They suggested that this centre is the deep acceptor responsible for the donor–acceptor pair and yellow luminescence band in GaN[41]. As to the origin of this hole trap, consider the following: several authors have reported the presence of a deep hole trap between 0.75 and 0.9 eV above the valence band [42]. The origin of this defect, however, is not as yet clear.

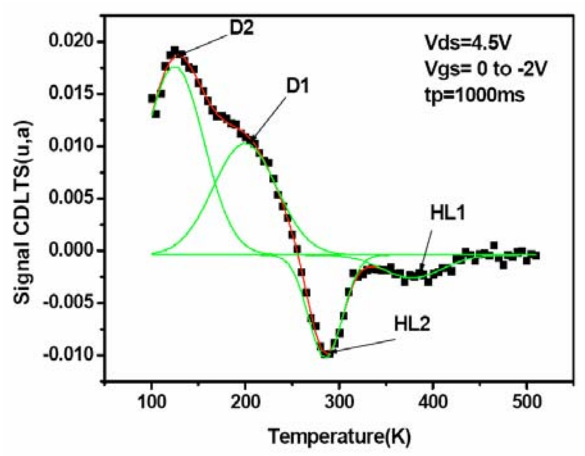


*Fig 7. A typical CDLTS spectrum showing the presence of four levels under a gate pulse.*

The electron traps E2 with an activation energy of 0.29eV and a cross section of $4.1\times10^{-17}cm^2$ can be attributed to the defect level with activation energy of 0.26eV reported by Hacke et al.[43] and 0.18eV reported by Götz et al.[44]. The very close correspondence between the Arrhenius plots for these levels and the similar activation energies derived from these plots suggest that they correspond to the same defect level. Marso et al.[45], Gassoumi have also observed a defect with similar signature in AlGaN/GaN/Si HEMT and have shown that this trap is located in the region below the 2DEG channel[46].

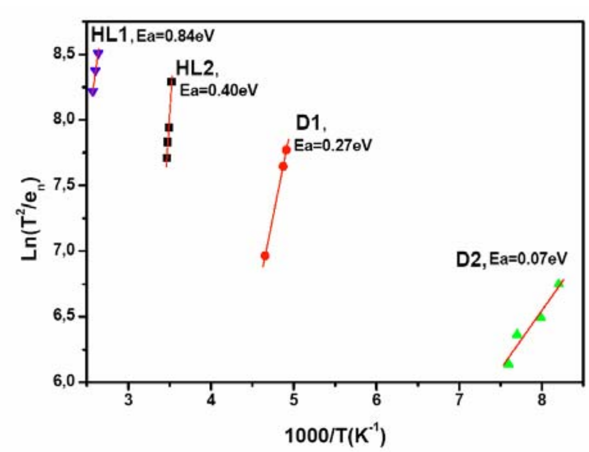


*Fig 8. Arrhenius plot for the deep levels observed in the AlGaN/GaN/SiC HEMTs under gate pulse.*

The microscopic nature of defect E3 is not clearly elucidated. Nevertheless, a level with close activation energy of 0.09 eV has been observed by CDLTS measurements and assigned to the N vacancy[46]. These defects are confirmed by conductance DLTS (CDLTS) technique under a gate pulse.

Hole-like trap (HL2) with activation energy 0.40 eV was observed with CDLTS. This defect may be located near the surface in the ungated region (between gate and drain). Indeed, I see neither by the classic DLTS nor by the measurement of the CDLTS under a drain-pulse.

## 4. Conclusion

The related deep levels in HEMT's were directly characterized by both capacitance and conductance Deep Level Transient Spectroscopy. Capacitance DLTS reveals three kinds of electron defects E1, E2 and E3, with an activation energy of 0.52, 0.29 and 0.09 eV, respectively and one hol-like trap HL1 with an activation energy 0.905eV. The conductance DLTS using a gate pulse, when the device is biased closer to the threshold voltage, shows one additional trap,HL2, located at the surface.

This work has pointed out the complementarity and the consistency of DLTS and CDLTS techniques. These combined analyses make possible the detection and the location of AlGaN/GaN traps in HEMTs.

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## References

[1] Y.-F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, et al. IEEE Electron Dev Lett **25,** 117 (2004).
[2] Y. Okamoto, Y. Ando, K. Hataya, T. Nakayama, H. Miyamoto, T. Inoue, et al. IEEE Trans Microw Theory Tech **52,** 2536 (2004).
[3] X. L. Wang, C. M. Wang, G. X. Hu, J. X. Wang, J. P. Li. Phys Stat Sol (c) **3,** 607 (2006).
[4] A. Chini, R. Coffie, G. Meneghesso, E. Zanoni, D. Buttari, S. Heikman, et al. 2.1 A/mm current density AlGaN/GaN HEMT. Electron Lett **39**(7), 625 (2003).
[5] Okamoto Yasuhiro, Ando Yuji, Hataya Koji. IEEE Trans Electron Dev **51**(11), 2536 (2004).
[6] X. L. Wang, C. M. Wang, G. X. Hu, J. X. Wang, T. S. Chen, G. Jiao, et al. Sol- State Electron **49**,1387 (2005).
[7] X. L. Wang, C. M. Wang, G. X. Hu, J. X. Wang, J. X. Ran, C. B. Fang, et al. Sci China Ser F **48,** 808 (2005)
[8] L. Shen, S. Heikman, B. Moran, R. Coffie, N.-Q .Zhang, D. Buttari, et al. IEEE Electron Dev Lett **22**(10), 457 (2001).
[9] M. Miyoshi, H. Ishikawa, T. Egawa, K. Asai, M. Mouri, T. Shibata, et al. Appl Phys Lett **85**(10),1710 (2004).

[10] C. M. Wang, X. L. Wang, G. X. Hu, J. X. Wang, H. L. Xiao, J.P. Li. J Cryst Growth **289,** 415 (2006).
[11] M. A. Khan, M. S. Shur, Q. C. Chen, J. N. Kuznia. Electron. Lett., **30**(25), 2175 (1994).
[12] G. Verzellesi, R. Pierobon, F. Rampazzo, G. Meneghesso, A. Chini, U. K. Mishra, C. Canali, E. Zanoni. in IEDM Tech. Dig., Dec. 2002, pp. 689–692.
[13] G. Meneghesso, A. Chini, E. Zanoni, M. Manfredi, M. Pavesi, B. Boudart, C. Gaquiere. In IEDM Tech. Dig., Dec. 2000, pp. 389–392.
[14] Y. Hasumi, H. Kodera. Electron. Commun. Jpn., **85**(2), 18 (2002).
[15] S. C. Binari, P. B. Klein, T. E. Kazior. Proc. IEEE, **90**(6), 1048 (2002).
[16] W. Kruppa, S. C. Binari, K. Dovespike. Electron. Lett., **31**(22), 1951 (1995).
[17] S. C. Binari, K. Ikossi, J. A. Roussos,W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, R. L. Henry. IEEE Trans. Electron Devices, **48**(3), 465 (2001).
[18] P. B. Klei. J. Appl. Phys. **92**, 5498 (2002).
[19] S. Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo. Appl. Phys. Lett. **81**, 3073 (2002).
[20] O. Mitrofanov, M. Manfra, N. Weimann. Appl. Phys. Lett. **82**, 4361 (2002).
[21] A.P. Zhang, L.B. Rowland, E.B. Kaminsky, V. Tilak, J. C. Grande, J. Teetsov, A. Vertiatchikh, L. F. Eastman. J. Electron. Mater. **32**, 388 (2003).
[22] P.H. Ladbrooke, S.R. Blight. IEEE Trans. Electron Devices **35**, 257 (1988).
[23] K. J. Choi, J. Lee. IEEE Trans.Electron Devices **48**, 190 (2001).
[24] A. Paccagnella, C. Tedesco, C. Canali, A. Cetronio, C. Lanzieri. Electron. Lett. **28**(22), 2107 (1992).
[25] M. Gassoumi, J.M. Bluet, C. Gaquière, G. Guillot, H. Maaref. In Press, Corrected Proof, Available online 10 April 2007.
[26] H. K. Cho, K. S. Kim, C.-H. Hong, H. J. Lee, J. Cryst. Growth **223**, 38 (2001).
[27] Z.-Q. Fang, D. C. Look, L. Polenta, J. Phys.: Condens. Matter **14**, 13061 (2002).
[28] H. K. Cho, C.S. Kim, C.-H. Hong, J. Appl. Phys. **94**, 1485 (2003).
[29] C. B. Soh, S. J. Chua, H. F. Lim, D. Z. Chi, W. Liu, S. Tripathy, J. Phys.: Condens. Matter **16**, 6305 (2004).
[30] S. A. Goodman, F. D. Auret, F. K. Koschnick, J. M. Spaeth, B. Beaumont, P. Gibart, Mater. Sci. Eng. B **71**, 100 (2000).
[31] Z.-Q. Fang, D.C. Look, J. Jasinski, M. Benamara, Z. Liliental-Weber, R.J. Molnar, Appl. Phys. Lett. **78**, 332 (2001).
[32] A. Hierro, M. Hansen, J.J. Boeckl, L. Zhao, J. S. Speck, U. K. Mishra, S. P. DenBaars, S. A. Ringel, phys. stat. sol. (b) **228**, 937 (2001).
[33] O. A. Soltanovich, E. B. Yakimov, N. M. Shmidt, A. S. Usikov, W. V. Lundin, Physica B **340–342**, 479 (2003).
[34] P. Hacke, T. Detchprohm, K. Hiramatsu, N. Sawaki, K. Tadatomo, K. Miyake, J. Appl. Phys. **76**, 304(1994).
[35] D. Haase, M. Schmid, W. Kürner, A. Dörnen, V. Härle, F. Scholz, M. Burkard, H. Schweizer, Appl. Phys. Lett. **69**, 2525 (1996).
[36] D. W. Jenkins, J.D. Dow, Phys. Rev. B **39**, 3317 (1989).
[37] H. M. Chung, W. C. Chuang, Y. C. Pan, C. C. Tsai, M. C. Lee, W. H. Chen, W. K. Chen, C. I. Chiang, C. H. Lin, H. Chang, Appl. Phys. Lett. **76**, 897 (2000).
[38] D. V. Lang, Space-Charge Spectroscopy in Semiconductors, in: Topics in Applied Physics, edited by P. Bräunlich, Vol. 37 (Springer, Berlin, 1979), chap. 3, pp. 93–133.
[39] C. B. Soh, S. J. Chua, H. F. Lim, D. Z. Chi, W. Liu, S. Tripathy, J. Phys.: Condens. Matter **16**, 6305 (2004).
[40] Polyakov, et al. J. Appl. Phys. **84**(2), 870 (1998).
[41] T. Ogino, M. Aoki. Jpn. J. Appl. Phys. **19**, 2395 (1980).
[42] F. D. Auret, W. E. Meyer, L. Wu, M. Hayes, M. J. Legodi, B. Beaumont, P. Gibart. Phys. Status Solidi C: Conf. **1**(9), 2271 (2004).
[43] P. Hacke, H. Nakayama, T. Detechprohm, K. Hiramatus, N. Sawaki. Appl. Phys. Lett. **68**, 1362 (1996).
[44] W. Gôtz, N.M. Johnson, H. Amano, I. Akasaki. Appl. Phys. Lett. **65,** 463 (1994).
[45] M. Marso, M. Wolter, P. Javorka, P. Kordos, H. Lu¨ th. Appl. Phys. Lett. **82n**, 633 (2003).
[46] M. Gassoumi, J.M. Bluet, G. Guillot, C. Gaquière, H. Maaref. Materials Science and Engineering: C **28**(5-6), 787 (2008).
[47] C.-H. Lin, W.-K. Wang, P.-C. Lin, Y-J. Chang, Y.-J. Chen. IEEE,Electron Device Lett., **26**(10), 710 (2005).
[48] D. V. Lang. J. Appl. Phys. **45**, 3023 (1974).

*Corresponding author:gassoumimalek@yahoo.fr