Deep traps responsible for capacitance hysteresis in AlGaN/GaN FAT-HEMT's studied under the temperature effects

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Capacitance characteristics with voltage of AlGaN/GaN FAT-HEMTs on Si substrate are reported. From C-V curves we can extract the 2DEG sheet charge density versus the gate bias and the carrier distribution profile. An important problem facing nitride-based high power microwave electronics is the presence of deep levels and anomalies in AlGaN/GaN structure. The existence of the capacitance hysteresis can be explained by built-in strain effects and internal electric field effects (due to spontaneous and piezoelectric polarizations) at the AlGaN/GaN interface. Also, it is induced by the location of the continuum of interface trap states relative to the Fermi level. The related deep levels are directly characterized and extracted by Deep Level Transient Spectroscopy (DLTS) measurement that has been studied in previous work. The identification of this trap has occurred and a remarkable correlation between C-V characteristics, defects and hysteresis capacitance effects has been discussed.

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1. Introduction

During the last decades, GaN- based material attracting a great deal of interest, consisting of GaN, AlN, InN and their alloys, has become the basis of an advanced, microwave-power-device technology for a number of reasons. The wide band gap of GaN (3.4 eV) makes GaN-based devices relatively resistant to thermal carrier emission and interband tunneling [1-2]. Indeed GaN has a large breakdown biase voltage, a strong spontaneous and piezoelectric field as well as an excellent carrier transport [3] and good thermal conductivity (of 1.3 W/cm in comparison with 0.5W/cm of GaAs) [4]. As a result from the latter feature, a two-dimensional electron gas (2DEG) can be formed at the AlGaN/GaN heterointerface with relatively high densities even without doping intentionally the barriers. These superior properties of GaN area adequate for high power amplifications [5-6]. The existence of such a high 2-DEG, makes the development of GaN-based high electron mobility transistors (HEMTs) very interesting for high temperature electronics, excellent high-frequency, high-power performance and high power microwave applications have been achieved with GaN based HEMTs [7-8]. In fact, AlGaN/GaN high electron mobility transistors (HEMTs) have been a subject of intense recent investigation and have emerged as attractive candidates for their ability to operate a high-power level and in a high-temperature environment [9]. On the other hand, for some applications, the use of Si as a substrate is revealed efficient to elaborate HEMTs with a low cost and an accurate integrating. In addition, the FAT-HEMT can operate in environments under huge temperature variations, so that they may be useful for space applications. Unfortunately, the mismatch of AlGaN is higher for Si, which leads to a formation of defects in bulk and at the surfaces as well. Defects and impurities are, however, unavoidable and hence can induce localized electronic states in the active layers. Most of them behave as trapping centers, leading to a limitation of the devices' performance. Nevertheless, some reliability issues related with defects and traps are not fully understood and solved yet, such as the hysteresis effect. The problems related to trapping are attributed responsibility for anomalies such as hysteresis in capacitance-voltage C-V characteristics. Hysteresis capacitance effect is a detrimental phenomenon for the FET performance. This anomalous is resulting from the presence of the trapping and de-trapping mechanism of deep centers thermally activated in the transistor [10]. Thus, an understanding of defects and anomalies in these structures is essential for improving materials quality and consequently, device performances. It is very important to understand this behavior in order to fully investigate the device at high temperatures.

The present work reports on an investigation performed by capacitance–voltage (C–V) measurements on AlGaN/GaN FAT-HEMT structures. Therefore, C-V measurements allow determining the 2D sheet charge density and the carrier distribution profile. We will report the hysteresis effects observed in capacitance characteristics of GaN-based HEMT on Si substrate. Consequently, for further improvement of AlGaN/GaN FAT-HEMTs it is crucial to investigate the electrical

active defects present in the structure and required to understand the origin of the hysteresis capacitance effect in order to overcome its degrading limitations. An attempt to correlate all of the results has been made in order to explain the origin of the hysteresis effect. The paper is organized as follows. The first section is dedicated to an introduction. As for the section II, it will compromise a sample elaboration. In section III, we present results and discussion. Conclusions are summarized in the last section IV.

2. Sample description

The AlGaN/GaN FAT-HEMT investigated is grown on a resistive silicon (111) substrate (4000-10.000Ω cm) by using molecular beam epitaxy (MBE). The epilayer consists of 10 Å AlN nucleation layer which can reduce the constraints and limit the quantity of dislocation, followed by a 2µm of unintentionally doped (Uid) GaN a 30 nm $Al_{0.25}GaN_{0.75}$ barrier layer, and a 5nm $Al_{0.25}Ga_{0.75}N$ spacer layer. On the top, a 1nm GaN cap layer is grown to ensure the Ohmic contact. The device processing is made following conventional FAT-HEMT fabrication steps. Hereafter, the metallization by means of evaporated 12/200/10/100 nm Ti/Al/Ni/Au is deposited at 850°C during 30s in N_2 ambient. A pre-treatment of the Ohmic contact area is performed prior to Ti/Al/Ni/Au metallization. The Schottky gate is realized using 100/150nm Ni/Au layers. Overlay metallization on the Ohmic contacts and measurement pads are also deposited during gate formation. The device had a gate width of 250 µm, a gate length of 200µm and spacing between gate-source and gate-drain of 2 µm. The shematic cross section of the $Al_{0.25}Ga_{0.75}N$/GaN/Si FAT-HEMTs is showns in the Fig.1. Measurements were performed using a PAR 410 capacitance meter and multi meter recorded in the 80-325K temperature range.

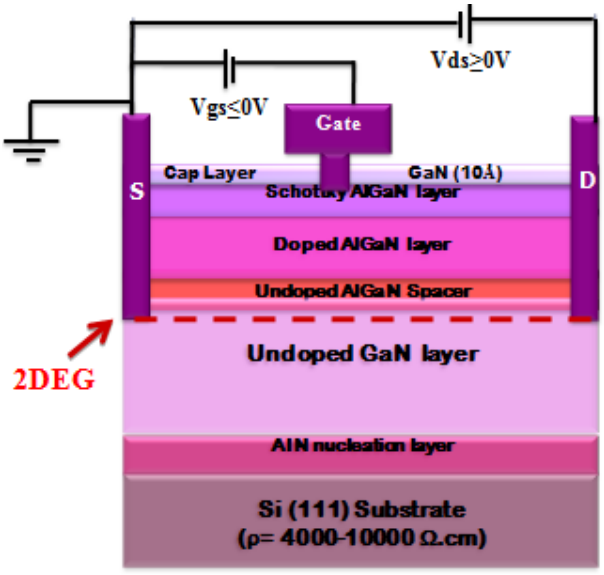

Fig. 1. Schematic diagram of $Al_{0.25}Ga_{0.75}N$/GaN FAT-HEMTs on Silicon substrates.

3. Results and discussion

3.1 Static measurements in Capacitance-Voltage characteristics

The Capacitance-Voltage (C-V) measurement is a powerful method for studying the fixed charges in metal-semiconductor structures and extracting the parameters for semiconductor heterostructures. This measurement has been further developed to investigate the presence of anomalies, its localization and distribution in AlGaN/GaN/Si FAT-HEMT heterostructures. This kind of large schottky area geometry was chosen because the measured capacitance is greater than that of transistors with low gate length. In order to validate the presence of a two-dimensional electron gas (2-DEG), we took C-V measurements using a capacitance meter of 1MHz frequency, which is represented in the inset Fig.2. At room temperature, the experimental built-in potential V_b determined by C-V measurements and found to be about 0.9 eV. The doping concentration N_D obtained from the same measurements is found to be equal to $N_D=4.4010^{19}cm^{-3}$. Furthermore, C (V) measurements allow estimating the values of the voltage applied and the reverse bias required in DLTS measurement. Experiment details are presented in previous work by M. Charfeddine et al. [11].

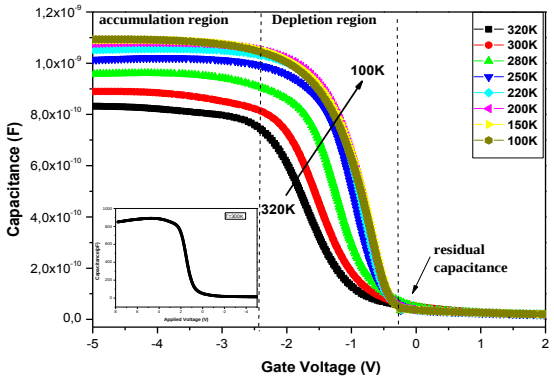

Fig.2. The C-V characteristics of the AlGaN/GaN/Si FAT-HEMTs measured at temperatures ranging from 100K to 320K.

In the present work, measurements of capacitance versus voltage of Schottky junction (Ni/Au)/AlGaN/GaN/Si at a temperature ranging from 100K to 320K are carried out in order to display the maximum space charge area and to determine the existence and location of thermally activated traps [12-14]. From the Fig.2, we shows that **(i):** the capacitance is flat at large reverse biases in the depletion region, due to only small changes in the 2DEG peak depth, and then decreases rapidly, depending on temperature, as the 2DEG is pinched off voltage **(ii):** as V_p (further increases, say to V_p=0.5V, the capacitance reduces to a constant parasitic value, independent of temperature **(iii):** for a gate voltage $|V_{gs}|$ greater than the pinched-off voltage. We observe an unusual behavior. Indeed, the maximal value of the

capacitance depends on the temperature. Furthermore, the shift on the C-V characteristics due to the temperature variation is noticeable in the range 250-320K (with increasing voltages) (Fig.2). However, when T<250K, the temperature has a small effect on the C-V characteristics and **(iiii):** the capacity shift to low gate-to source voltages (in the arrow direction) when it cooled (Fig.3). According to Miczek et al. [15-16], this shift towards higher voltages reflects the crossing Fermi level with a deep donor level, since the shift is little floating. This donor level is a shallow level or superficial level contribution to the conduction band.

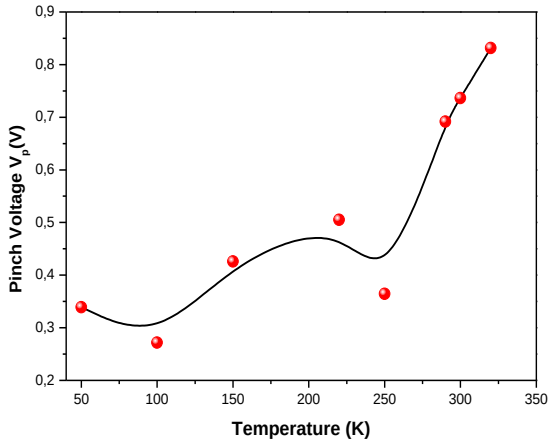

Fig.3. Evolution the pinch-off versus temperature for the Ni/Au/AlGaN/GaN/Si FAT- HEMT Schottky junction.

On the other hand, the density of charge depleted in AlGaN/GaN $N_s(V_{gs})$ for different temperatures and the carrier distribution profile $N_{C\text{-}V}(x)$ can be extracted using C-V plots according to the relation:

$$N_S(CV) = \frac{1}{q.S}\int_{Vgs=Vp}^{Vgs}\left(C_{mesurée} - C_{parasite}\right)dV_{gs} \quad \text{Eq. (I)}$$

$$and \qquad x(CV) = \frac{\varepsilon S}{C_{measured} - C_{parasitic}} \quad \text{Eq. (II)}$$

$$\Rightarrow N_{c-V}(x) = \frac{1}{\frac{d\,(1/(C_{measured} - C_{parasitic})^2)}{2.dV}\varepsilon.S^2.q} \quad Eq.(III)$$

Where S is the surface of the Schottky contact, ε is the dielectric constant, x represents the AlGaN barrier layer depth until interface AlGaN /GaN HEMT structure and q is the electronic charge. The results are plotted in Fig.4 according to Eq. (I). It exhibits the linear evolution of the sheet carrier concentration Ns as a function of the gate bias V_{gs} in the temperature ranging from 50 to 320K. The slope of Ns-Vgs can be approximated by $\varepsilon_{AlGaN}/d_{AlGaN}$. The important value of this curve is the 2DEG sheet concentration for V_{gs} equal to 2.5V, is obtained by 1.334 x 10^{17} e/m^2. As can be seen, the Ns densities decreases when increases the temperature (on heating). The reason for decreased 2DEG sheet density is the following **(i):** built-in strain effects and internal electric field effects (due to spontaneous and piezoelectric polarizations) that control the 2DEG. **(ii):** the electrons trapping by deep centers are thermally activated. **(iii):** the slope of the Ns-Vgs plots corresponds to the gate capacitance. This last is more sensitive to the temperature. **(iiii):** However, for T=300K, the slope of the Ns-Vgs equal to 6.37x 10^{16}e/m^{2}V^{-1}. While for T=100K, the slope is 9.103x 10^{16} e/m^{2}V^{-1}. This reveals that: low temperatures are promising to achieve significant 2DEG densities, when there are not thermal activated electrons.

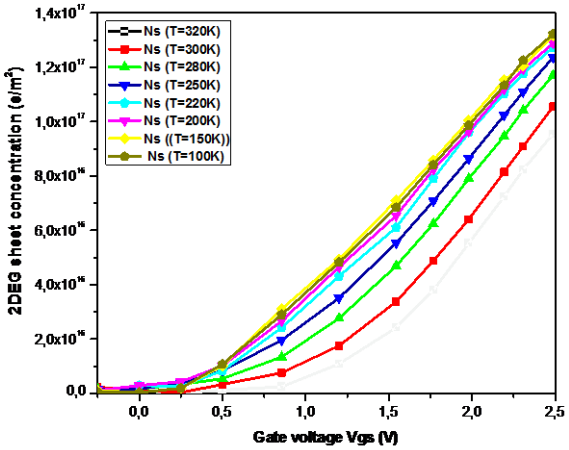

Fig. 4. The 2D Sheet charge density in an AlGaN/GaN/Si FAT – HEMT versus the gate bias for different temperatures.

Acording to Eq. (II) and Eq. (III) we can plot the carrier distribution profile. Fig.5 shows that: the carriers are mostly located at 329Å from the surface corresponding to 2DEG density at the AlGaN/GaN heterostructures. Also, it is possible to get an idea of residual doping in the GaN channel (< 1.10^{20} e/m^3) and we find that the carrier density decreases gradually when moving away from the interface, illustrating the insulating character of the buffer.

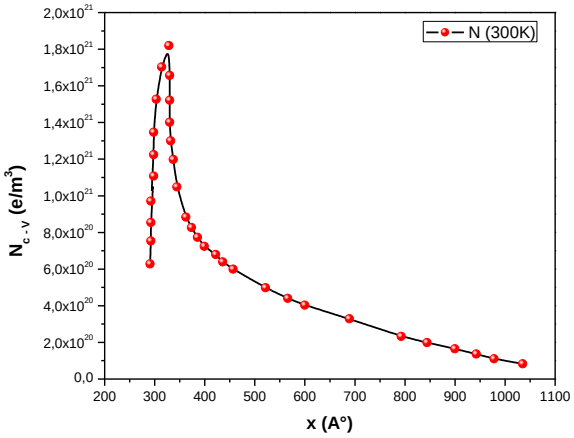

Fig.5. The carrier distribution profile.

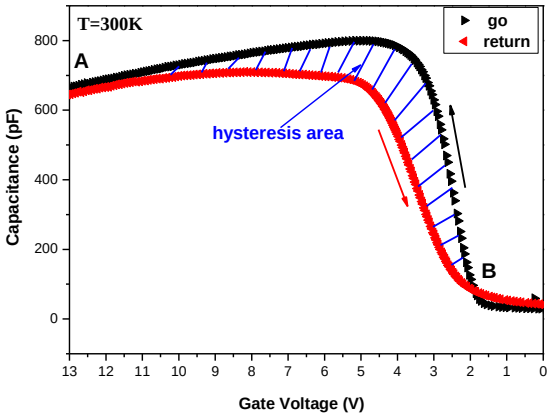

Fig. 6. The hysteresis observed in the capacitance-voltage (C-V) characteristics on AlGaN/GaN/Si FAT-HEMTs by sweeping from 4 to 0 V and back to 4 V.

3.2 The hysteresis capacitance effects

Capacitance-Voltage hysteresis was measured in the heterostructure have been performed after voltage application at the gate of the component. An example is given to 300K and the directions of the voltage sweep are shown in Fig. 6. The observed anomaly is an undesirable effect. It is considered as a response delay in Capacitance-Voltage. The parasitic effect is characterized by a shift and large variation of the Capacitance–Voltage by sweeping from 12 to 0 V and back to 12V. The C-V curve shifts considerably toward positive voltages and this shift is well observed at room temperature. Fig.6 illustrates this phenomenon, and the amount of hysteresis (dashed area) is an indicator of an increase in negative charge integrated in the AlGaN barrier layer or GaN layer. This rate of negative charges accumulated could be attributed to the presence of defects favoring injection of electrons from the gate in the barrier layer through a tunneling mechanism assisted by defects, for high reverse bias electrons. With increasing temperature of the devices up to 300K, C-V hysteresis curves tend to disappear gradually, and the electrons captured by deep traps are re-issued [17]. So three combined effects which are responsible for the hysteresis effects which are: the very thermodynamically unstable nature of the 2DEG induced built-in strain effects, internal electric field effects (due to spontaneous and piezoelectric polarizations) and the existence of defects.

Now, we will investigate this phenomenon for different temperatures at a frequency of 1 MHz. It is characterized by a shift of the C–V curve when the gate voltage V_{gs} varies in one way and then back for each temperature. This shift is well observed becomes more important when the temperature (T=300K), whereas at 100K it is totally absent. This behavior confirms that we are in the case of thermally activated defects responsible for shift capacity. Fig.7 illustrates this degradation in capacitance hysteresis versus the voltage for various temperatures. Compared to the Fig.1 the shift on the hysteresis characteristics due to the temperature variation is noticeable in the range 200-300K with decreasing voltages and are they different from those of Fig. 2. This direction change of the bias recording may be explained by the presence of deep levels in the structure which causes the non-equilibrium seen by the evolution of the hysteresis effect with temperature. The deep levels may limit the performances of FAT-HEMT transistors.

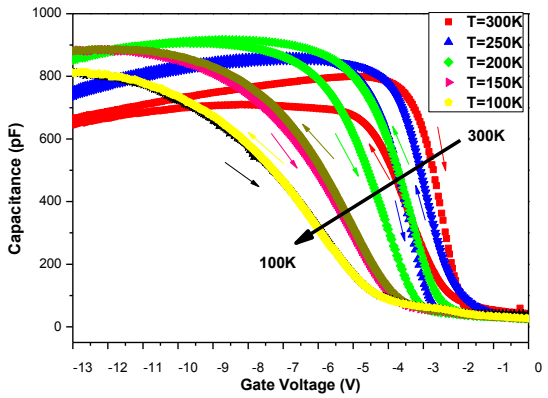

Fig.7. Typical C–V hysteresis curves, measured at a temperature range of 100-300K on AlGaN/GaN/Si FAT-HEMTs. The bias was swept forth and back from 12 to 0 V and back to 12V.

We define the points A and B (Fig.6) for which the capacitance is independent of the sense of voltage variation. The hysteresis capacitance voltage ΔC is expressed as:

$$\Delta C = C_A - C_B$$

Fig.8 shows the hysteresis capacitance variation ΔC versus the temperatures. We observed a sudden rise in the capacitance at a certain specific temperature, whereas it seems to be decreases at 250K and in the order of 300K. A possible explanation of this large variation in capacitance it is that **(i):** the temperature has an influence on the defects found **(ii):** the reduction in capacity is probably due to a Fermi level- defect crossing.

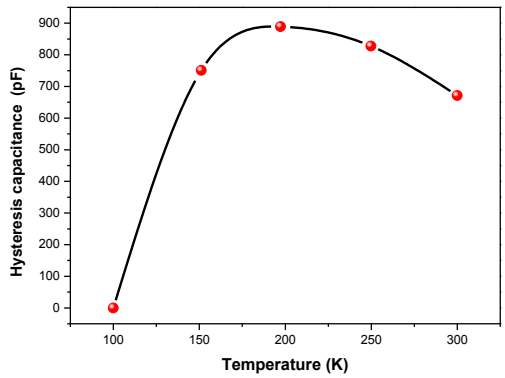

Fig.8. The variation of the capacitance hysteresis as a function of temperature on AlGaN/GaN/Si FAT-HEMTs.

To understand the evolution of the hysteresis phenomena as function of the temperature, we have determined the hysteresis area at each temperature (from 100K to 300K). Fig.9 reveals that: the C-V hysteresis area increases proportionally with the temperature. According to the temperature range measured, we confirmed that the trap generation leads to an obvious hysteresis effect at a temperature about 300K. This leads us to consider that this phenomenon is probably caused by the presence of defects activated around this temperature.

Many studies of the hysteresis effect in AlGaN/GaN HEMT transistors have been reported, but due to its complex behavior, the exact location of the traps involved is still unclear (the buffer, the barrier, or the surface of the transistor), and depends on the device. Some studies have attributed to electrons tunneling from the Schottky gate to localized states in the structure [18]. Byrum et al. [1], have been attributed hysteresis capacitance to the charges accumulation at the hetero-interface when the energy states of vacant spaces in Nitrogen (N) and/or a donor level located just above the Fermi level. The condition for the step of capacity is similar to the hysteresis capacitance. These impurities can be incorporated into the hetero-structure AlGaN/GaN during the growth process. As reported by Chikhaoui et al. [17], this phenomenon indicates an increase in the built-in negative charge, either in the AlGaN barrier or in the GaN layer. From the calculated and experimental C-V characteristics, C.Mizue et al. [19], found that the charging and discharging of interface states near the AlGaN conduction-band edge mainly the cause of stretch- out and the appearance of the hysteresis capacity effect. This phenomenon is attenuated by the addition of an oxide layer such as Al_2O_3 between the metal and the AlGaN layer which prevents the electrons to cross the barrier.

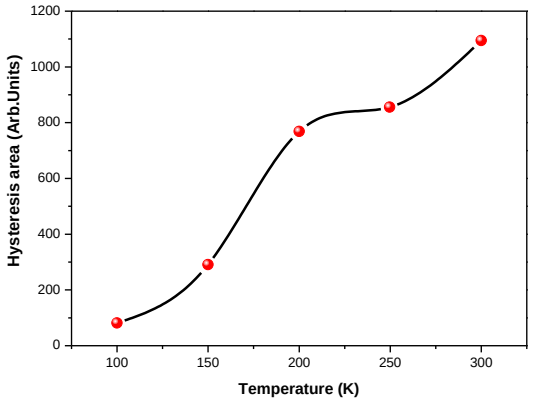

Fig.9. C–V hysteresis area as a function of temperature on AlGaN/GaN/Si FAT-HEMTs.

This phenomenon has been studied by drain source current–voltage characteristics and from other techniques such as a technique labeled “reverse” deep level transient spectroscopy was used to show that the deep traps responsible for the hysteresis. As reported by M.M. Ben Salem et al. [20], have been established a link between kink and hysteresis effects when we attribute this effect to the presence of a defect in the transistor. I_{ds}–V_{ds} measurements have shown the presence of hysteresis effect in the device. This idea is supported by M.Gassoumi et al. [10], who claims that hysteresis effect is caused to the presence of traps in HEMTs structure by using drain-source current voltage (I_{ds}–V_{ds}–T) measurements as a function of gate voltage and temperature have been performed. This delayed response can be attributed to the phenomenon of trapping and detrapping deep centers located near the surface of the channel. Nakajima et al. [21], showed this effect can be accounted for a delay of I_{ds} answer that should be attributed to trapping and detrapping of deep centers near the surface states of channel. Another suggestion is presented by S.Bouzgarou et al. [22], have correlated this effect with the presence of a dominant trap. This trap has been observed on this transistor by using CDLTS technique and qualifies this defect to parasitic hysteresis observed on the output characteristics.

In order to characterize, locate and identify defects could be present in the same FAT-HEMT component and responsible for the hysteresis capacitance effect mentioned. Deep Level Transient Spectroscopy (DLTS) measurements have been carried out on the FAT-HEMT transistors by M. Charfeddine et al. [11]. A detailed study

of deep levels using this technique has revealed several limiting phenomena associated in GaN technology, namely the Hysteresis effect.

The variation of the capacitance versus voltage (Fig.3) and the area separating the two go–return C−V curves (Fig.8), plotted as a function of temperature, prove the presence of defects is observed at a temperature in the order of 300 K. We can then attribute the traps responsible for hysteresis capacitance effects originated in our transistor by DLTS technique. It should be located in the AlGaN layer because the trap is only detects by using this technique. This direct correlation was the aim of our work and this relation between the DLTS technique and the hysteresis effect were confirmed in other experimental results [22, 23].

4. Conclusion

In summary, we have investigated Capacitance-Voltage measurements and defect analysis on AlGaN/GaN grown on Si substrate. From which we can validate the presence of the two dimensional electron–gas (2-DEG) and several parameters have been extracted. In fact, Capacitance–Voltage (C-V) and (C-V-T) characteristics show the apparition of anomalies: hysteresis capacitance effect. The relation between the hysteresis capacitance and existing deep centers has also been found. Comparison with the noticeable parasitic effect has been observed at a temperature ranging about 300K and a dominant trap has been proved by using Deep Level Transient Spectroscopy (DLTS) technique in the previous work. We can suggest that the defect is responsible to parasitic hysteresis effect observed on the capacitance- voltage characteristics.

References

[1] L. E. Byrum, G. Ariyawansa, R. C. Jayasinghe, N. Dietz, A. G. U. Perera, S. G. Matsik, I. T. Ferguson, A. Bezinger, H. C. Liu. Journal of Applied Physics, **105**, 023709 (2009).

[2] G. Ariyawansa, M. B. M. Rinzan, M. Strassburg, N. Dietz, A. G. U. Perera, S. G. Matsik, A. Asghar, I. T. Ferguson, H. Luo, H. C. Liu. Appl. Phys. Lett., **89**, 141122 (2006).

[3] H. Morkoç, Handbook of Nitride Semiconductors and devices (Wiley-VCH Berlin), **I-III,** (2008).

[4] P. Gangwani, S. Pandey, S.Haldar, M. Gupta, R. S. Gupta, Solid State Electronics, **51**, 130 (2007).

[5] O. Aktas, Z. F. Fan, A. Botchkarev, S. N. Mohammad, M. Roth, T. Jenkins, L. Kehias, H. Morkoc, IEEE Electron Device Lett., **18**(6), 293 (1997).

[6] C. Yong, C. Zhiqun, Y. Zhenchau, T. Wah, K. Lau, J. chein, IEEE Electron Device Lett., **28**(5), 328 (2007).

[7] X. L. Wang, T. S. Shen, H. L. Xiao, C. M. Wang, G. X. Hu, W. J. Luo, J. Tang, L. C. Guo, J. M. Li, Solid-State Electron., **58**, 926 (2008).

[8] D. Ducatteau, A. Minko, V. Hoël, E. Morvan, E. Delos, B Grimbert, H. Lahreche, P. Bove, C. Gaquière, J. C. De Jaeger, S. Delage, IEEE Electron Device Letters., **27**, 7 (2006).

[9] Y. Chang, K. Y. Tong C. Surya, Semicond. Sci. Technol., **20**, 188 (2005).

[10] M. Gassoumi, J. M. Bluet, G. Guillot, C. Gaquière, H. Maaref, Materials Science and Engineering C, **26**, 787 (2006).

[11] M. Charfeddine, M. Gassoumi, H. Mosbahi, C. Gaquiére, M. A. Zaidi, H. Maaref, Journal of Modern Physics, **2**, 1228 (2011).

[12] S. K. Jha, C. surya, K. J. Chen, K. M. Lau, E. Jelencovic, Solid State Electron, **52**, 606 (2008).

[13] B. Raeissi, J. Piscator, P. Engström, S. Hall, O. Buiu, M. C. Lemme, H. D. B. Gottlob, P. K. Hurley, K. Cherkaoui, H. J. Osten, Solid State Electron, **52**, 1274 (2008).

[14] L. Semra, A. Telia A.Soltani, Surf. Interface Anal., **42**, 799 (2010).

[15] M. Miczek, Ch. Mizue, T. Hashizume, B. Adamowicz J. Appl. Phys., **103,** 104510 (2008).

[16] M. Miczek, B. Adamowicz, Ch. Mizue, T. Hashizume, Japanese Journal of Applied Physics, **48**(4), 04C092 (2009).

[17] W. Chikhaoui, J M. Bluet, C. Bru-Chevallier, C. Dua, R. Aubry, Phys. Status Solidi C, **7**, 92 (2010).

[18] A. Y. Polyakov, N. B. Smirnov, A. V. Govorkov, A. V. Markov, A. M. Dabiran, A. M. Wowchak, A. V. Osinsky, B. Cui, P. P. Chow, S. J. Pearton, Appl. Phys. Lett., **91**, 69 (2007).

[19] Ch. Mizue, Y.Horio, M. Miczek, T. Hashizume Japanese Journal of Applied Physics, **50**, 021001 (2011).

[20] M. M. Ben Salem, S. Bouzgarrou, N. Sghaier, A. Kalboussi, A. Souifi, Materials Science and â Engineering B, **127,** 34 (2006).

[21] A. Nakajima, Sh. Yagi, M. Shimizu, K. Adachi, H. Okumura, Materials Science Forum, **556**, 1035 (2007).

[22] S. Bouzgarrou, Na. Sghaier, M. M. Ben Salem, A. Souifi, A. Kalboussi, Materials Science and Engineering C , **28**, 676 (2008).

[23] M. Tapajna, K. Cico, J, Kuzmik, D. Pogany, G .Pozzovivo, G .Strasser, J-F Carlin, N. Grandjean, K. Fröhlich, Semiconductor Science and Technology, **24**, 035008 (2009).

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