Effects of illumination on I-V, C-V and G/w-V characteristics of Au/n-CdTe Schottky barrier diodes

H. KANBUR*, Ş. ALTINDAL[a], T. MAMMADOV[a,b], Y. ŞAFAK[a]
[a]*Department of Physics, Faculty of Arts and Sciences, Gazi University, 06500 Ankara,Turkey*
Department of Physics, Faculty of Arts and Sciences, Bozok University, 66100 Yozgat,Turkey
[b]*National Academy of Science, Institute of Physics, Baku, Azerbaijan*

In order to interpret the effect of illumination on the electrical characteristics of Au/n-CdTe Schottky barrier diodes (SBDs) the forward and reverse bias current-voltage (I-V), capacitance-voltage (C-V), and conductance-voltage (G/w-V) characteristics of these SBDs have been investigated at room temperature using a tungsten lamp under both different illumination levels and in dark. Under illumination, both of the values of forward and reverse currents have increased with increasing illumination intensity. In the reverse bias, the change in current is higher than the forward bias at the same applied bias voltage. This behavior can be attributed that electron-hole pairs generate in the junction as a result of the light absorption. Experimental results show that both of the values of the capacitance and conductance have increased with increasing illumination levels and give the peaks at high illumination levels. The illumination process causes shifts in the capacitance-voltage (C-V) and conductance-voltage (*G*/w-V) curves towards forward bias and the shifts have increased with increasing illumination level. This behavior can be explained by the built-up of fixed charge between metal and semiconductor which is attributed to the changes in the number of interface states (N_{ss}) due to the illumination process. In addition, the series resistance (R_s) of diodes can significantly alter the *C-V* and *G* /w-V characteristics and decrease with increasing illumination level.

(Received November 3, 2010; accepted June 9, 2011)

Keywords: Au/CdTe, I-V/C-V characteristics, Illumination characteristics, Series resistance, Surface states.

1. Introduction

Cadmium telluride (CdTe) has gained considerable interest as one of the most promising II-VI semiconductors. CdTe is suitable materials for applications in electric and optoelectronic devices due to the direct band gap of 1.45 eV, high optical absorption coefficient, producting it reasonable mobility life time for both electrons and holes, and a variety of different techniques used for CdTe thin film deposition [1-6]. Metal/CdTe interfaces play an important role in optoelectronic devices such as infrared detectors and sensors in thermal imaging, solar cells etc. [2,3]. A clear understanding of the physical principles underlying the properties of these interfaces is therefore essential in order to develop practical devices based on this semiconductor material. The properties of charge transport have been investigated with Schottky devices and the dominant charge transport mechanisms in Au/CdTe SBDs have been identified as thermionic emission over the barrier, Poole-Frenkel, and space charge limited conduction [2-4,6]. The knowledge of the electrical properties of the barrier where photo-voltage is generated is important in the development and optimization of any photovoltaic device. In the past, interesting investigation of the metal/CdTe contacts were performed by using single crystal mechanism and by observing the effect of shunt and series resistance on the electrical characteristics of the polycrystalline CdTe devices [5].

The electronic of semiconductor materials are strongly affected by the presence of carrier trapping centers in the forbidden band gap. The exact nature of the interaction between photons and these traps is not clear, but it appears that the presence of photons, in some way, facilitates charge exchange between these defects and the CdTe bands. There dose not appear any to be no photon-induced damage, i.e. the device characteristics revert to in dark the results when the illumination is put off. In recent years, the C-V and G-V characteristics of metal-semiconductor (MS) or metal-insulator-semiconductor (MIS) Schottky diodes [7-16] and solar cells [17-25] have been investigated considering the N_{ss}, R_s and insulator layer effect. The series resistance R_s significantly alters the device C and G characteristics from their ideal behavior and makes the measured C and G strongly illumination dependent.

Many electron-hole pairs may be generated in the junction as a result of the light absorption. Illumination-generated these electrons either recombines with the holes are move out of interfacial insulator layer which is deposited or native. On other hand illumination-generated holes may diffuse in this interfacial insulator layer, but are less mobile than the electrons; many stationary hole traps are also present. Due the effect of illumination, the main diode parameters such as ideality factor (n), barrier height (Φ_B) at M/S interface, series resistance (R_s) of device, interface states (N_{ss}) near M/S interface and in the forbidden band gap may change under illumination. Therefore, under illumination forward and reverse bias I-

V, C-V and G/w-V characteristics provide an important property in solar cells and SBDs. In this study, the forward and reverse bias I-V, C-V and G/w-V measurements of Au/n-CdTe Schottky barrier diode (SBD) are performed in the dark and under illumination at room temperature. In order to achieve a better understanding, the effects of series resistance R_s on the C-V and G/w-V characteristics in the wide range of applied voltage were investigated. Experimental results show that both N_{ss} and R_s are important parameters that influence the electrical characteristics of SBD.

2. Experimental procedure

Epitaxial layers of CdTe were grown on monocrystalline CdTe (111) substrate by photostimulated vapor phase epitaxy (PSVPE). Approximately a 5 μm epitaxial layers were deposited at 650 ºC with a 350 μm/h growth rate. In the growth, Cd source temperature was kept at 350 ºC for control to stoichiometry while CdTe source temperature was 750 ºC [26,27]. By controlling stoichiometry, the growth prosess makes it possible to obtain *n*-type epitaxial layers of CdTe. For the fabrication process, the CdTe wafers were decreased for 5 min in boiling trichloroethylene, acetone and ethanol consecutively and then etched in a sequence of H_2SO_4 an H_2O_2, 20% HF, a solution of $6HNO_3$:1HF:$35H_2O$, 20% HF. Preceding each cleaning step, the wafer was rinsed thoroughly in deionized water of resistivity of 18 M Ω.cm. Immediately after surface cleaning, high purity gold (Au) metal (99.999 %) with a thickness of 1000 Å was thermally evaporated with a 2.2 Å/s grow rate onto the whole back surface of the wafers at a pressure of 10^{-8} mbar in a turbo molecular fitted vacuum coating system (Bestek Technique). To form ohmic contacts on the back surface of the wafer, we sintered the evaporated Au at 400 ^{o}C for 5 min in flowing dry nitrogen ambient at the rate of 2 l/min. After ohmic contact, circular dots of 1 mm in diameter and 1100 Å thick Au Schottky contacts (front rectifier contacts) were deposited onto CdTe surface in the same vacuum system. The metal thickness layer and the deposition rate were monitored with the help of quartz crystal thickness monitor. I-V measurements were performed by the use of a Keithley 220 programmable constant current source, a Keithley 614 electrometer. The C-V and G/w-V measurements were performed at 500 kHz by the using HP 4192A LF impedance analyzer (5 Hz-13 MHz). Small sinusoidal signal of 40 mV peak to peak from the external pulse generator is applied to the sample in other to meet the requirement [25]. All of the measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card. Also, resistivity and Hall measurements of the CdTe layers were carried out at room temperature by using Van der Pauw method (Lakeshore Hall effect measurement system). The values of the resistivity, Hall carrier concentration and Hall mobility were found 1.8 Ω cm, $2.17\text{x}10^{15}$ cm^{-3} and 1523 $cm^2\ V^{-1}\ s^{-1}$, respectively. Hall measurements indicated the films to be n-type.

3. Results and discussions

The forward and reverse bias I-V characteristics of Au/n-CdTe SBD have been investigated both in dark and under six different illuminations levels. The semi-logarithmic LnI-V curves of Au/n-CdTe SBD at room temperature are shown in Fig. 1. It can be seen in Fig. 1, each Ln (I)-V curve consists of a linear range with different slopes. In general, the relationship between the applied-bias voltage (V≥3 kT/q) and the current through a barrier between metal and semiconductor of the MS, MIS and solar cells, based on thermionic emission theory (TE), is given by [7,8,25]

$$I = I_o \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \qquad (1)$$

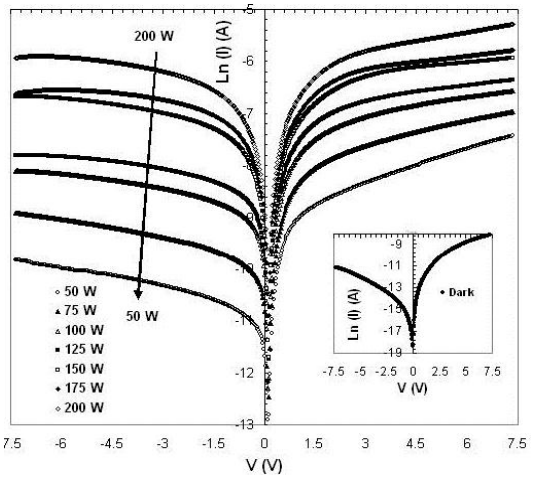

Fig. 1. Forward and reverse bias semilogarithmic LnI-V characteristics of Au/n-CdTe SBD in dark and under six illumination levels.

where *V* is the applied bias voltage on the SBD, n is an ideality factor and I_o is the reverse saturation current derived from the straight-line intercept of *LnI* at zero bias is given by

$$I_o = A\ A^*\ T^2 \exp\left(-\frac{q\Phi_{Bo}}{kT}\right) \qquad (2)$$

where Φ_{Bo} is the zero-bias barrier height, A is the rectifier contact area, A^* is the effective Richardson constant and equals to 12 A cm^{-2} K^{-2} for n-type CdTe, T is the absolute temperature in Kelvin and k is the Boltzmann constant. The ideality factor is calculated from the slope of the linear region of the forward bias *LnI-V* plot and can be written from Eq.(1) as

$$n = \frac{q}{kT}\left(\frac{dV}{dLnI}\right) \qquad (3)$$

where *dLnI/dV* is the slope of linear region of *LnI* vs *V* plots. The value of Φ_{Bo} is calculated from the extrapolated I_o at zero according to following equation as

$$\Phi_{Bo} = \frac{kT}{q} Ln\left(\frac{AA^{**}T^2}{I_o}\right) \quad (4)$$

The determined values of the I_o, n and Φ_{Bo} both in dark and under six illumination levels are given in Table 1. As can be seen in Table 1, the experimental values of I_o, Φ_{Bo} and n obtained from

Table 1. The values of various parameters for Au/n-CdTe SBD obtained from I-V data in dark and under six illumination levels.

Illumination Levels	I_o (A)	n	Φ_{Bo} (eV)	R_s (kΩ)	R_{sh} (kΩ)
Dark	$1.65x10^{-8}$	2.86	0.698	24.1	523.0
50 W	$8.21 x10^{-7}$	3.25	0.597	12.4	135.0
75 W	$1.75 x10^{-6}$	3.69	0.577	7.8	54.2
100 W	$4.61 x10^{-6}$	4.28	0.552	5.2	24.0
125 W	$6.40 x10^{-6}$	4.39	0.544	4.2	17.8
150 W	$8.74 x10^{-6}$	4.49	0.536	2.8	5.73
175 W	$1.40 x10^{-5}$	4.79	0.524	2.4	5.3
200 W	$2.16 x10^{-5}$	4.98	0.512	1.4	2.71

forward bias I-V data for the Au/n-CdTe SBD $1.65x10^{-8}$ A, 2.86 and 0.698 eV (in dark) to $2.16x10^{-5}$ A, 4.98 and 0.512 eV (under 200 W). It is clear that the n of Au/n-CdTe SBD is considerably larger than unity. These values of ideality factors show that the structures obey a MIS configuration rather than MS structure. The high value of ideality factor has been attributed to a native insulator layer at metal/semiconductor interface and particular distribution of interface states localized at semiconductor/insulator interface. Because the diode ideality factor greater than unity is generally attributed to the presence of a bias dependent Schottky barrier height, image forces lowering, generation-recombination or interface recombination, interface impurities, barrier inhomogenity and interfacial insulator layer [10,22,28-30]. Also the value of n and I_o increase with increasing illumination intensity can be attributed to illumination activates the interface recombination of photo-generated carriers [30]. As can be seen in Fig. 1, Ln(I)-V curves are linear on a semi-logarithmic scale at intermediate forward bias voltage region, but it deviates considerably from linearity at high forward bias voltages due to the effects of some factors such as series resistance, native interfacial insulator layer, a wide distribution of low BH patches and particular distribution of N_{ss} at M/S interface states, etc. [7-10]. When the value of R_s is significant, particularly in the downward curvature of the forward bias I-V plots, the value of N_{ss} is effective in both inversion and depletion regions and depletion range and their distribution profile changes from region to region in the band gap [8,22,24,25,28].

The bias voltage dependent series resistance profile of Au/n-CdTe SBD was obtained from the I-V data both in dark and under each illumination level using *Ohm Law* ($\delta V_i/\delta I_i$) and are given in Fig. 2. As can be shown in Fig. 2, at sufficiently high forward bias region (V≥4 V) the value of series resistance is almost independent from bias voltage. On the other hand the series resistance is independent of bias voltage for sufficiently high reverse bias region (V≤ -4 V), which is equal to the diode shunt resistance, R_{sh}. The value of R_s decreases with increasing illumination level in the voltage range measured and these changes are effective especially more significant at low forward bias and high reverse bias regions. It is well known the real series resistance of SBD is in the sufficiently high forward bias voltage. It is clear that the values of R_s and R_{sh} were found strongly dependent on the intensity of illumination level and applied bias voltage and decrease with the increasing illumination level. Such behavior of R_s and R_{sh} can be explained by the enhanced conductivity of the CdTe and it is an expected behavior.

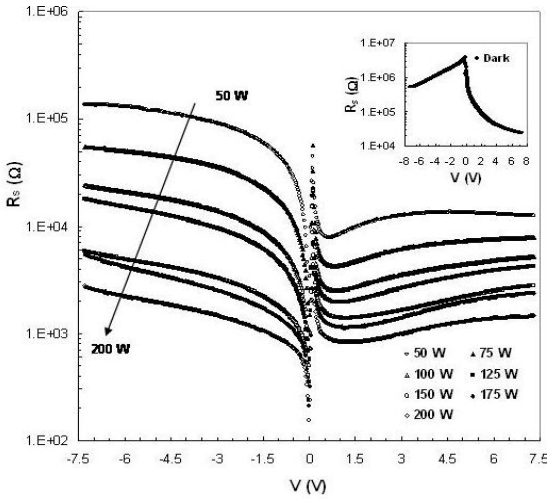

Fig. 2. The R_s vs V curves of Au/n-CdTe SBD in dark and under six illumination levels.

For SBDs with native or deposited interfacial insulator layer, the density distribution of the interface states (N_{ss}) in equilibrium with the semiconductor and the value of the ideality factor become greater than unity and can be expressed as [31].

$$n = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}\right] \quad (5)$$

where δ is the thickness of interfacial insulator layer, W_D is the width of the depletion layer calculated from C^{-2} vs V characteristics at 1 MHz. As shown in Table 1 the value of n increases with increasing illumination level due to increase in illumination induced interface states [31] as indicated by the relation in Eq. 5. It is clear that the main electrical parameters such as I_o, n, Φ_{Bo}, R_s and R_{sh} were found strongly dependent on the illumination levels and

while the values of I_o and n increase, Φ_{Bo}, R_s and R_{sh} have decreased with the increasing illumination level.

The *C-V* and *G/w-V* measurements of the Au/n-CdTe SBD carried out in dark and six illumination levels at room temperature and are given in Fig. 3. As shown in Fig.3, while the value of capacitance increases especially in the accumulation region, conductance increases in the inversion region. It is clear that the value of R_s is an important parameter to designate the noise ratio of device as dependent on illumination levels. There are several methods to extract the series resistance of MIS Schottky diode in the literature [24,25,32-35].

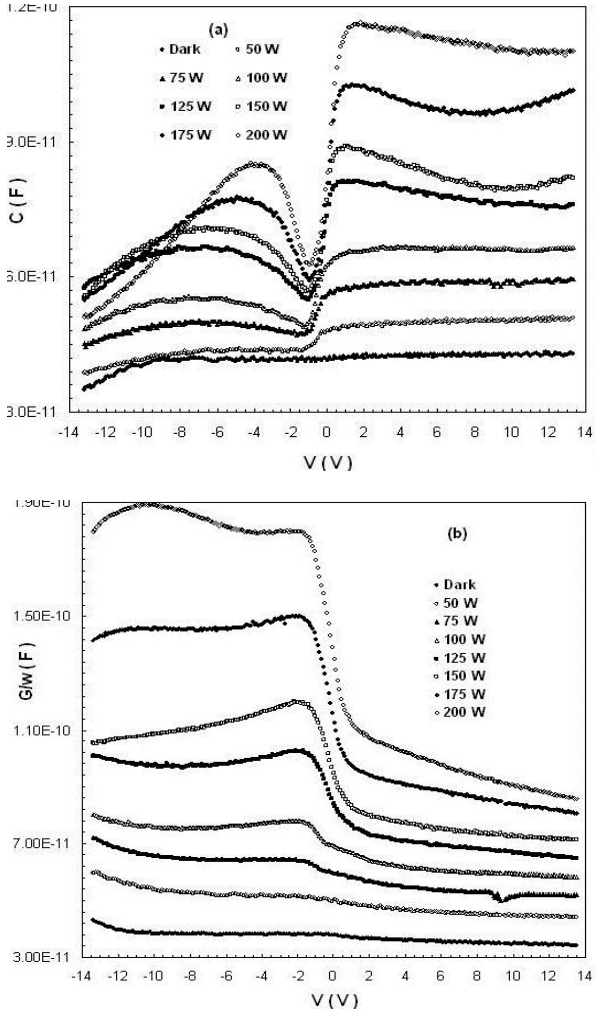

Fig. 3. (a) Measured capacitance C vs V curves (b) and conductance G/w vs V curves of Au/n-CdTe SBD in dark and under six illumination levels.

We have used the conductance method developed by Nicollian and Goetzberger [25]. The conductance technique [8,25,35] is based on the conductance losses resulting from the exchange of majority carriers between the interface states and majority carrier band of the semiconductor when a small ac signal is applied to MIS Schottky diodes [8,25].

The applied ac signal causes the Fermi level to oscillate about the mean positions governed by the dc bias, when the MIS Schottky diode is in the depletion. The real series resistance of MIS Schottky diodes can be subtracted from the measured capacitance (C_m) and conductance (G_m) in strong accumulation region at high frequency (f≥500 kHz) [25,34-36]. In addition, the series resistance which is dependent on voltage and illumination levels can be subtracted. Then, the admittance Y_{ma} is given by [8,9,24,25] .

$$Y_{ma} = G_{ma} + j\omega C_{ma} \tag{6}$$

Comparing the real and imaginary parts of the admittance, the series resistance of MOS and SBD structures are given by [25].

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{7}$$

Using Eq.(7), the values of R_s were calculated as a function of bias and are given in Fig. 4. As can be seen in Fig. 4, the value of R_s give a peak in the certain voltage ranges and began disappear at low illumination levels and these peaks are attributed to the particular distribution of localized density of the interface states. Also, the peak position shifts towards forward bias region with increasing illumination level due to the restructure and reordering interface states between Au and n-CdTe and in the CdTe band gap.In order to obtain the N_{ss}, we used Hill-Coleman method [37]. According to this method, the N_{ss} can be determined by using the following equation;

$$N_{ss} = \frac{2}{qA}\frac{(G_m/w)_{\max}}{(((G_m/w)C_{ox})^2 + (1-C_m/C_{ox})^2))} \tag{8}$$

where A is the area of rectifier contact, w (=2πf) is the angular frequency and C_{ox} is the capacitance of native insulator layer in strong accumulation region. The value of C_m, R_s and N_{ss} which is corresponding to the conductance peak value for Au/n-CdTe SBD determined from C-V and G/w-V data in the illumination level range of 0-200 W and are given Table 2. As shown in Table 2, while the value of N_{ss} increases, the R_s decreases with the increasing illumination levels. In addition, the distribution of interface states profile dependent on the illumination level was obtained from dark-illumination capacitance data as following Eq. (9).

$$N_{ss} = \frac{q}{A}\left[\left(\frac{1}{C_{dark}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{Cill.} - \frac{1}{C_{ox}}\right)^{-1}\right] \tag{9}$$

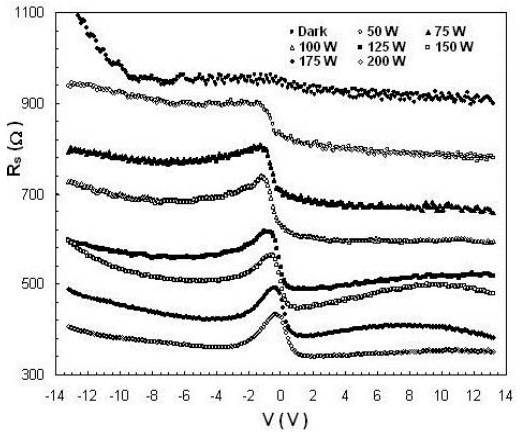

Fig. 4. The series resistance profile of Au/n-CdTe SBD calculated from measured capacitance C and conductance G/w data in dark and under six illumination levels.

where C_{dark} and $C_{ill.}$ are the measurement capacitance in dark and under illumination, respectively. The advantage of this method comes from the fact that it permits determination of many properties of the insulating interface layer, the semiconductor substrate, and interface easily. In this method [38], the N_{ss} is extracted from its capacitance contribution to the measured experimental C-V curve. In the equivalent circuit of MS or MIS type diodes, the oxide capacitance C_{ox} is in series with the parallel combination of the interface state capacitance (C_{it}) and the space charge capacitance (C_{sc}). In dark and at high frequencies, interface states cannot respond to the ac excitation, so they do not contribute to the total capacitance directly.

Table 2. The values of various parameters for Au/n-CdTe SBD obtained from C-V and G/w data in dark and under six illumination levels.

Illumination Levels	V_m (V)	C_m (F)	G_m/w (F)	N_{ss} ($eV^{-1}cm^{-2}$)	R_s (Ω)
Dark	-0.5	$4.17x10^{-11}$	$3.79x10^{-11}$	$3.02x10^{10}$	899
50 W	-0.1	$4.76x10^{-11}$	$4.98x10^{-11}$	$3.96x10^{10}$	779
75 W	0.2	$5.66x10^{-11}$	$5.99x10^{-11}$	$4.77x10^{10}$	658
100 W	0.8	$6.25x10^{-11}$	$6.71x10^{-11}$	$5.34x10^{10}$	594
125 W	0.9	$8.13x10^{-11}$	$7.70x10^{-11}$	$6.13x10^{10}$	517
150 W	1.2	$8.88x10^{-11}$	$8.19x10^{-11}$	$6.52x10^{10}$	480
175 W	1.4	$1.03x10^{-10}$	$9.57x10^{-11}$	$7.62x10^{10}$	383
200 W	1.8	$1.17x10^{-10}$	$1.08x10^{-10}$	$8.60x10^{10}$	351

The values of C as a function of bias voltage and the values of N_{ss} measured in dark and under illumination are given in Fig. 5(a) and (b), respectively. For the case of an Au/CdTe SBD with a native insulator layer, insulator/oxide layer capacitance was obtained as 4 nF in the strong accumulation region C-V plot. As shown in Fig. 5(b), the values of N_{ss} increase from inversion region towards the accumulation region with the increasing bias voltage.

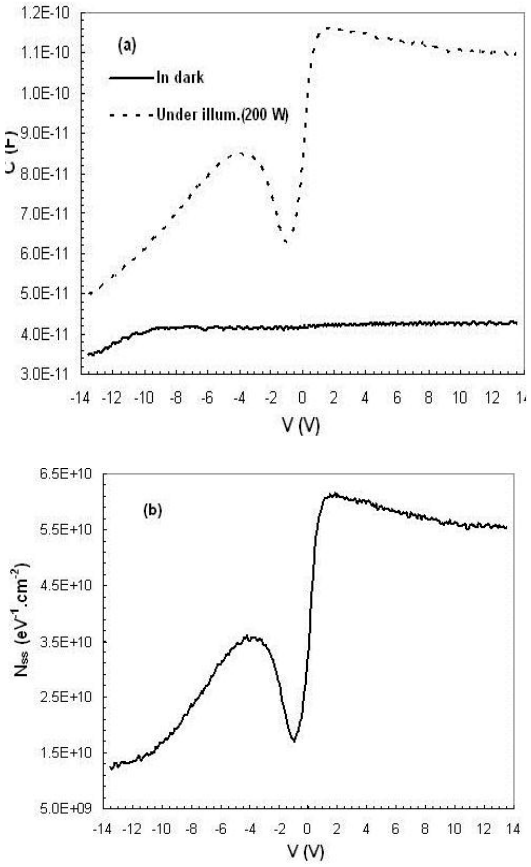

Fig. 5. (a) Measured capacitance in dark and under illumination (b) and density distribution profile of illumination induced interface states.

4. Conclusions

Under both in dark and different illumination levels I-V, C-V and G/w-V measurements of Au/n-CdTe Schottky SBD are performed at room temperature. It is clear that the main electrical parameters such as I_o, n, Φ_{Bo}, R_s and R_{sh} obtained from I-V data were found strongly dependent on the illumination levels and while the values of I_o and n increase, Φ_{Bo}, R_s and R_{sh} decrease with the increasing density of illumination level. Such behaviors of these main electrical parameters can be attributed that electron-hole pairs generate in the junction as a result of the light absorption. The C-V and G/w-V characteristics show that both of the values of capacitance and conductance increase with the increasing illumination levels and give the peaks especially at high illumination levels. Experimental results show that the values of R_s decreases and N_{ss} increases with the increasing illumination levels. Also, the changes in R_s with illumination exhibit a linear behavior. In conclusion, when ignoring the effect of illumination and bias voltage on I-V, C-V and G/w-V characteristics, it can lead to many significant errors in the main electrical parameters.

References

[1] K. M. Al-Shibani, Physica B, **322**, 390 (2002).
[2] I. M. Dharmadasa, G.G. Roberts, M.C. Petty, J. Phys. D. Appl. Phys., **15,** 901 (1982).
[3] M. Pattabi, S. Krishnan, Ganesh, X. Mathew, Solar Energy, **81**, 111 (2007).
[4] S. Gurumurthy, H. L. Bhat, V. Kumar, Semicond. Sci. Technol., **14,** 909 (1999).
[5] L. A. Kosyachenko, X. Mathew, V. V. Motushchuk, V. M. Sklyarchuk, Solar Energy, **80,** 148 (2006).
[6] X. Mathew, Semicond. Sci. Technol., **18**, 1 (2003).
[7] E. H. Rhoderick, R. H. Williams, Metal-Semiconductor Contacts; Clarendon Press, Oxford, (1988).
[8] S. M. Sze, Physics of Semiconductor Devices; Willey, New York, (1981).
[9] F. Yakuphanoglu, Physica B, **388**, 226 (2007).
[10] Ş. Karataş, Ş. Altındal, A. Türüt, A. Özmen, Appl. Surf. Sci., **217**, 250 (2003).
[11] F. A. Padovani, R. Stratton, Solid. State Electron. **9**, 695 (1966).
[12] S. Varma, K.V. Rao, S. Kar, J Appl Phys. **56,** 2812 (1984).
[13] A. Kassis, M. Saad, Renewable Energy **34,** 965 (2009).
[14] M. O. Aboelfotoh, Physical Rev. B., **39**, 5070 (1989).
[15] A. S. Bhuiyan, A. Martinez, D. Esteve, Thin Solid Films, **161,** 93 (1988).
[16] D. Donoval, M. Barus, M. Zdimal, Solid State Electron., **34**, 1365 (1991).
[17] J. Shewchun, R. Singh, D. Burk and F. Scholz, Appl. Phys. Lett., **35,** 416 (1979).
[18] W. M. R Divigalpitiya, Solar Energy Materials **18**, 253 (1989).
[19] R. N. Hall, Solid-State Electronics, **24**, 595 (1981).
[20] S. Özdemir, Ş. Altındal, Sol. Energy Mater. and Sol. Cells, **32**, 115 (1994).
[21] M. Wolf, G.T. Noel and R.J. Stirn, IEEE Trans. Elect. Devices, **4,** 419 (1977).
[22] Ş. Altındal, A. Tataroğlu, İ. Dökme, Solar Energy Mater. and Solar Cells, **85,** 345 (2005).
[23] P. Vitanov, M. Kamenova, N. Tyutyundzhiev, M. Delibasheva, E. Goranova, M. Peneva, Thin Solid Films, **297**, 299 (1997).
[24] H. Kanbur, Ş. Altındal, A. Tataroğlu, Appl. Surf. Sci., **252,** 1732 (2005).
[25] E.H. Nicollian, J.R. Brews, MOS (Metal-Oxide-Semiconductor) Physics and Technology; John Wiley&Sons, New York, (1982).
[26] G. A. Kaljuzhanya, T. S. Mamedov, K. H. Herrman, M. Wendt, Kristall und Technik, **14,** 849 (1979).
[27] G.M. Guro, G.A. Kaljuzhanya, T.S. Mamedov, Shelepin Sov. Phys. JETP, **50,** 1141 (1979).
[28] S. Chand, J. Kumar, Semicond. Sci. Technol. **10,** 1680 (1995).
[29] S. Ashok, K. P. Pande, Sol. Cells, **14**, 61 (1985).
[30] M. Saad, A. Kasiss Sol. Energy Mater. and Sol. Cells, **77,** 415 (2003).
[31] M.Y. Feteha, M. Soliman, N. G. Gomaa, M. Ashry, Renewable Energy, **26**, 113 (2002).
[32] H. Norde, J. Appl. Phys., **50,** 5052 (1979).
[33] S. K. Cheung, N.W. Cheung, Apply. Phys. Lett., **49**, 85 (1986).
[34] İ. Dökme, P. Durmuş, Ş. Altındal, Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms **266**, 791 (2008).
[35] E. H. Nicollian, A. Goetzberger, Bell Syst. Tech., **7,** 1055 (1967).
[36] A. Tataroğlu, Ş. Altındal, Microelectron. Eng., **83**, 582 (2006).
[37] W. A. Hill, C. C. Coleman, Solid State Electron., **23,** 987 (1980).
[38] D. E. Yıldız, Ş. Altındal, Microelectronic Engineering, **85**, 289 (2008).

*Corresponding author: hatice.kanbur@bozok.edu.tr