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Electrical and photoelectrical characterization of n-ZnSe/p-GaAs devices prepared by Metal Organic Chemical Vapor Deposition(MOCVD)

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In this work, the electrical characteristics of the n-ZnSe/p-GaAs structure, epitaxially grown by metal organic chemical vapor deposition (MOCVD), were investigated. The dark current–voltage (I–V) and capacitance–voltage (C–V) characteristics of the structure were determined at various temperatures in the range of 298–398 K. The charge transport conduction mechanism in forward biased condition is described by the modified Schockley effect. Some important junction parameters such as series resistance, R_s, shunt resistance , R_{sh}, ideality factor,*n*, and barrier height Φ_{BO} , were determined from the analysis of these curves. The ideality factor of the device is higher than unity, suggesting that the device shows a non-ideal behavior due to series resistance and barrier height inhomogeneities. The barrier height values obtained from the I–V and C–V characteristics were compared. It has been observed that the barrier height value obtained from the C–V measurements are higher than that obtained from the I–V measurements at various temperatures. The effect of illumination on the I-V characteristics was studied and the important solar cell parameters were obtained .

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Keywords: ZnSe/GaAs, MOCVD, Heterojunction, Photoelectric, Electrical characterization

1. Introduction

Zinc selenide (ZnSe), a well known II–VI semiconductor with cubic zinc blende structure and with a wide direct band-gap , i.e. 2.7 eV , is found to be a very promising material for optoelectronic and heterojunction solar cells [1] . It has been used in many applications such as a protective and antireflection coating for infrared-operating electrochromic thermal-control surfaces [2], light-emitting diodes [3–4], dielectric mirrors [5] and photodiodes [6,7]. Since most electronic devices are produced in the form of thin film, for any such applications, the material preparation and characterization plays a vital role and also the crystallographic quality of thin films largely depends on the ambient pressure and lattice match [8]. The growth and study of the prepared film on lattice-matching substrates also plays a crucial role for such applications.

The epitaxial growth of ZnSe was usually performed on Si [9], Ge [9] , GaAs [10] and many other material substrates. Various effects such as the enhancement of growth rate and the improvements of crystalline qualities were observed .

ZnSe-GaAs is one of the most promising heterovalent material combinations in view of good lattice matching (0.27% at room temperature (RT))[11]. A broad variety of techniques has been used for the deposition of ZnSe films, such as metal organic chemical vapour deposition (MOCVD) [12], RF magnetron sputtering [13], molecular beam epitaxy (MBE) [14], metal organic vapour phase epitaxy (MOVPE) [15] and vacuum evaporation [16].

We report here the results of the temperature dependence of the dark current –voltage and capacitance voltage characteristics of n-ZnSe/p-GaAs devices prepared by metal-organic chemical vapor depositions (MOCVD) method at different temperatures. The values of the essential parameters for the interpretation of these measurements, as well as for an evaluation the effective parameters of the device under illumination were derived.

2. Experimental details

ZnSe epitaxial layer of thickness 2-3 μm were grown on p-type GaAs (100) substrates using a Metal Organic Chemical Vapor Deposition, MOCVD, system with a horizontal reactor founded in University of Manchester Institute of Science and Technology UMIST, UK.

Diethylzinc (DEZn) was used as the source for Zn, selenium hydride (H_2Se) was used as the source Se. Both these source gases were diluted in H_2. Just prior to growth , the GaAs substrate was steamed in 1-1-1 trichloroethane vapor for 30 min, then etched in a (5 : 1 : 1) H_2SO_4:H_2O_2:H_2O mixture for 5 min at room temperature to remove its surface residue oxide[17]. After the chemical cleaning, substrate was mounted in the reactor and cleaned by the H-radicals at 650°C. Usually this step was carried out in the H_2Se environment, because removal of the surface oxide layer and improvement of surface polarization of non-polar substrates was expected there[18] . After this treatment, the substrate temperature was lowered to the deposition temperature and the growth

of ZnSe film was started by introducing diethylzinc. Finally the growth was resumed for the desired ZnSe epilayer. Typical growth conditions are listed in Table 1.

For the I–V measurements, stabilized power supply and high-impedance Keithley 617 electrometer were used. The dark C–V measurements were performed at different temperatures using a computerized capacitance–voltage system consisting of C–V meter (model 4108, Solid State Measurement, Inc., Pittsburg). The temperature of the samples was measured during electrical measurements by NiCr–NiAl thermocouple with accuracy ±1 K. The I-V characteristics were also investigated under different illumination using a 500 W tungsten halogen lamp measurements . The intensity of light was measured by a digital lux-meter .

3. Results and discussion

3.1 Dark I-V characteristics

n-ZnSe/p-GaAs heterojunction devices were forward biased when applying a positive bias voltage to the ZnSe. The dark current versus bias voltage plots (I-V) of the diode structure at different temperatures in the range 298-398 K is shown in Fig. 1. As observed from Fig. 1, a non-linear behavior was obtained between the dark electrical current and the bias voltage as well as asymmetrical behavior exhibiting rectification effect. Since ZnSe and GaAs make ohmic contacts with their electrodes of high work function and low work function, respectively, so we infer that a junction is formed between ZnSe and GaAs which is responsible for rectification effect in the device due to the energy barrier which is formed at the interface between the ZnSe and GaAs, i.e. at ZnSe/GaAs interface.

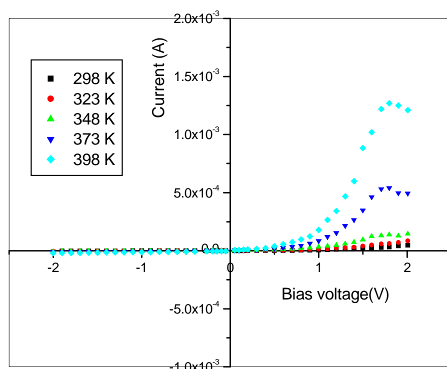

Fig. 1 Current–voltage characteristics of the n-ZnSe/p-GaAs heterojunction at different temperature.

The rectification ratio (RR) is calculated as the ratio of the forward current to the reverse current at a certain applied voltage [19]. The obtained values of the RR at different temperatures are listed in Table 2. As typically shown in Table 2, insufficient but apparent rectification characteristics were demonstrated at different temperatures.

To analyze the I–V characteristic curves with respect to conduction mechanisms through p-ZnSe/n-GaAs heterojunctions and device parameters, It found out the implication of Schockley mechanism by seeking out the linear region in the ln (I)–V plot of the forward current–voltage characteristics of the device. The semilogarithmic plot for the device is shown in Fig. 2. As observed , the plot consists of a linear region between 0.4–1.5 V and two curved regions at biases higher than 1.5 V and lower than 0.4 V. It is known that for a Schockley diode having high series resistance and small shunt resistance, the ln (I)–V plot contains a linear region only in a small range of moderate voltage, while at higher voltages, a downward curved region exist. That is why, we consider that the forward characteristics of the device up to 1.5V can be fitted well by the modified Schockley equation [20]

$$I = I_0\left\{\exp\frac{q(V-IR_s)}{nkT}-1\right\}+\frac{V-IR_s}{R_{Sh}} \quad (1)$$

where I_0 is the reverse saturation current which gives the numbers of charges able to overcome the energetic barrier in reverse bias., n is the diode quality factor which gives information about the recombination process takes place in the device and shape of the interfaces[21] , R_s and R_{sh} are series and shunt resistance of the device , respectively, and q is the electronic charge. The source of the series resistance R_s is mostly the combined effect of bulk of ZnSe layers of the device and the barrier. For an ideal diode, $R_{s\to 0}$ [22]. The source of shunt resistance R_{sh} is attributed to the leaky nature of the barrier. For an ideal barrier, $R_{sh\to\infty}$ [22] .

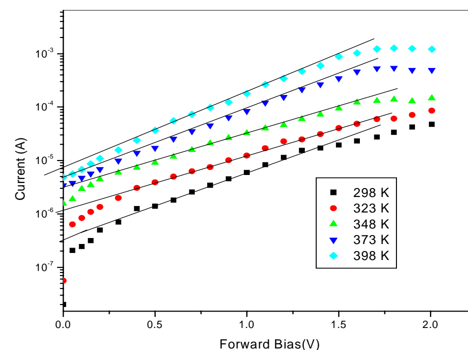

Fig. 2. Plots of the forward I–V of the n-ZnSe/p-GaAs heterojunction at different temperatures.

Now, to find out the exact voltage region wherein the Shockley mechanism predominates, it is required to improve the linearity of the ln (I)–V plot and therefore it is essential that the effect of the R_s and R_{sh} should be

removed. For this, we need to determine the values of R_s and R_{sh} by using Eq.(1) as follows:

The junction resistance R_J, can be given as

$$R_J = \frac{dV}{dI} = R_s + \frac{1}{[\beta I_0 \exp\{\ \beta(V - IR_s) + 1/R_{Sh}\ \}} \quad (2)$$

where β=q/nkT.

For higher forward bias(V> 1.5 V) , the curved region in ln (I)–V plot is attributed to series resistance R_s and therefore Eq. (1) can be approximated as

$$I = I_0 \exp[\beta(V - IR_s)] \quad (3)$$

For low voltages(V< 0.4 V) , where R_{sh} is predominating, the approximation $\beta I_0\exp[\beta(V-IR_s)] << 1/R_{sh}$ is valid, and Eq. (2) becomes

$$R = R_s + R_{Sh} \quad (4)$$

Usually $R_s << R_{sh}$, so the value of R_J approaches to R_{sh} at low biases.

The values of R_s and R_{sh} are determined from the plot of R_J against V , where $R_J = \partial V/\partial I$, which can be obtained from the I–V characteristics. It is observed from Fig. 3 that at sufficient high forward voltage, the junction resistance approaches to a constant value, which is the series resistance (R_s). On the other hand, the junction resistance is also constant at high reverse bias, which is equal to the diode shunt resistance (R_{sh}).

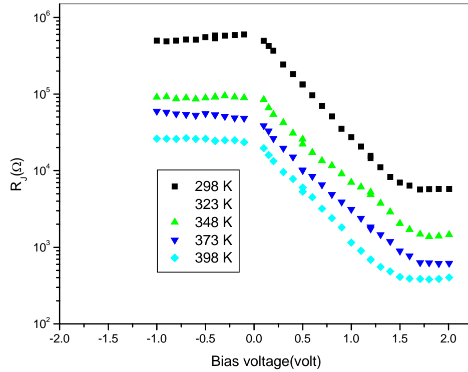

Fig. 3. Plots of junction resistance versus applied voltage of the n-ZnSe/p-GaAs heterojunction at different temperatures.

For determination of the values of diode quality factor n and the reverse saturation current I_0, we required to improve the linearity of the ln (I)–V plot and hence remove the effect of R_s. This can be achieved by making the following change in the variable junction voltage (V_J):

$$V_J = V - IR_S \quad (5)$$

Substituting from Eq.(5) in Eq(1) , the modifdied Schockly Eq. becomes

$$I = I_0[\exp(\beta V_J) - 1] + \frac{V_J}{R_{Sh}} \quad (6)$$

At higher forward biases, Eq. (6) becomes

$$I = I_0 \exp(\beta V_J) \quad (7)$$

Therefore, from the plot of ln (I) vs. V_J , n and I_0 can be deduced . Further, to increase the accuracy, we should remove the effect of the R_{sh} from the ln (I)–V plot, as well. This is achieved by plotting ln ($I-V_J/R_{sh}$) vs. V_J because ($I-V_J/R_{sh}$) can be considered to describe the current flowing in the junction only. Such a plot for our device is shown in Fig. 4 . The removal of the effect of R_s and R_{sh} has lead to the increase in linearity of the ln (I)–V plot. The values of n and I_0 are respectively obtained from the slope and the extrapolating the linear region of the curve to zero applied voltage at different temperatures and listed in Table (2)

The reverse saturation current, I_0 is defined by [23]

$$I_0 = AA^* \exp\left(\frac{-q\Phi_{BO}}{kT}\right) \quad (8)$$

where the quantities A, A*, T , q, k and Φ_{B0} are the diode area, the effective Richardson constant, temperature in Kelvin, the electronic charge, Boltzmann,s constant and the zero- bias barrier height respectively. The experimental values of the zero-bias barrier height was determined from the obtained values of saturation current ,using the above equation , and listed in Table 2.

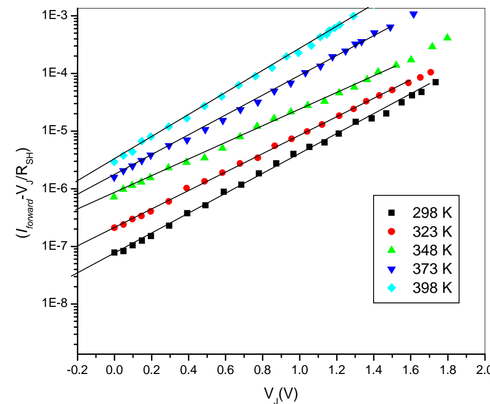

Fig.4 Plots of the forward current ($I_{forward} - V_j/R_{sh}$) versus junction votage of the n-ZnSe/p-GaAs heterojunction at different temperatures .

Fig. 5 shows the temperature dependence of the ideality factor ,n , and zero -bias barrier height Φ_{BO} . As observed ,the experimental values of n increase with a decrease in temperature while the values of the experimental barrier height decrease with a decrease in temperature . Furthermore, a value of 0.95 eV for the n-ZnSe/p-GaAs heterojunction structure was obtained at room temperature that is significantly larger than the value of 0.6 eV of the conventional Au/GaAs Schottky diode. As can be seen from the results above the high values of n, depending on the sample temperature , which are much larger than unity may occur in asymmetrical junctions which could be attributed to the increase in junction current with temperature [24].

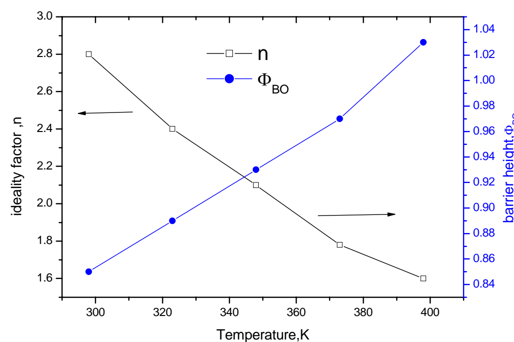

Fig.5 Plot of ideality factor and barrier height against temperature .

3.2 Capacitance – voltage characteristics

The capacitance–voltage (C–V) measurements of the n-ZnSe/p-GaAs devices were performed at the frequency of 1 MHz and over the temperature range 298-398 K. This frequency suggests that the redistribution of free carrier inside the n-GaAs side can respond to this value (1 MHz) while that of n-ZnSe cannot. This may be attributed to the different in the relaxation time for both of n-ZnSe and p-GaAs used in this study [25]. From this point of view, information about the depletion region extending in the n-GaAs side can be obtained regardless that of n-ZnSe side.

The junction capacitance,C_J of n-ZnSe/p-GaAs junctions with depletion layer width *W* is given by [25]

$$C_J = \frac{\varepsilon A}{W} \quad (9)$$

where ε is the dielectric constant of the semiconductor material and A is the cross-sectional area of the diode. Within the abrupt junction approximation, and for a p-n junction, the dependence of the depletion width on doping density, N_a, in the p-type region is given by [20]

$$(10)\, W = \sqrt{\frac{2\varepsilon}{qN_a}\left(V_o - V_a\right)}$$

Here, V_o is the built-in potential and V_a is the applied bias.

Thus, applying a reverse bias to the diode causes an increase of *W*, which decreases the capacitance. The capacitance is then

$$(11)\, C_J = \frac{A}{2}\sqrt{\frac{2q\varepsilon}{\left(V_o - V_a\right)}N_a}$$

In the p-ZnSe/n-GaAs junction , a measurement of the capacitance-voltage curve gives information about the doping density in the n-type region. Since increasing reverse bias increases the depth of the depletion region, information on the doping density and the built-in voltage by measuring the capacitance as a function of reverse bias can be obtained .

In general case, the dopant on one side of the junction has been diffused or implanted into a semiconductor of the opposite type; thus the diffused dopant has a concentration that decreases rapidly with depth from the surface of the semiconductor. If the drop in concentration is very rapid, the abrupt junction approximation is a good one. If the drop is less rapid, a linearly graded junction is a better approximation to the dopant profile.

According to above discussion , the doping density on the lightly doped side of a n-ZnSe/ p-GaAs junction can be found by constructing a plot of $1/C_j^2$ vs. V_a as shown in Fig.6. From the expression for C_J above we find

$$\frac{1}{C_j^2} = \frac{2}{A^2}\frac{V_0 - V_a}{q\varepsilon N_a} \quad (12)$$

Thus, the slope of the straight line of the graphical representation of Fig. 6 inversely proportional to the doping density and an intercept equal to the built in potential Vo. The change in N_a and V_o with temperature are given in Table 3 . As shown in Table 3 , the N_a and V_o were found to be a strong function of temperature. The values of N and V_o for the device versus temperature are shown in Fig. 7 while the carrier concentration increases with increasing temperature, V_o decreases in the temperature range 298 - 398 K .

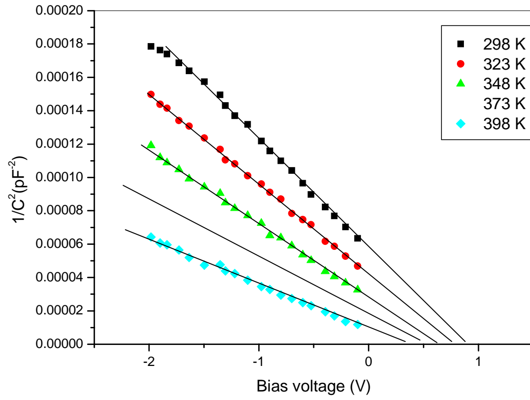

Fig. 6 Plots of $1/C^2$ against bias voltage .

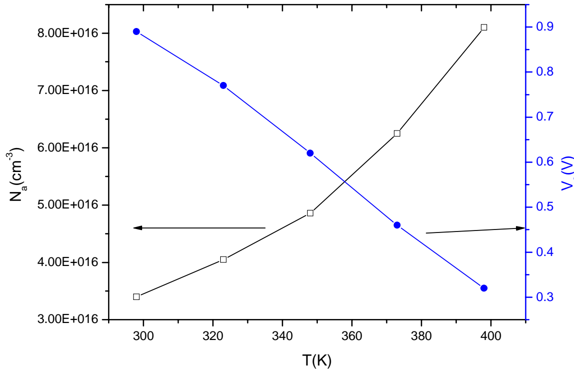

Fig. 7. Carrier concentration and built-in poltential against temperature

The barrier height for n-ZnSe/p-GaAs diode can be determined using the following well-known equation, using C–V measurements[26]

$$\Phi_b=V_o+V_p \quad (13)$$

where V_p is the potential difference between the Fermi energy level (E_f) and the top of the valence band in the neutral region of p-GaAs, which is directly equal to E_f, and can be calculated by knowing N_a and N_c, density of states in the conduction band, which is N_v=2.8x10^{19} cm^{-3} for p-GaAs at room temperature[27]

$$N_a = N_v \exp(\frac{V_p}{kT}) \quad (14)$$

The above Eq. is valid for only the diodes which show ideal behavior, the ideality factor (n) is equal to unit, otherwise it is higher than unit. In an ideal Schottky barrier, the barrier height is independent of the bias and current flows only due to thermionic emission, n =1. Factors which make n larger than unity are the bias dependence of barrier height, electron tunneling through the barrier, and the carrier recombination within the depletion region. Since these devices operate under high-level injection, deviations from the ideal behavior are also observed because of enhanced minority carrier transport by the drift field in the quasi-neutral region. For non-ideal structures, this equation should be corrected by taking into account of ideality factor [28]:

$$\Phi_b=C_2V_o+V_p \quad (15)$$

where C_2 corresponds to $1/n$. Where, the values of the ideality factor (n) have been obtained from the forward bias I–V characteristics. Measurement of the depletion region capacitance under forward bias is difficult because the diode is conducting and the capacitance is shunted by a large conductance. However, the capacitance can be easily measured as a function of the reverse bias [29].

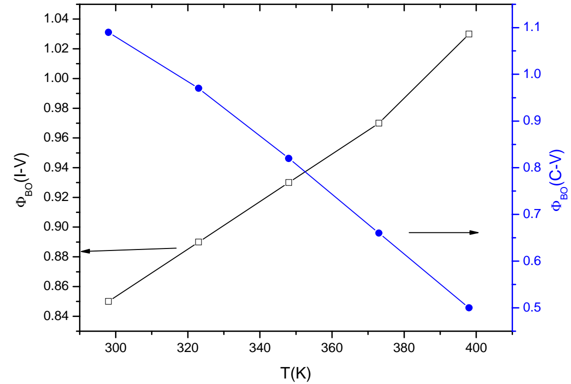

Fig. 8 Plots of Φ_{BO}(I-V) and Φ_{BO}(C-V) against temperature.

Fig. 8 shows the barrier height against temperature, Φ_{BO} obtained from the I–V characteristics (using Eq. (8)) and from the C–V measurements. The barrier height extracted from the C–V measurements increase slowly with decreasing temperature, in contrast to the I–V measurements. Therefore, there is more current at low temperature than predicted by thermionic emission theory and the results of the C–V measurements. Also, the values of the barrier height extracted from the C–V curves are higher than derived from the I–V measurements as expected. Although, this discrepancy could be explained by the existence of excess capacitance at the structure due to the an interfacial layer or trap states in the semiconductor, the existence of the barrier inhomogeneity offers another explanation. If the barriers are uniform and ideal, the two measurements yield the same value; otherwise, they will yield different values.

3.3 I-V characteristics under illumination

Fig. 9 shows the current-voltage characteristics of the fabricated n-ZnSe/p-GaAs heterojunction recorded at different illumination intensities (as mentioned in the figures) at 298 K to study the junction behavior under illumination. The diode equation of the thin film solar cell under illumination condition corrected for series resistance R_s and shunt resistance R_{sh} can be represented as[30]

$$I = I_o\left[\exp\frac{q(V-IR_s)}{nkT}-1\right]+\frac{V-IR_s}{R_{sh}}-I_L \quad (16)$$

where I_L is the light current, I_0 is the reverse saturation current and n is the diode ideality factor, which can all be dependent on bias voltage and temperature. However, for an ideal diode n being constant and I_0 is only dependent on temperature. Usually, n has a value between 1 and 2. The short - circuit current $I_{SC} = I|_{V=0}$ and the open-circuit voltage $V_{OC} = V|_{I=0}$ under different illumination intensities were measured from the I–V characteristics.

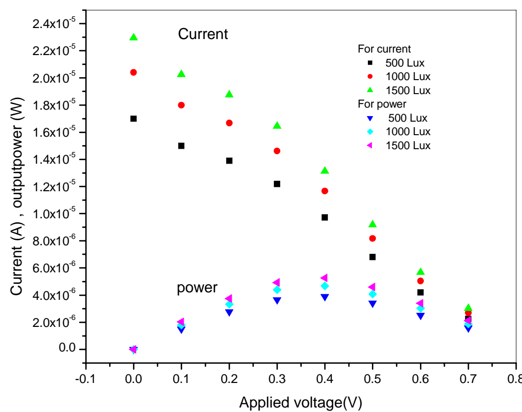

Fig.9. Plots of photocurrent and output power against applied voltage at different intensitie.

The series and shunt resistance were calculated using following equations:

$$R_s = \left.\frac{dV}{dI}\right|_{V=V_{oc}} \quad (17)$$

$$R_{sh} = \left.\frac{dV}{dI}\right|_{I=I_{sc}} \quad (18)$$

The values of R_s and R_{sh} are tabulated in Table 4 . As observed , the obtained values are in good agreement with that of under dark condition .

The open circuit voltage, V_{OC} can be expressed in the following way:

$$V_{oc} = \frac{nkT}{q}\ln\left(\frac{I_{sc}}{I_0}+1\right) \quad (19)$$

The parameters of the heterojunction obtained after the effect of different light illumination have been tabulated in Table 1. The fill factor obtained of the n-ZnSe/p-GaAs heterojunction is very low compared to the other thin film solar cells[1] . The major contributor to the relatively low efficiency of the n-ZnSe/p-GaAs heterojunction was the large value of series resistance R_S.

It has been observed that on illumination there was a small increment in both I_{SC} and V_{OC} of n-ZnSe/p-GaAs heterojunction which in turn enhanced the fill factor.

4. Conclusion

The fabricated Au/p-ZnPc/p-Si devices by MOCVD method showed a rectification behavior and photovoltaic characteristics due to the formation of a barrier at ZnSe - GaAs interface . The downward concave curvature of the forward bias current-voltage at low and high voltages are caused by the presence of the effect of shunt and series resistances respectively . The correction of the I-V curves at different temperatures from the effect of series and shunt resistances were made . Then the accurate values of the reverse saturation current and diode ideality factor were calculated.

The value of the barrier height obtained from the I-V and C–V characteristics at a frequency of 1MHz were compared . The discrepancy between the obtained values may be due to the presence of an interface layer and barrier height inhomogeneities that prevail at the ZnSe - GaAs interface. Also, it can be said that the excess capacitance resulting from the interface states in equilibrium with the GaAs substrate that can follow the AC signal of the C-V measurements at 1 MHz is not constant. The photovoltaic parameters of the device under different illuminations were found to be restricted by the effect of series and shunt resistances,

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