Electrical characteristics of a Schottky device based on maleic anhydride deposited on *p*-type silicon by spin coating technique

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Al/Maleic Anhydride (MA)/p-Si metal-polymer-semiconductor (MPS) structures were prepared on *p*-Si substrate by spin coating and these MPS structures had a good rectifying behavior. The capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) characteristics of Al/MA/p-Si structures were investigated in the frequency (*f*) range of 1kHz-10MHz at room temperature. The parameters of diodes such as ideality factor, series resistance, barrier height and flat band barrier height were calculated from the forward bias *I-V* characteristics. The investigation of interface states density and series resistance from capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) characteristics in the MPS structures with thin interfacial insulator layer have been reported in order to explain the electrical characteristics of metal/polymer/semiconductor (MPS) with Maleic anhydride (MA) interface. The values of interface states density D_{it} and series resistance R_s were calculated from measurements of *C* and *G*. The values of interface states density D_{it} and series resistance R_s were calculated from measurements of *C* and *G*. These values of D_{it} and R_s were responsible for the non-ideal behavior of *I-V* and *C-V* characteristics. The *I-V*, *C-V-f* and *G-V-f* characteristics confirm that the barrier height, D_{it} and R_s of the diode are shown parameters that strongly dependent on the electrical parameters in the MPS structures.

1. Introduction

Organic semiconductors have increasingly attracted attention to wide applications in various electronic and optoelectronic devices in recent decades [1]. By using organic semiconductors, it is possible to prepare flexible, large-area devices which have very light weights and low manufacturing cost. The greatest feature of the organic materials is that they can be chemically adjusted separately the band gap, valence and conduction band energies, charge transport as well as the solubility or other structural properties [2]. In addition, organic materials have reached the early stages of commercialization with the technological success of thin film organic optoelectronic devices, particularly organic light-emitting devices and improvement of their efficiency. Manufacturing yield and long-term stability have been considerably achieved, too [1-3,4-5]. Owing to their stability and barrier height (BH) enhancement properties, organic materials have been employed particularly in electronic devices [1-3, 7–10]. It is believed that the organic/inorganic semiconductor Schottky barrier diodes are useful to increase the quality of devices fabricated using the semiconductor [11].

When organic films are inserted between metal and semiconductor, they modify both electrical and dielectric properties of Schottky barrier diodes (SBDs). When a bias voltage is applied across the diode, the combination of the interfacial insulator or polymer layer, depletion layer and series resistance of the diode share this applied bias voltage. Interface states at metal/semiconductor interface can be divided in two main groups depending on the thickness of the interfacial layer. These surface states act as recombination centers which provide a tunneling path for the carriers. One of the groups communicates with the metal rapidly if the value of interfacial layer is lower than about 30 Å, the other group communicates with the semiconductor if the value of interfacial layer is higher than about 30 Å[12,13].

The interface states and polymeric interfacial layer in metal/polymers/semiconductor (MPS) structures play an important role in determination of the main characteristics of electrical and dielectric parameters of organic optoelectronic devices. The remarkable interest in the electrical and optical properties of organic molecular semiconductors reflects their increasingly widespread use in organic and hybrid inorganic–organic devices [13-15].

The performance of a MPS structure depends on various factors such as presence of the localized interface states at the metal/organic polymer interfacial layer and organic polymer/semiconductor interfacial layer, metal to semiconductor barrier height, ideality factor and series resistance of MPS diodes. Interfacial polymer layer and series resistance are very important parameters of a MPS diode because the total voltage is shared by interfacial layer, depletion layer and series resistance of the diode when a voltage is applied to this diode. The magnitude of

this shared voltage depends on thickness of interfacial layer's structure and series resistance [16,17]. Thereby, the performance and reliability of these devices depend especially on both series resistance and interfacial layer quality. Series resistance should be taken into account for an accurate and reliable determination of the electrical characteristics. Kilicoglu et al. [3], and Gullu et al. [18] reported that the non-polymeric organic compounds known as Tetra amide-I, Congo Red, and Rhodamine B interfaced to the inorganic p-Si provides the rectifying *I–V* characteristics. They showed that the organic interfacial layer formed at the location of metal/semiconductor junction has a rectification behavior in which the values of Schottky barrier height and ideality factor are greater than those of the conventional Al/*p*-Si diode [19–26].

Metal semiconductor (MS) Schottky barrier diodes with an interfacial polymer such as polyaniline, poly (alkylthiophene), polypyrrole, polythiophene, poly (3-hexylthiophene), and polyvinyl alcohol (PVA) are taken into account research topics because of their potential applications and interesting properties by chemists, physicists, and electrical engineers as well[27,28].It is the first timemaleic anhydride (MA) was used amonginter facial polymers. It is an excellent monomer and has reactive anhydride or hydrolyzed anhydride functional groups (carboxylic groups) [29]. MA can be polymerized by various methods [30] such as radical solution [31-33], electrochemical [34], plasma[35], UV [36] and γ-irradiation [37], high pressure [38,39]and solid state [40] polymerizations. Low molecular weight poly(MA) is called as oligo(MA) and known as biopolymer. Poly(MA) and their derivatives widely used in industrial cooling water, boiler water, oil field injection, sugar mill evaporator, reverse osmosis, desalination and bioengineering applications [40,41]. But, oligo (MA) derivatives have not been studied enough. Synthetic route of oligo (MA) is shown in Fig. 1, the detailed information about the synthesis can be found in the article of Kahraman [30].
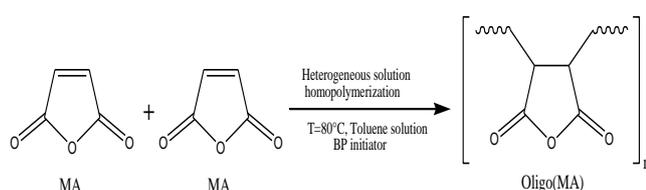
Fig. 1. Synthetic route of oligo (MA).

In this paper, MA used as thin interfacial polymer layer was deposited on *p*-Si using spin coating system to get high performance Al/MA/*p*-Si diodes. *C-V* and *G-V* measurements of the diodes were performed in the frequency range of 1kHz-10MHz at room temperature to explain the effects of series resistance and interface state density. The diode parameters such as ideality factor, series resistance, barrier height, flat-band barrier height were calculated from the forward bias *I-V* characteristics.

C-V-f, *G-V* and *I–V* characteristics of Al/MA/*p*-Si diode shave been studied and reported in this article.

2. Experimental

In this work, the samples were prepared on *p*-type Si (111) wafer which had 280 μm thickness and 10 ohm resistivity. Chemical cleaning procedures were applied before processing the wafer. Firstly, it was dipped into acetone for 10 minutes at 50°C then washed by deionized water and released into methanol for 2 minutes. After methanol bath the wafer was inserted in $NOH_4:H_2O:H_2O_2$ solution for 15 minutes at 70°C. It was dipped into deionized water to remove solution on the wafer surface. In order to take away free oxygen on the surface, the wafer was bathed in 2% HF solution for 2 minute. Finally, deionized water was used to complete cleaning procedure. Following surface cleaning, aluminum (Al) metal with purity of 99.999% was thermally evaporated on the whole back surface of the wafer with thickness of 640 Å. Then, the wafer was annealed at 500°C in vacuum for 10 minutes to dope aluminum into back surface of wafer. Again, the ohmic contact thickness of 800 Å was made by evaporating aluminum (Al) metal on the back of the *p*-Si substrate. Next, a Maleic anhydride organic film was formed by spin coating technique. Maleic anhydride and dimethylformamide (DMF) were mixed in 2:1 molar ratio, and stirred for an hour. The film was deposited by spin coating at 500 rpm for 1 minute and then at 1700 rpm for 45 seconds polished on surface of the wafer. Finally, rectifying contacts were deposited on organic film with a diameter of 1.3 mm using a metal shadow mask by evaporating 99.999% purity aluminum (Al) metal with thickness of 800 Å. All evaporation processes were carried out in a vacuum coating unit at about in 2×10^{-6} torr placed inside the vacuum chamber. *I-V* and *C-V* measurements were taken at room temperature to determine the electrical characteristics of the Schottky diodes. The schematic representation of the devices is shown in Fig. 2.The organic layer thickness was estimated to be about 10 nm from measurement of the interfacial layer capacitance in the accumulation region from *C–V* characteristic at 1MHz.
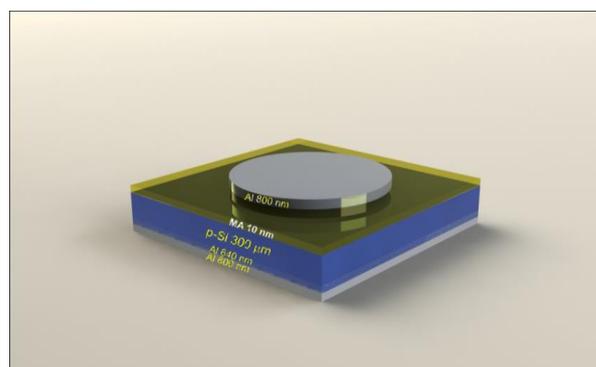
Fig. 2. Cross-sectional view of Al/MA/p-Si Schottky diode for electrical characterization.

3. Results and discussion

3.1. Current–voltage characteristics

The electrical characteristics of Al/MA/p-Si diodes have been analyzed by assuming the standard thermionic emission theory of the Schottky barrier model holds. According to this theory, it is usually assumed that the current is only controlled by the transport of carriers across the diode interface but both the drift and diffusion of carriers are unimportant within the depletion region. The weak voltage dependence of the reverse-bias current and the exponential increase of the forward-bias current are the characteristic properties of rectifying contacts [11,13].

The current through a Schottky barrier diode is due to thermionic emission current and is given by the relations [11,13]

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \quad (1)$$

and

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \quad (2)$$

where I_0 is the saturation current derived from the straight line intercept of the $\ln I - V$ plot at V=0. ϕ_b is the effective barrier height at zero bias, A^* is the Richardson constant and equals 32 A/cm^2 K^2 for p-type Si, where q is the electron charge, V is the applied voltage, A is the diode area, k is the Boltzmann constant, T is the temperature in Kelvin, n is the ideality factor. From Eq.(1), it is given

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \quad (3)$$

On the other hand, the effective barrier height ϕ_b can be defined from Eq. (2) as

$$\phi_b = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \quad (4)$$

The forward and reverse bias measurements of the Al/MA/p-Si SBDs were carried outat room temperature and are given in Fig. 3. As can be seen in Fig. 3, the semi-logarithmic I-V characteristics of the diodes show a good behavior, i.e. While the reverse current shows weak voltage dependence, the forward current increases exponentially with the voltage.The current curve in forward bias region becomes dominated by series resistance from contact wires or bulk resistance of the organic semiconductor and the inorganic semiconductor giving rise to the curvature at high current in the $\ln I - V$ plot. The forward bias semi-logarithmic $\ln I - V$ plots have a linear region in the voltage range of0.1-0.8 V and then deviate considerably from linearity especially due to the effect of R_s and interfacial polymer layer.
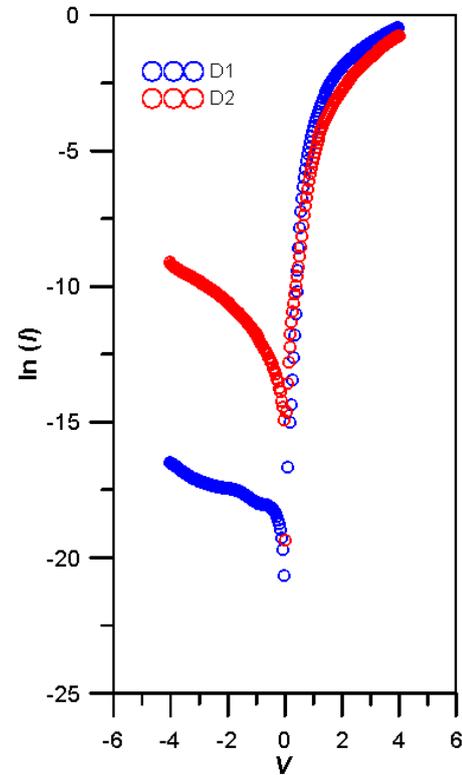
Fig. 3. Experimental forward and reverse bias semi-logarithmic $\ln I - V$ characteristics of the Al/MA/p-Si Schottky barrier diode at room temperature.

The values of the ideality factor and barrier height for Al/MA/p-Si organic Schottky devices were calculated from the forward I–V characteristics with MA layer presented in Fig. 3 using Eqs. (3) and (4), respectively. The Al/MA/p-Si (MPS) structures with a large value of n is far from ideal due to the presence of a thick interfacial oxide layer and the interface states. These values indicate that the current flow mechanism across the interface is also due to the generation-recombination and leakage currents. High values of n can be attributed to the presence of interfacial thin native oxide layer, to a wide distribution of low- SBH patches (or barrier in homogeneities) and to the bias voltage dependence of SBH [3]. The corresponding values of ideality factor and Schottky barrier height (SBH) are 1.89 and 0.75 eV for D1 diode, and are 1.38 and 0.78 eV for D2 diode, respectively.

Increasing of ϕ_b and n values have been attributed to particular distribution of interface states and polymeric composite layer between metal and semiconductor. The non-ideal value of n can be a consequence of several factors such as interface dipoles due to interface doping or specific interface structures, fabrication induced defects at the Al/MA/p-Si interface, recombination and generation, series resistance effect and image-force effect [42].

The series resistance (R_s) is an important parameter in the electrical characteristics of MPS diodes. This parameter is significant in the downward curvature of the forward bias *I-V* characteristics, but the other two parameters (n and ϕ_b) are significant in both the linear and non-linear regions of *I-V* characteristics. The values of R_s, n and ϕ_b were achieved using a method developed by Cheung and Cheung [16]. According to this method, this function can be written as

$$\frac{dV}{d(\ln I)} = n\frac{kT}{q} + IR_s \qquad (5)$$

$$H(I) = V - \frac{nkT}{q}\ln\left(\frac{I}{AA^*T^2}\right) \qquad (6)$$

and $H(I)$ is given

$$H(I) = n\phi_b + IR_s \qquad (7)$$

where ϕ_b is the barrier height obtained from data of the downward curvature region in the forward bias *I-V* characteristics.

In Fig. 4, experimental $\dfrac{dV}{d(\ln I)}$ vs. *I* and $H(I)$ vs. *I* plots are presented for the Al/MA/*p*-Si structures at room temperature, respectively. Eq. (4) should give a straight line for the data of the downward curvature region in the forward bias *I-V* characteristics. Where a plot of $\dfrac{dV}{d(\ln I)}$ vs *I* will be linear and give the R_s as the slope and $\dfrac{nkT}{q}$ as the *y*-axis intercept. Using the *n* value determined from Eq.(4) and the data of the downward curvature region in the forward bias *I-V* characteristics in Eq.(5), a plot of $H(I)$ vs *I* will also lead to be a straight line (as shown in Fig. 4) with the *y*-axis intercept equal to $n\phi_b$. The slope of this plot also determines R_s which can be used to check the consistency of this approach. The values of R_s and *n* were calculated from $dV/d\ln(I)$ versus *I* curve, yielding values of $R_s = 39\Omega$ and $n = 1.936$ for D1 diode and $R_s = 34$ $\Omega$and $n = 1.992$ for D2 diode at room temperature. Similarly, the plot of $H(I)$ versus *I* gives the series resistance $R_s$and the barrier height ϕ_b. The values of ϕ_b and R_s were calculated, yielding values of $\phi_b = 0.74 eV$ and $R_s = 26.25\Omega$ for D1 diode and $\phi_b = 0.73 eV$ and $R_s = 22.38$ $\Omega$for D2 diode at room temperature.
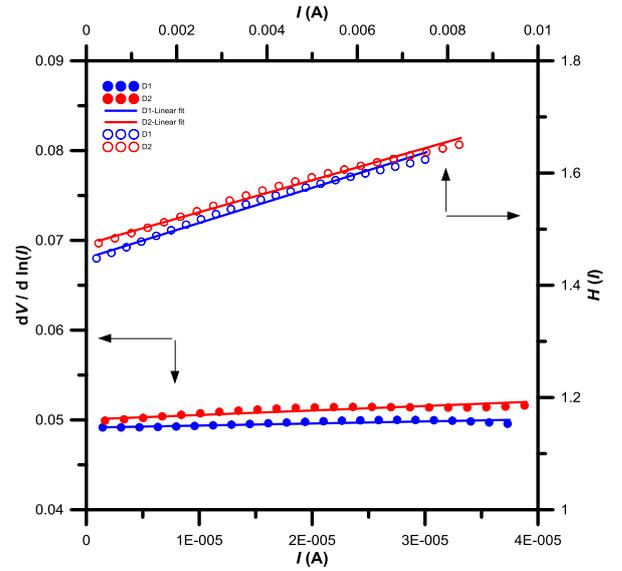
Fig. 4. The $dV/d(\ln I)$ vs. I and $H(I)$ vs I characteristics of Al/MA/p-Si structures at room temperature in dark.

Cheung functions are only applied to the nonlinear region in high voltage section of the forward-bias $\ln I - V$ characteristics [43]. The value of series resistances may also be large for the higher ideality factor values. Furthermore, the values of series resistance are very high for these devices. This situation indicates that the series resistance is a current-limiting factor for MPS structures. The effect of the series resistance is usually modeled with series combination of a diode and a resistance. The voltage drop across a diode is expressed in terms of the total voltage drop across the diode and the resistance. The very high series resistance behavior may be ascribed to decrease of the exponentially increasing rate in thecurrent due to space charge injection into the MA organic thin film at higher forward- bias voltages [43].

3.2. Analysis of capacitance–voltage characteristic of Al/MA/p-Si diodes

Fig. 5(a) and (b) show the voltage dependence of the measured *C–V* and *G–V* characteristics for D1 and D2, fabricated Al/MA/*p*-Siat 1MHz at room temperature. The bias voltage was varied between -4 and +4 VDC for all samples. As shown in Fig. 5(a) and (b), both *C–V* and *G–V* curves have three regimes as accumulation–depletion–inversion regions. The values of the capacitance and conductance depend on a number of parameters such as thickness and formation of the oxide layer, series resistance and energy distribution or density of interface states. The effect of the interface state density can be eliminated when the *C–V* and *G–V* curves are measured at sufficiently high frequencies ($f \geq 500$kHz) [44], since the charges at the interface states cannot follow an a.c. signal [44]. In this case, the interface states are in equilibrium with the semiconductor.
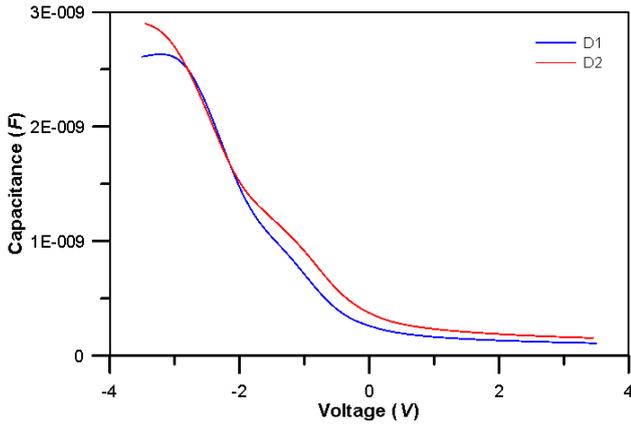
Fig. 5a. C–V characteristics of the Al/MA/p-Si MIS diode.

Fig. 5b. G–V characteristics of the Al/MA/p-Si MIS diode.
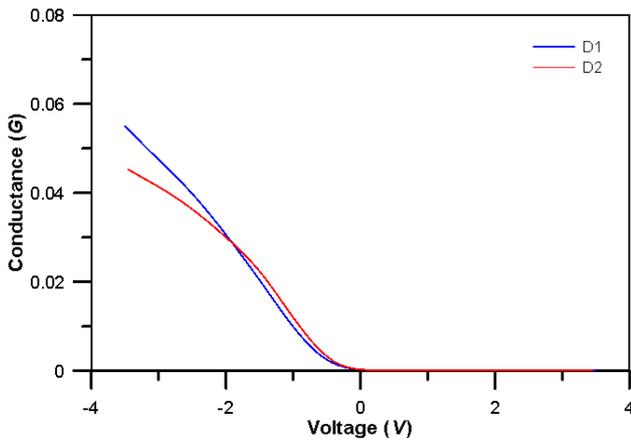
Fig. 5c. C⁻²-V plots of Al/MA/p-Si for 1 MHz at room temperature.

The C^2-V plot is presented at 1MHz in Fig. 5(c). As can be seen in the figure, C^2-V plots give a straight line in a wide range of applied bias voltages. The slope corresponds to the localized doping concentration [45]. This is derived from the standard Schottky–Mott analysis [45] where the doping concentration in a *p*-type semiconductor can be extracted in the depletion region via

$$\frac{\partial(1/C^2)}{\partial V} = \frac{2}{A^2 \varepsilon_s \varepsilon_0 q N_A} \qquad (8)$$

where *C* is the capacitance in the depletion region, *A* is the area of device, *V* is the gate voltage, N_A is the ionized traps like-acceptor which is determined from the slope of C^2-V plot, ε_s is the permittivity of the semiconductor ($\varepsilon_s = 11.8\varepsilon_0$ for Si) and ε_0 is the vacuum permittivity ($\varepsilon_0 = 8.85 \times 10^{-12}$ F/m) [13].

The barrier height can be obtained from the following relation [13]:

$$\phi_b(C-V) = V_{bi} + E_F - \Delta\phi_b \qquad (9)$$

where E_F is the energy difference between the bulk Fermi level and valance band edge and $\Delta\phi_b$ is the image force lowering and given by [13]:

$$\Delta\phi_b = \left(\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}\right)^{1/2} \qquad (10)$$

where E_m is the maximum electric field and given by [13]:

$$E_m = \frac{2qV_{bi}N_A}{\varepsilon_s\varepsilon_0} \qquad (11)$$

The frequency-dependent E_F values were obtained from

$$E_F = \frac{kT}{q}\ln\left(\frac{N_v}{N_A}\right) \qquad (12)$$

with

$$N_v = 4.82 \times 10^{15} T^{3/2}\left(\frac{m_h^*}{m_0}\right)^{3/2} \qquad (13)$$

where N_v is the effective density of states in valance band for *p*-Si, $m_h^* = 0.16m_0$ is the effective mass of holes [11, 13] and m_0 is the rest mass of the electron.

As well as barrier height, flat-band barrier height is calculated. It is considered to be a real fundamental quantity and given as [46]

$$\phi_{bf} = n\phi_b - (n-1)\frac{kT}{q}\ln\left(\frac{N_v}{N_A}\right) \qquad (14)$$

Initially, V_{bi} is found from the extrapolation of C^{-2}-*V* plot to the voltage axis, we calculated the value of V_{bi} as 0.96 and 0.95V for D1 and D2 diode at room temperature (300 K) and 1 MHz, respectively. The N_A value was found as 3.51×10^{15} and 7.09×10^{15}cm^{-3} for D1 and D2 diodes. Using Eqs. (9), (11) for diode D1, the values of $\Delta\phi_b$ and E_F have been calculated as 0.0198 and 0.199eV, respectively. The values of $\Delta\phi_b$ and E_F have been found as 0.023 and 0.182eV for diode D2, respectively. Using Eq. 8, the barrier height value $\phi_b(C-V)$ was calculated as 1.18 and 1.17eV for D1 and D2 Schottky diodes, respectively. Also using Eq.13 flat-band barrier height was found 1.37 and 1.007eV for D1 and D2 diodes.

As seen from the obtained values, the difference between $\phi_b(I-V)$ and $\phi_b(C-V)$ for the Al/MA/*p*-Sidiodes originates from the different nature of the *I–V* and *C–V* measurements. Due to different nature of the *C–V* and *I–V* measurement techniques, the barrier heights deduced from them are not always the same. The capacitance *C* is insensitive to potential fluctuation sonalength scale of less than the space charge region and *C–V* method averages over the whole area and measures to describe BH. Thed. c. current *I* across the interface depends exponentially on the barrier height and thus sensitively on the detailed distribution at the interface [13,47]. Additionally, the discrepancy between the barrier height alues of the device may also be explained by the existence of the interfacial layer and the trap state sin the semiconductor [46,55]. Consequently, the barrier heights obtained from C^{-2}-*V* characteristics at 1 MHz are remarkable higher than the values obtained from *I–V* characteristics at room temperature.

The discrepancy can be due to the organic layer plus interfacial native oxide layer between the metal and the *p*-Si. In addition, the existence of barrier height inhomogeneity could be another explanation for this discrepancy [24, 42]. Using Eq.8, the width of the depletion layer (W_d) have been determined as

$$W_d = \sqrt{\frac{2\varepsilon_s V_{bi}}{q N_A}} \qquad (15)$$

where the value of W_d was calculated 5.99 10^{-5}cm for diode D1 and 4.242 $\times10^{-5}$cm for diode D2.The maximum barrier field (E_{max}) which exists at the interface of the devices is defined as [45]

$$E_m = \frac{2V_{bi}}{W_d} \qquad (16)$$

We calculated values of E_m as 3.22×10^4 and 4.60×10^4V/cm for Schottky diodes D1 and D2, respectively.

In order to determine voltage dependent of the series resistance (R_s) values, using admittance method given by Nicollian and Brews [45]. This method provides the determination of R_s in the whole measured range diode. According to this method, the real value of R_s at sufficiently high frequencies ($f \geq 500$ kHz) and in strong accumulation region corresponds to the value of series resistance (R_s) for, metal/insulator/semiconductor (MIS) or metal/oxide/semiconductor (MOS) structures and can be subtracted from the measured C_m and G_m values as following [45].

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \qquad (17)$$

where ω is the angular frequency, C_m and G_m represent the measured capacitance and conductance in the strong accumulation region. According to Eq. (8) at high frequencies, we calculated the voltage dependent R_s values. As seen in Fig. 6, the *R-V* plots give a distinguishable peak from about -4 V to -4 V.
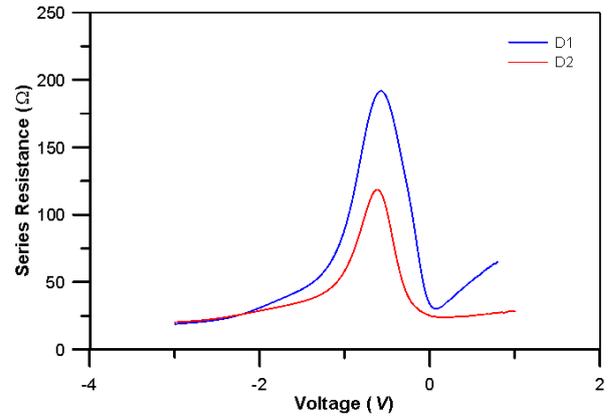
Fig. 6. The voltage dependence of the series for 1 MHz at room temperature.

In this study, frequency dependence of interface states densities were obtained using the Hille-Coleman method which is very useful in understanding the electrical properties of the interface [45]. According to this method, the D_{it} values can be calculated by using the following equation:

$$D_{it} = \frac{2}{qA}\left(\frac{(G_{c,max}/\omega)}{(G_{c,max}/\omega C_i)^2 + (1 - C_c/C_i)^2}\right) \qquad (18)$$

where A is the rectifier contact area, ω is the angular frequency, $G_{c,max}$ is related to the maximum in the corrected G-V curve; and C_c is capacitance to $G_{c,max}$. C_i is the capacitance of interfacial layer [44]. The value of C_i can be obtained from the C-V and G/ω-V measurements in strong accumulation region at high frequency (1 MHz), using the relation [45]

$$C_i = C_m \left[1 + \frac{G_m^2}{(\omega C_m)^2} \right] = \frac{\varepsilon_i \varepsilon_0 A}{d} \qquad (19)$$

We calculated the value of C_i as 40nF and 24nF for diodes D1 and D2 at room temperature (300 K) and 1 MHz, respectively. Using Eq.(16) the values of interface states densities were found as $1.56 \times 10^{13} \text{eV}^{-1}\text{cm}^{-2}$ and $1.317 \times 10^{13} \text{eV}^{-1}\text{cm}^{-2}$ for diodes D1 and D2. The energy distribution of the interface states of the diode changes from 2.44×10^{12} to $1.24 \times 10^{13} \text{eV}^{-1}\text{cm}^{-2}$. Aydogan et. al.[43] found that the deposition of polymers on to the inorganic semi-conductor could generate a large number of interface states at the semiconductor surface, which strongly influenced by the properties of the PANI/p-Si/Al structure. Cakar et.al.[48] have determined the interface properties of Au/PYR-B/p-Si/Al contact. They found that the interface-state density values varied from 4.21×10^{13} to $3.82 \times 10^{13} \text{eV}^{-1}\text{cm}^{-2}$. In another study, Aydin and Turut [49] have investigated the interface-state density properties of the Sn/methylred/p-Si/Al diode and the interface state density was found to vary from 1.68×10^{12} to $1.80 \times 10^{12} \text{eV}^{-1}\text{cm}^{-2}$. It is evaluated that the interface properties of the Al/p-Si junction are changed by depending on the organic layer inserted into the metal and the semiconductor. The organic interlayer appears to cause to a significant modification of interface states even though the organic–inorganic interface appears abrupt and unreactive [50,51]. The MA organic layer increases the effective barrier height clearly upon the modification of the semiconductor surfaces and the chemical interaction at the interface of the MA organic layer to the p-Si and oxide-organic interface states will give rise to new interface states.

4. Conclusions

In summary, we have fabricated and investigated the electrical characteristics of the Al/MA/p-Si MPS Schottky structures formed by coating of the organic material to directly p-Si substrate. It has been seen that the MA thin film on p-Si substrate showed a good rectifying behavior. The forward I-V characteristics of the devices have been analyzed on the basis of the standard thermionic emission theory. The barrier height, the ideality factor and series resistance of the device were calculated from the I-V characteristic and Cheung method.

The frequency dependence capacitance-voltage (C–V-f) and conductance–voltage (G/ω–V-f) characteristics of the metal–polymer–semiconductor (Al/MA/p-Si) SBDs were investigated in the frequency range of 1 MHz at room temperature. The forward and reverse bias (C–V-f)

and (G/ω–V-f) characteristics of the MPS structures show that both capacitance and conductance were quite sensitive to frequency and voltage. Such a behavior of the C and G/ω is attributed to particular distribution of interface states at the polymer interface and series resistance. Series resistance is dependent both frequency and voltage and changes from region to region. This behavior considered that the trap charges have enough energy to escape from the traps at the metal-semiconductor interface in the Si band gap. The real series resistance of MPS structure can be obtained from the C-V and G/ω-V measurements in strong accumulation regions at high frequency (1 MHz). Interface states cannot follow a.c.signal in accumulation region.

It is concluded from experimental results that the location of D_{it} between Si/MA and R_s have a significant effect on electrical characteristics of the Al/MA/p-Si SBDs, which are responsible for the non-ideal behavior of the C–V characteristics. The developed this Al/MA/p-Si MPS type SBD can be used as a good electronic material combination for possible applications. This work declared here recommends that the MA interlayer should be considered, among other organics, as a potential thin film for the novel MIS devices.

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