Electrical characteristics of atomic layer deposited Au/Ti/Al_2O_3/*n*-GaAs MIS structures over a wide measurement temperature

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We have prepared the Au/Ti/Al_2O_3/*n*-GaAs structures and investigated their current-voltage (*I-V*) characteristics with the temperature (in 20-320K range) as a parameter, and current-temperature (*I-T*) characteristics with bias voltage as a parameter. The ultrathin Al_2O_3 metal-oxide layer on the *n*-GaAs substrate has been formed by atomic layer deposition (ALD) method. Ti(10nm) rectifying contacts have been fabricated on Al_2O_3/*n*-GaAs structure by DC magnetron sputtering. The ideality factor value has remained between 1.10 -1.06 from 130 K to 320 K. The barrier height (BH) value has increased with a slope of α = -0.31 meV/K from 320 K to 110 K. Then, it has been seen that the decrease in the BH value from 110 K to 20 K obeys a double Gaussian distribution (GD) of the BHs due to the BH inhomogeneity. The experimental *I-T* characteristics have been interpreted by plotting the theoretical *I-T* characteristics with and without the GD based on the TE current theory at each bias voltage. Moreover, the BH values have been also determined from the Richardson curves plotted using the *I-T* data at each forward and reverse bias voltage. It has been observed that the BH reduction is higher under reverse bias voltage than under forward bias voltage regime due to the barrier inhomogeneity which is not recommended for the Schottky diode being a rectifying device.

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1. Introduction

Metal-semiconductor (MS) rectifying or ohmic contacts are of vital importance for device applications such as photovoltaic solar cells, *p-n* junctions, bipolar transistors, metal-semiconductor field effect transistors (MESFETs) and metal-oxide-semiconductor FETs (MOSFETs) [1-11]. The ultrathin layers formed by atomic layer deposition (ALD) have found applications such as buffer layers for the growth of high quality materials in the formation of thin films and insulators for thin film transistors, interfacial layers for MOSFET transistors and high-electron mobility transistors, surface passivation layers of channel-FETs [4-13]. The ALD is a vapor-phase thin film deposition method characterized by alternating exposure cycles of chemical species with self-limiting surface reactions. The films with accurate and excellent thickness control and uniform over large substrate areas can be produced by the ALD method [1-3]. As interfacial layer, the metal-oxide Al_2O_3 is an attractive candidate with a dielectric constant of 9.1 and a wide band-gap of 6.6 eV [1, 2, 9-11]. Integration of ALD oxides with GaAs or other inorganic semiconductors enables lower gate leakage currents, high breakdown voltages, and improved surface passivation [1-6].

We have prepared the Au/Ti/Al_2O_3/*n*-GaAs MIS structures utilizing ALD-grown Al_2O_3 metal oxide interfacial layer. Ti(10 nm) Schottky contacts were made using magnetron DC sputter technique, and Au(50 nm) metallic layer was evaporated as a top layer on the Ti/*n*-GaAs structure in high vacuum system of 10^{-6} Torr. Au thin films are more often used as a top layer to protect other metallic layers and as cap-layer to prevent the oxidation of the Schottky metal. We have investigated the current-voltage characteristics (*I-V*) in the measurement temperature range of 20-320 K with steps of 10 K. Furthermore, the current versus temperature (*I-T*) characteristics have been also investigated with bias voltage as a parameter in the measurement temperature range of 20-320 K. Furthermore, the fact that he BH value sharply decreases due to the barrier height inhomogeneity from 110 K to 20 K has been explained by a double Gaussian distribution (GD) of the BHs. Moreover, the barrier height (BH) values have been also determined from Richardson curves at each forward and reverse bias voltage. Thus, the BH versus bias voltage plots have ben been drawn and established the BH reduction versus band bending (V_{bb}) plots for reverse and forward bias voltage. Thus, one might reach the conclusion how the BH reduction occurs under forward bias or under reverse bias.

As known, an ideal rectifying device needs a low-barrier contact under forward bias and a high-barrier contact under reverse bias [12,13], that is, the effective BH should be higher under reverse bias than under forward bias, but an inhomogeneous Schottky contact may behave like a high-barrier contact under forward bias and a low-barrier contact under reverse bias due to the pinch-off effect which is not recommended for the Schottky diode as a rectifying device [12,13].

2. Experimental details

The Au/Ti/Al_2O_3/*n*-GaAs MIS structures were fabricated using *n*-type single crystals GaAs wafer with (100) surface orientation, having thickness of 300 μm, $6.8x10^{15}$ cm^{-3} carrier concentration (N_D) and 1.2 Ω cm resistivity (given by the manufacturer). Before the SBDs fabrication process, the samples were ultrasonically degreased by dipping into acetone for 2 minutes and in propanol for 2 minutes, respectively and then, rinsed in DI water of resistivity of 18 MΩ cm and dried under N_2 flow. After surface cleaning of *n*-GaAs, high purity Indium (99.999%) with a thickness of about 2000 Å was coated to the back of the *n*-GaAs wafer for making ohmic contacts by the thermal evaporation at a base pressure about 10^{-6} Torr. Low ohmic contact to *n*-GaAs was obtained by annealing at 385 ^{0}C for 3 min under dry nitrogen flow. The ALD of Al_2O_3 thin films was carried out in Cambridge Nanotech Savannah 100 reactor. The Al_2O_3 deposition was performed at 200 ^{0}C, using trimethylaluminum (TMA) (Al precursor), and water (oxygen precursor), for a total of 30 cycles. Standard photolithography technique was used for pattern fabrication on GaAs. Ti(10 nm) Schottky contacts were made using magnetron DC sputter technique, and Au(50 nm) to protect the Ti metallic layer was evaporated as a top layer on the Ti/*n*-GaAs structure in high vacuum system of 10^{-6} Torr. Finally the photoresist was removed by washed with DI water and then with N_2. All the electrical characterizations were carried out using Keithley 2400 current source and 6514 electrometer.

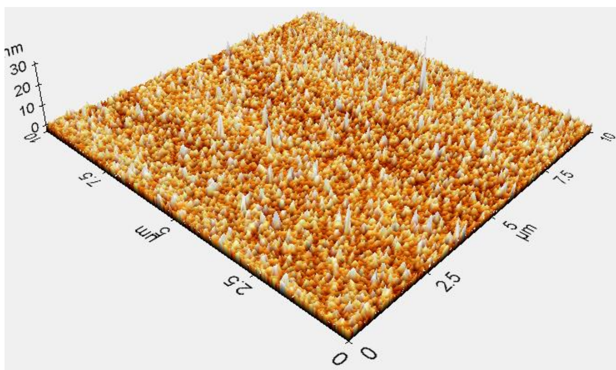

Fig. 1. AFM surface image with 3D for 3 nm thick Al_2O_3 layer on the GaAs substrate

Temperature-depended measurements were carried out using ARS closed cycle helium cryostat in 20-320K range. Surface roughness was measured using Nano-Magnetics-AFM with tapping mode. Fig. 1 shows the AFM surface image with 3D for ~3 nm thick Al_2O_3 layer on GaAs substrate. The Al_2O_3 layer surface on GaAs has root-mean-square (RMS) roughness value of 0.904 nm which is a reasonable smooth.

3. Results and discussion

Fig. 2 shows the current-voltage (*I-V*) characteristics of one of the Au/Ti/Al_2O_3/*n*-GaAs MIS structures in the measurement temperature range of 20-320 K. The reverse bias current could only be measured in temperature range of 240-320 K because the reverse current is below the detection limit of the *I-V* measurement equipment at lower temperature. It is assumed that the forward bias current through a thin interfacial layer is due to thermionic emission current and it can be expressed as [14-16]

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] , \quad (1)$$

where

$$I_0 = SA^* \kappa_n T^2 \exp\left(-\frac{q\Phi_b}{kT}\right) , \quad (2)$$

is the saturation current density, Φ_b is the effective barrier height at zero bias in a SBD without the interfacial layer, n is an ideality factor, A^* is the effective Richardson constant and equals to 8.16 $Acm^{-2}K^{-2}$ for *n*-type GaAs, S is the Schottky contact area, κ_n is the transmission coefficient the across interfacial layer and is given by

$$\kappa_n = \exp\left(-\frac{4\pi\delta}{h}(2m^* \chi)^{1/2}\right) = \exp\left(-a\delta(\chi)^{1/2}\right), \quad (3)$$

where $a\delta(\chi)^{1/2}$ is the electron tunneling factor, $a = \frac{4\pi}{h}(2m^*)^{1/2}$ is a constant dependent on effective mass, $m^*= 0.067m_o$ is the effective tunneling mass of electrons, χ is the effective BH presented by the thin interfacial layer or the energy difference between the conduction band edges of the semiconductor and the interfacial layer, and δ is the thickness of the interfacial layer. Eq.(1) and thus Eq.(2) are the standard TE equation for Schottky barriers except for the term $\exp\left(-a\delta(\chi)^{1/2}\right)$ which is the tunneling probability. If the interfacial layer is extremely thin and is transparent to electron, then $\kappa_n \approx 1$. Then, Eq.(2) can be written as [14-16]

$$I_0 = SA^*T^2 \exp\left(-\frac{q\Phi_b}{kT}\right)\exp\left(-a\delta(\chi)^{1/2}\right) ,$$

$$kT\ln\left(\frac{A^*ST^2}{I_0}\right) = q\Phi_b + akT\chi^{1/2}\delta \quad (4)$$

In the usual analyses of the experimental data on Schottky contacts, the BH value is determined from the extrapolated I_0. However, this is an apparent barrier height $q\Phi_{b0}$ when an interfacial layer is present. The effective or measured barrier height $q\Phi_{b0}$ is given by

$$q\Phi_{b0} = kT\ln\left(\frac{A^*AT^2}{I_0}\right) , \quad (5)$$

where $\Phi_{b0} = \Phi_{b0}(T)$ is the effective barrier height at zero bias for a SBD with the interfacial layer at each measurement temperature. Thus, from Eqs.(4) and (5), we have

$$q\Phi_{b0}(T) = q\Phi_b + akT\chi^{1/2}\delta . \quad (6)$$

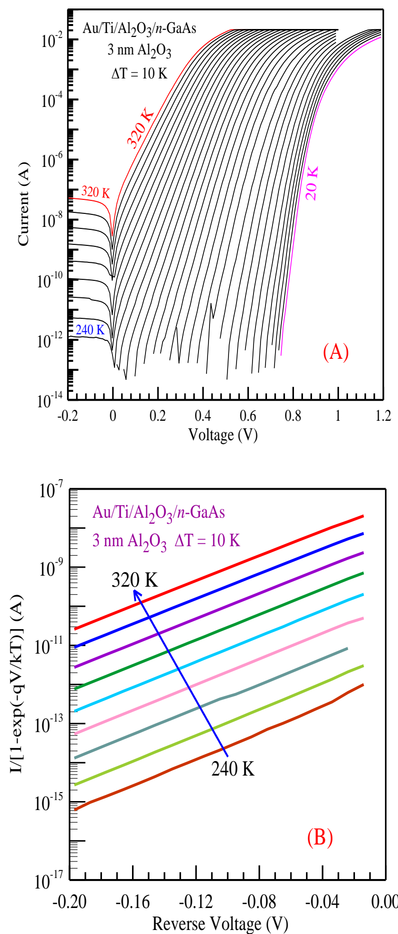

Fig. 2. (A) Forward bias current-voltage curves for the Au/Ti/A$_2$O$_3$/n-GaAs structure in the temperature range of 20-320 K with steps of 10 K and the reverse bias current-voltage curves range from 240 to 320 K with steps of 10 K. (B): Semi-logarithmic {I/[1-exp(-qV/kT)]} versus V plots from the reverse bias I-V data in Fig. 2 (A)

The presence of a linear region over several orders of magnitude in the *I-V* semi-log plot can be clearly seen from the temperature-dependent forward bias *I-V* curves in Fig. 2 (A). The deviation of the linearity at high voltages can be attributed to the series resistance coming from the neutral region between the ohmic contact and depletion layer plus Al_2O_3 oxide layer. The ideality factor n values are determined from the slopes of the forward-bias *lnI* vs *V* plot using Eq.(1). Fig. 3 shows BH versus temperature plot (*solid squares*) and ideality factor versus temperature plot (*open squares*) for the device. The ideality factor value of the device has remained almost constant between 1.10-1.06 in the temperature range of 130-300 K (Fig. 3). Therefore, it can be concluded that the forward bias *I-V* characteristics follow the well-known thermionic emission (TE) equation in about 130-320 K range. [16-30]. The low values of the ideality factor suggest that the current flow across the device is dominated by the thermionic emission over the BH in this temperature range because the Al_2O_3 interfacial layer is very thin. As stated in [18], the sputtering can help to remove the defect filled oxide layer and to increase the diode quality. Therefore, the improvement should be expected from the Al_2O_3 interfacial layer between Au/Ti and the GaAs substrate. That is, one can expected a passivation effect of the Al_2O_3 layer and the sputter cleaning effect of the surface of the GaAs substrate.

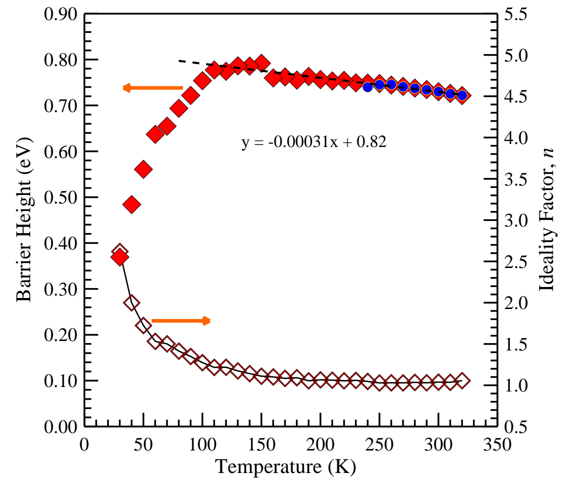

Fig. 3. Barrier height versus temperature plot, the data indicated by solid squares from the forward bias saturation currents in Fig. 2 (A), and the data indicated by solid circles from the reverse bias I-V data in Fig. 2 (B), and ideality factor versus temperature plot (open squares)

The BH values indicated by open triangles in Fig. 3 have been calculated from the intercept of the linear portion of the forward bias *I-V* plot using equation (2). The BH value has linearly increased from 0.72 eV at 320 K to 0.79 eV at 110 K and then has decreased from 0.79 eV at 110 K to 0.37 eV at 20 K. The linear increase in BH value from 320 to110 K can be attributed to the temperature dependence of the BH or n-GaAs band gap. The BH temperature coefficient, α, is calculated from the linear

portion by $\Phi_{b0}(T) = \Phi(T{=}0) - \alpha T$. The fitting to $\Phi_{b0}(T)$ data yields a straight line with the slope of α = -0.31 meV/K. The decrease in the BH value from 110 K to 20 K can be ascribed to the barrier height inhomogeneity which is active especially at low temperature [19-27].

Fig. 2 (B) shows the semi-logarithmic {I/[1-exp(-qV/kT)]} versus V plots [14] from the reverse bias I-V data in the temperature range of 240-320 K in Fig. 2 (A) for the device. The curves in Figure 2 (B) were formed for calculating the zero bias reverse bias BH values. The zero bias reverse bias BH value at each temperature was determined from the intercept of the reverse-bias ln{I/[1-exp(-qV/kT)]} versus V curves using eqn.(1). The data indicated by solid circles in Fig. 3 belong the zero bias reverse bias BH values in the temperature range of 240-320 K. The zero bias BH values from the forward and reverse bias I-V characteristics coincide with each other which indicates the elimination or minimization of the polarity from ions between the Al_2O_3 layer and GaAs substrate. [31-34].

The double linearity of the $\Phi(T) = \Phi_{b0}(T)$ versus $(kT)^{-1}$ and $(n^{-1}$-1) versus $(kT)^{-1}$ plots for the BH and ideality factor values at temperatures below 130 K in Fig. 4 says that the decrease in the BH with decreasing temperature may be explained in terms of a double Gaussian distribution (GD) of the Schottky BHs with the mean BH $\overline{\Phi}_b$ and standard deviation of the distribution, σ_{s0} [19-28]. This model is incorporated on the concept of the spatially inhomogeneous BHs and potential fluctuations at the interface and on a TE mechanism with the GD function. The GD of the BHs yields the following expression for the BH [35-37]:

$$\Phi_{b0}(T) = \overline{\Phi}_{b0} - \frac{q\sigma_{s0}^2}{2kT} \quad (7)$$

where $\Phi_{b0}(T)$ is the zero-bias BH obtained from the experimental forward bias I-V characteristics (Fig. 2) at each temperature. The variation of the experimental ideality factor $n(T)$ with temperature is given by [35, 36]

$$\left(\frac{1}{n(T)} - 1\right) = -\beta_1 + \frac{q\beta_2}{2kT} \quad , \quad (8)$$

where parameters β_1 and β_2 represent the voltage deformation of the BH distribution at an inhomogeneous interface. β_1 is the voltage coefficient of the mean BH $\overline{\Phi}_b$, and β_2 is the voltage coefficient of the standard deviation. The parameters have been obtained from the intercept and slopes of the linear fits to linear regions in Fig. 4 which are plotted from the ideality factor and BH values in 20-130 K range. The $\Phi(T)$ vs $(2kT)^{-1}$ and $(n^{-1}$-1) versus $(kT)^{-1}$ plots in Fig. 4 give values of $\overline{\Phi}_{bo}$ = 0.96 eV, σ_{s0} = 61 mV and the β_1= -0.126 and β_2= -0.0026 V for the straight lines on the left side of the graphs in Fig. 4, respectively. Similarly, in Fig. 4, the straight lines on the right side give values of $\overline{\Phi}_{bo}$ = 0.85 eV, σ_{s0} = 50 mV and β_1= -0.08 and β_2= -0.0051 V, respectively.

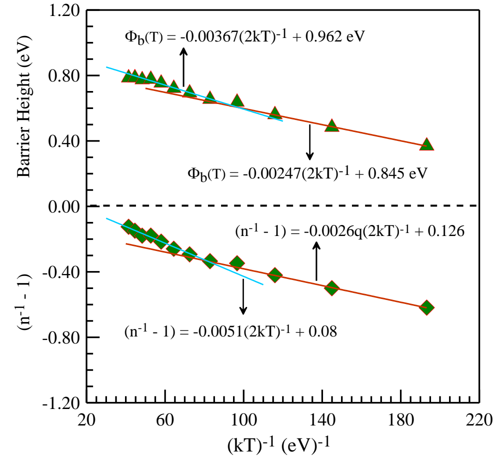

Fig. 4. Experimental apparent barrier height from the saturation currents and ideality factor versus $(2kT)^{-1}$ plots according to the Gaussian distributions in the temperature range of 20-130 K

From Eqs.(6) and (7), the voltage-independent and voltage-dependent BH can be written as

$$\Phi_b(T) = \overline{\Phi}_{b0} - \frac{q\sigma_s^2}{2kT} + akT\chi^{1/2}\delta \quad (9)$$

$$\Phi_b(V,T) = \overline{\Phi}_{b0} - \frac{q\sigma_s^2}{2kT} + \left(\beta_1 - \frac{q\beta_3}{2kT}\right)V + akT\chi^{1/2}\delta \quad (10)$$

respectively. The presence of an interfacial layer at MS interface has been also taken into account here [Eqs. (9), (10)]. This bias dependence of BHs in the distribution through mean BH and standard deviations leads to the bias-dependent ideality factor in inhomogeneous Schottky diodes [35-45].

Fig. 5 shows the experimental current versus temperature curves with the applied voltage as a parameter for the device. The bias voltage ranges from 0.038 V to 0.647 V with steps of about 0.04 V and from 0.647 V to 0.988 V with steps of about 0.03 V. As seen from the I-V curve at each temperature in Fig, 2, the deviation of linearity or the downward concavity due to the series resistance begins at 0.72 V for 100 K and at 0.84 V for 20 K. Therefore, we can be said that the portion above 0.84 V of the experimental current versus temperature curves in Fig. 5 only reflect the temperature-dependent behavior of the GaAs bulk plus the Al_2O_3 layer. That is, when Fig. 5 is considered together with Fig. 2, it can be said that the current versus temperature curves in Figure 5 are affected from the series resistance of the GaAs bulk plus the Al_2O_3 layer above ~10^{-3} A.

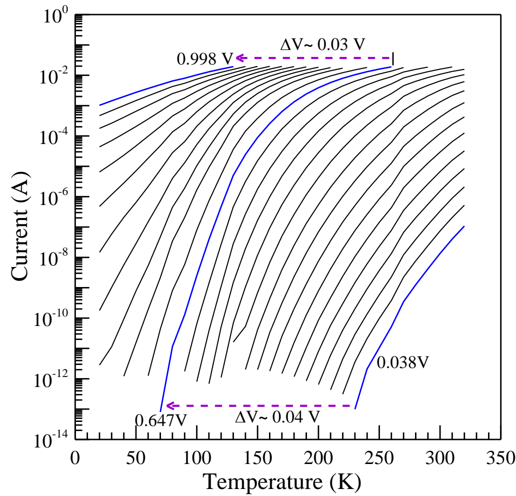

Fig. 5. Experimental Current versus temperature plots as a function of the applied forward voltage

Before interpreting the temperature-dependent behavior of the experimental current curves, let us study to obtain the theoretical *I-T* curves at each bias voltage using Eq.(6) or (9) or (10) in Eq.(1). The obtained theoretical curves are given in Figs. 6 and 7. When considering the theoretical calculations, it is seen that the mean BH $\overline{\Phi}_{b0}$ in Eq.(9) is constant and the second term on the right side in the equation increases with a decrease in the temperature, therefore the apparent BH value decreases with decreasing the temperature. The apparent BH in Eq.(6) is the temperature-dependent due to the second term on the right side in the equation, therefore the apparent BH value decreases with decreasing the temperature. However, the contribution of this term to the apparent BH value increases with increasing temperature, for example 2.24x10^{-3}, 9.21x10^{-3} and 1.41x10^{-2} eV for χ = 0.032 eV at 20 K, 60K and 130 K, respectively.

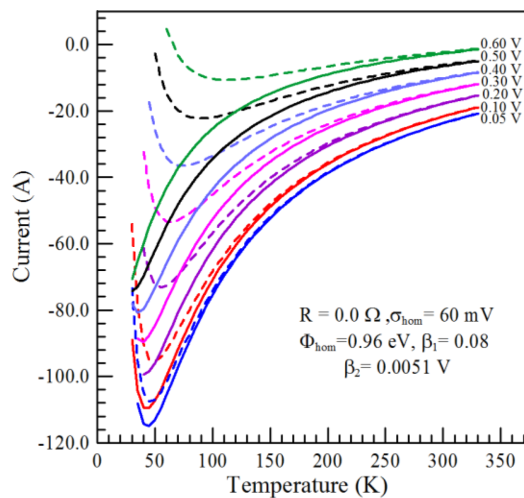

Fig. 6. Theoretical current versus temperature curves as a function of the applied voltage using eqn. (9) or (10) in eqn. (1), dashed lines for eqn. (9), and solid lines for eqn.(10)

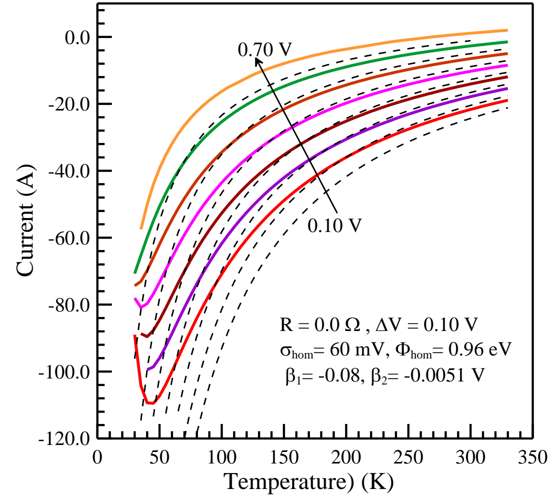

Fig. 7. Theoretical current versus temperature curves as a function of the applied voltage using eqn. (6) or (10) in eqn.(1), dashed lines for eqn.(6) or for TE equation, and solid lines for eqn.(10).

As can be seen from the theoretical curves in Figs. 6 and 7, the current at each bias increases with increasing temperature which is in good agreement with the thermal activation mechanism of a Schottky diode [36-50] and it trends to saturate after a given temperature although R=0. That is, the saturation behavior of the current in Figure 6 and 7 at high temperatures is not only due to the series resistance. When the experimental *I-T* curves at each bias voltage in Fig. 5 are compared with the corresponding theoretical *I-T* curves in Figs. 6 and 7, it is seen that the shape of the experimental *I-T* curves is similar to that of the curves plotted using Eq.(10) in Fig. 7.

However, the apparent BH in Eq.(10) is the bias-dependent due to the third term on the right side in the equation, and therefore, the disruptions resulting in the Eq.(9) are compensated at least partially as Eq.(10) has been used. It is clearly seen from Fig. 6 that the curves with the dashed line are generated using Eq.(9) and the curves with the solid lines are obtained using Eq.(10). The current curves with dashed line in Figure 6 increase with the decrease of temperature at low temperature region, that is, it shows the negative thermal activation behavior. As can be seen from the current curves in Fig. 6, the negative thermal activation behavior in the current curves with dashed line is compensated at least partially in the solid-line current curves plotted using Eq.(10), due to the bias-dependent third term on the right side in Eq.(10).

Fig. 8 shows the theoretical Richardson ln(I/T^2) versus $(kT)^{-1}$ curves with the forward bias voltage as a parameter. The curves with the dashed line and solid line in the figure have been obtained using Eqs.(6) or (10) in Eq.(1) respectively.

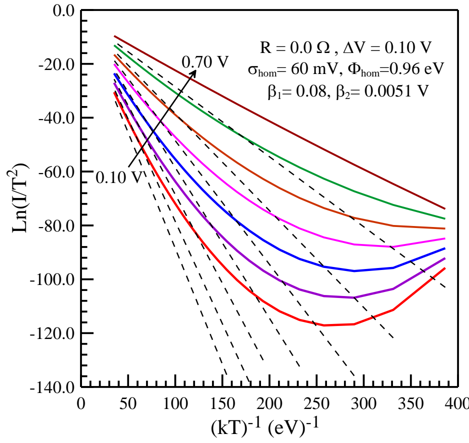

Fig. 8. Theoretical Richardson curves as a function of the applied voltage using eqn. (6) or (10) in eqn.(1) in the temperature range of 30-230 K, dashed lines for eqn.(6) or for TE equation, and solid lines for eqn.(10)

The theoretical Richardson curves in Fig. 8 have been plotted for the interpretation of the experimental Richardson curves in Fig. 9. As mentioned above, if $\Phi_b(V,T)$ given in Eq.(10) is used in place of Φ_b in Eq.(1), then Eq.(1) is called the modified TE current equation with the GD function which is given for Schottky contacts with the spatially inhomogeneous. As can be seen from Fig. 8, the theoretical curves with the solid line below 0.70 V deviate of the linearity in at low temperatures, but they trends to be linear with increasing bias voltage over the whole measurement temperature for all bias voltages above 0.60 V. When the bias-independent BH equation (9) was used, an excessive deviation from linearity is observed at low temperatures and at high bias voltages (these plots are not given here). It has been mentioned above that the experimental apparent BH (Fig. 4) determined from the saturation current (V=0 volts) for each temperature (Fig. 2) decreases with decreasing temperature obeying to the Gaussian distribution of the BHs in the temperature range of 20-130 K.

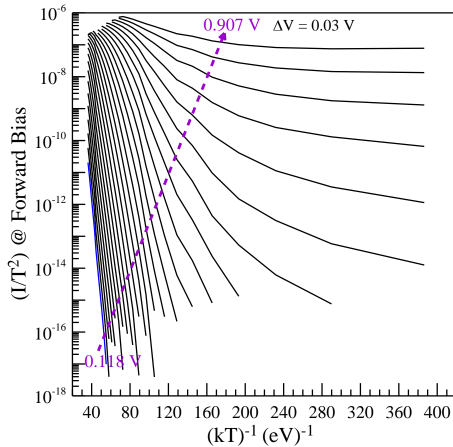

Fig. 9. Experimental Richardson (I/T^2) versus $(kT)^{-1}$ plots as a function of the forward applied voltage in the temperature range of 40-320 K

Thereby, the explanations above for Figs. 4 and 8 or Fig. 10 should be not confused with each other. As can be seen, Fig. 10 shows the experimental (indicated with triangles) and theoretical (the dashed lines) Richardson (I/T^2) versus $(kT)^{-1}$ curves for the forward applied voltage of 0.756 and 0.786 V. Thus, it can be said that the deviation of the linearity observed at low temperatures and high bias voltages in the experimental Richardson curves may be attributed to the fact that the current through the diode flows preferentially through the lower barrier-small local regions called as the patches [12, 13, 38-50].

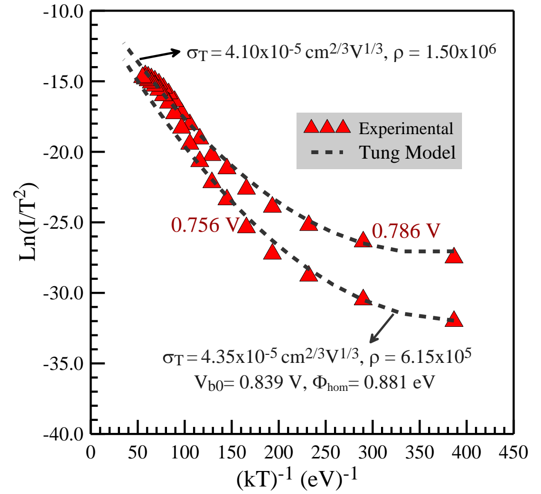

Fig. 10. Richardson (I/T^2) versus $(kT)^{-1}$ plots at the forward applied voltage of 0.756 and 0.786 V, Triangles: the experimental data, the dashed lines: theoretical curves according to patch model [12]

According to Tung's model, the TE current expression can be modified for the case of a configuration of low circular BH-patches [12, 13]. Thus, the current through the junction formed from the low-SBH patches can be approximately described as [12]:

$$I = A_{eff}\rho A^* T^2 \exp\left(-\frac{\Phi_{eff}}{kT}\right)\left[\exp\left(\frac{(V-IR_s)}{kT}\right)-1\right] \quad (11)$$

Thus, we have rewritten Eq.(1) for the total current flowing through the diode taking into account the effective area of the diode given by ρA_{eff}, ρ is the number of patches covering area of the diode as free parameter, the product ρA_{eff} represents the value of the total effective area of the patches contributing to the current transport. The effective area of a low-BH patch A_{eff} can be expressed as [12]

$$A_{eff} = \frac{8\pi\sigma_T^2}{9}\left(\frac{\eta}{V_{b0}-V}\right)^{1/3} \quad (12)$$

However, according to Tung's patch model, the ideality factor and effective BH are given by [12]

$$n \approx 1 + \frac{\sigma^2 (V_{b0} - V + IR_s)^{-1/3}}{3kT\eta^{2/3}}, \qquad (13)$$

$$\Phi_{eff} = \Phi_{\text{hom}} - \frac{\sigma^2}{2kT}\left(\frac{V_{b0} - V + IR_s}{\eta}\right)^{2/3}, \qquad (14)$$

respectively, where Φ_{hom} is the homogeneous BH, $\eta = \varepsilon_s\varepsilon_o/qN_d$, ε_s and N_d are the dielectric constant and the dopant density of the semiconductor substrate. V_{b0} is the zero bias band bending of the uniform barrier. As can be seen from Eq.(12), A_{eff} depends on the bias voltage. For small and circular patches, Tung [12] assumes a GD of low-SBH circular patches characterized by a distribution with standard deviation σ_T and the interaction of the patch with the surrounding depletion region causes a pinch-off or saddle point in the potential barrier away from the interface [12, 13 ,17]. Fig. 10 has been plotted by considering Eqs.(11)-(14) according to Tung's model [12]. A lateral homogeneous BH value of 0.88 eV has been used in the equations above. The dashed lines in Figure 10 display the modeling to the experimental Richardson (I/T^2) versus $(kT)^{-1}$ curves at the forward voltages of 0.756 and 0.786 V. It has been obtained the values of 4.35x10^{-5} cm$^{2/3}$V$^{1/3}$, 1.44x10^{-11} cm^2 and 6.15x10^5 for σ_T, A_{eff} and ρ at 0.756, respectively, the values of 4.10x10^{-5} cm$^{2/3}$V$^{1/3}$, 1.14x10^{-11} cm^2 and 1.50x10^6 at 0.786 V, respectively. Furthermore, the effective area of the diode, ρA_{eff}, has been obtained as 8.24x10^{-6} cm^2 and 1.71x10^{-5} cm^2 for 0.756 and 0.786 V, respectively, because A_{eff} depends on the bias voltage. The Eq.(11) was modeled with number generation for varying parameters of σ_T, A_{eff} and ρ with Mathcad software. We did not use the fitting methods with error analysis because the equation involves same parameters in exponential part. So the iterative approach with fitting methods is not successive for this case.

The linear portion of each experimental curve in Fig. 9 has been chosen for obtaining the bias-dependent BH, and thus Fig. 11 has been generated. Similarly, the Richardson (I/T^2) versus $(kT)^{-1}$ curves have been also plotted for calculating the reverse bias dependent BH. The reverse bias-dependent BH versus bias voltage plot is given in the inset of Fig. 12. The forward bias-dependent BH versus bias voltage plot is given in Fig. 13. Moreover, the inset of Fig. 12 also shows the band bending (V_{bb}) versus reverse applied voltage plot. The temperature dependence of the Fermi potential in the calculations was neglected, and the value of V_n= 0.11 V at 300 K was only used. From the minimum and maximum values of 0.71 eV and 0.83 eV, a mean value of 0.79 eV with a standard deviation value of 46 meV has been obtained from the reverse bias-dependent BH data in Fig. 12. From the minimum and maximum values of 0.85 eV and 0.93 eV, a mean value of 0.87 eV with a standard deviation value of 19 meV has been obtained from the forward bias-dependent BH data in Fig. 13.

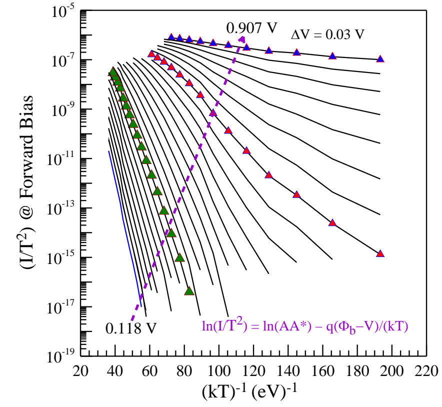

Fig. 11. Experimental Richardson (I/T^2) versus $(kT)^{-1}$ curves plotted by taking for calculation of the barrier height at each forward bias voltage

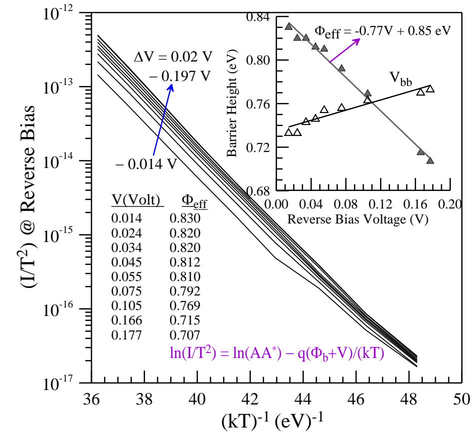

Fig. 12. Experimental Richardson (I/T^2) versus $(kT)^{-1}$ plots as a function of the reverse applied voltage for Au/Ti/A_2O_3/n-GaAs structure. The inset shows barrier height and band bending (V_{bb}) versus reverse applied voltage plot. Fermi potential V_n = 0.11 V at 300 K. The temperature dependence of the Fermi potential was neglected here.

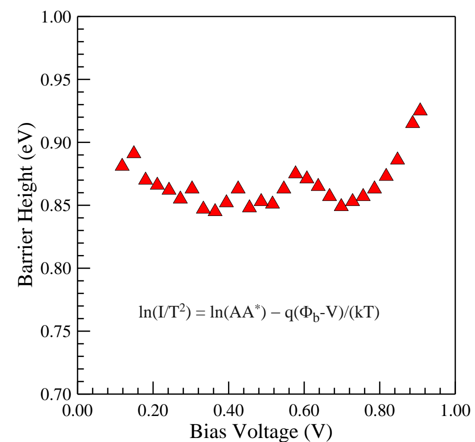

Fig. 13. Barrier Height as a function of the forward applied voltage from experimental Richardson (I/T^2) versus $(kT)^{-1}$ plots in Fig. 11

In the reverse bias case, the effective BH decreases with the voltage, leading to unsaturated reverse current, as can be seen in the inset of Fig. 12. As mentioned in refs.[12, 13, 17], the saddle-point potential energy increases with an applied forward bias and decreases with the reverse bias [12, 13, 17]. An increase in the effective SBH is due to rise in the saddle point potential under forward applied bias that controls the current transport with the applied voltage [12, 13]. That is, the model [12, 13] says that the effective BH is higher under forward bias than under reverse bias. The effective area of a low-BH patch A_{eff} is about obtained as 1.34×10^{-11} cm^2 at 0.0 V from data above, thus a small circular patch radius = 13.11 nm using the modeling parameters on Figs. 14 and 15. This patch radius value is about 30 times lower than the depletion layer width w. The diffusion potential distributions for patches can be determined using equation (6) in ref.[12]. Fig. 14 shows the diffusion potential distributions for patches with various Schottky BH difference, from the barrier difference of 0.0 V to the barrier difference of 0.35 V with the steps of 0.05 V, as a function of the distance z from the MS interface towards the semiconductor. The critical value of the barrier difference for the potential pinch-off is about 0.052 V here. As well-know, when the BH difference is less than critical value, there is no potential pinch-off. As can be seen from Fig. 14, the pinch-off degree increases with an increase in the barrier height difference. Fig. 15 shows the diffusion potential distributions of low-SBH circular patches for different bias voltages across the MS contact, from the reverse bias of -0.30 V to forward bias of 0.30 V with the steps of 0.10 V, as a function of the distance z from the MS interface towards the semiconductor. As seen from the Figure, the saddle point potential slowly increases with increasing forward bias, and slowly decreases with reverse bias. Ru et all. [13] have showed that the pinch off is stronger under forward bias voltage than under reverse bias voltage, considering the model of Tung [12].

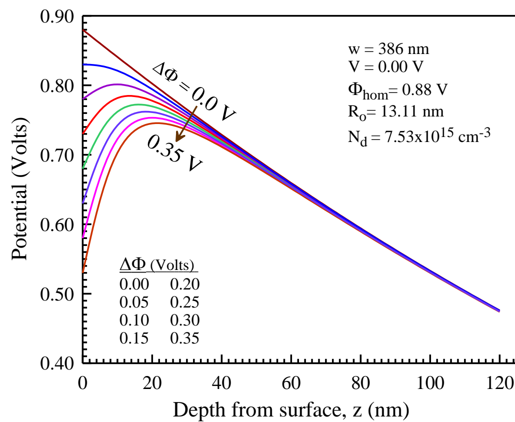

Fig. 14. Diffusion potential distributions for low-SBH circular patches with various Schottky barrier height difference, the barrier difference of 0.0 V to the barrier difference of 0.35 V with the steps of 0.05 V, as a function of the distance z from the MS interface towards the semiconductor

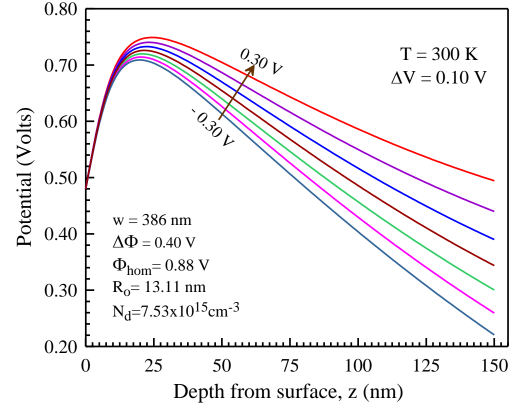

Fig. 15. Diffusion potential distributions for low-SBH circular patches patches under the bias voltage, from the reverse bias of -0.30 V to forward bias of 0.30 V with the steps of 0.10 V, as a function of the distance z from the MS interface to the inside of the semiconductor

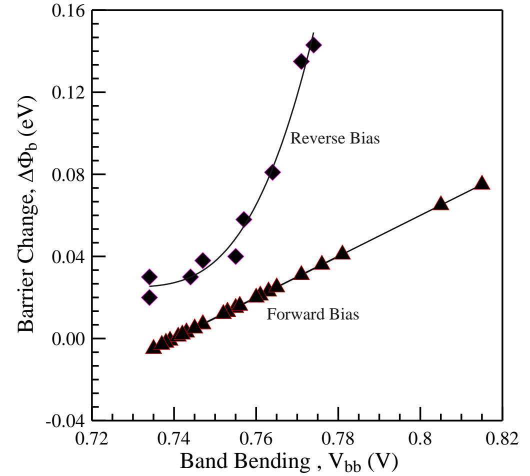

Fig. 16. Experimental Barrier Height versus band bending curves from the bias dependent forward and reverse bias barrier height data in Figures 10 and 11 plots for Au/Ti/A_2O_3/n-GaAs structure

We can now give the BH reduction or change with the reverse and forward bias from the above information in Fig. 16. It has been seen from Fig. 16 that the BH reduction is higher under reverse bias voltage than under forward bias voltage. The results we have found for the Au/Ti/Al_2O_3/*n*-GaAs structure are in agreement with those for NiSi/*n*-Si Schottky diodes [13] and with the model of Tung [12] who suggest that the pinch off is stronger under forward bias voltage than under reverse bias voltage. However, it has been desired from a technological point of view that a device always should be a low-barrier rectifying contact under forward bias voltage and a high-barrier rectifying contact under reverse bias voltage. Thus, it can be said that the pinch-off effect is not recommended for the Schottky diode as a rectifying device because the pinch-off model says that an inhomogeneous Schottky contact behaves like a high-barrier contact under forward

bias voltage and a low-barrier contact under reverse bias voltage [12, 13].

4. Conclusions

It has been observed from the experimental results above that the *I-V* characteristics of the device have followed the TE current model in 130-320 K range which is confirmed by the ideality factor values in 1.10-1.06 range although the device is a MIS SBD with the Al_2O_3 interfacial layer. While the BH value from the forward bias *I-V* characteristics has increased with the slope of α = -0.31 meV/K in 110-320 K range, and it has decreased obeying the GD of barrier heights based on the modified TE current equation in the temperature in 20-110 K range. In the current-temperature (*I-T*) curves at each bias voltage, the current has increased with increasing temperature and tend to saturate at further temperatures. The experimental results have shown that the barrier height strongly depends on the spatial barrier inhomogeneity and thus the bias voltage. We have shown that the shapes of the experimental *I-T* curves at each bias voltage are in similarity with those obtained from the modified TE with GD and conventional TE current models. However, the forward and reverse bias-dependent BH data from the *I-T* curves have shown that the device behaves like a high-barrier contact under forward bias voltage and a low-barrier contact under reverse bias voltage due to the inhomogeneous Schottky barrier height which is understandable with patch pinch-off effects based on Tung's model.

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