Electrical characterization of Au/ZnO/TiO_2/n-Si and (Ni/Au)/ZnO/TiO_2/n-Si Schottky diodes by using current-voltage measurements

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In this study, we fabricated two types Schottky diodes (SDs), Au/ZnO/TiO_2/n-Si (MIS-1) and (Ni/Au)/ZnO/TiO_2/n-Si (MIS-2), to investigate main electrical parameters such as ideality factor (n), barrier height (Φ_b), interface states (N_{ss}) and series resistance (R_s). ZnO/TiO_2 thin film was deposited on polycrystalline n-type Si substrate using DC magnetron sputtering system. The analysis of current-voltage (I-V) measurements of ZnO/TiO_2/n-Si Schottky diodes (SDs) were performed with two different rectifier contacts as Au and Ni/Au at room temperature. The values of n, Φ_b and R_s were calculated as 1.80, 0.88 eV and 106.12 Ω for MIS-1 and 1.97, 0.82 eV and 50.13 Ω for MIS-2 SDs, respectively, from forward-bias I-V curves. The energy distribution profile of N_{ss} for both SDs was obtained from the forward bias I-V measurements by taking the bias dependence of the effective barrier height (Φ_e) into account. In addition, the values of Φ_b and R_s of MIS-1 and MIS-2 SDs were determined using Cheung's and Norde's functions and the obtained results have been compared with each other.

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1. Introductıon

There are recently a vast number of reports of experimental studies for metal-semiconductor (MS) and metal-insulator-semiconductor (MIS) SDs which play an important role in modern device technology [1-23]. The performance of SDs depends on electrical parameters such as ideality factor, barrier height formation at M/S interface, series resistance and interface states. Electronic properties of SDs are characterized by these parameters. In general, the forward bias I-V characteristics of MIS structure are linear on a semi-logarithmic scale at a low bias voltage but deviate considerably from linearity due to the effect of interfacial insulator layer, N_{ss} and R_s when the applied bias is sufficiently large [1,5].

In MIS type diodes, interfacial insulator layer between metal and semiconductor such as ZnO, TiO_2, SiO_2, SnO_2, Si_3N_4, ZrO_2 and HfO_2, which are high dielectric constant (high-k) materials, have been widely used [1-9]. Among these insulator layer materials, ZnO and TiO_2 are a large band-gap (approximately 3.2 eV) semiconductor materials which have been used in many optical and electrical device applications such as antireflection coatings, solar cells, optical filters and thin film gas sensor [1,8,24-29]. Thin films of ZnO and TiO_2 can be obtained through deposition by a various techniques such as sputtering, chemical vapor deposition and sol-gel methods [1,6-8,25-27]. The sputtering technique is widely utilized because of being capable of obtaining uniform, dense and precise stoichiometric these thin films [30]. Fabricating high quality metal contact to ZnO is essential for the performance and reliability of Schottky diode based devices [24].

In this study, the main electrical parameters of Au/ZnO/TiO_2/n-Si and (Ni/Au)/ZnO/TiO_2/n-Si SDs have been investigated at room temperature using forward bias I-V measurements. The values of n, Φ_b and R_s were obtained from I-V curves, Cheung's function [31] and Norde's function [32]. In addition, the density of interface states as a function of E_c-E_{ss} was obtained from I-V measurements.

2. Experimental Procedure

TiO_2 and ZnO thin films were deposited on 350 μm thickness, 0.01 Ω.cm resistivity and phosphorus doped (n-type) polycrystalline Si substrates using DC magnetron sputtering system, respectively. For the fabrication process, Si wafer was decreased in organic solvent of $CHClCClL_2$, CH_3COOH and CH_3OH, etched in a sequence of H_2SO_4 and H_2O_2, 25 % HF, a solution of 7 HNO_3:1HF:40H_2O, 25 % HF and finally quenched in de-ionized water with resistivity of 18 MΩ-cm for a long time. Latter to cleaning and etching steps, the Si substrate's back surface was mounted onto the stainless steel holder and loaded into the DC magnetron sputtering system. Before the TiO_2 and ZnO deposition, the ohmic contact was formed by deposition of high purity Au (99.999%) at 400 ^oC under $2x10^{-6}$ torr vacuum and the sample was annealed at 375 ^oC to achieve good ohmic contact behavior. Then, the substrates were also tested to see whether or not it has a good ohmic contact behavior.

The substrate was replaced to upper surface immediately after the forming Au back ohmic contacts. Firstly, TiO_2 thin film with thickness of 1500 Å was deposited using high purity (99.999%) Ti target, under specific Ar+O_2 reactive gas mixture (Ar/O_2=90/10 sccm) controlled with mass flow controllers. Then, ZnO thin film with thickness of 150 Å was deposited using high purity (99.999%) ZnO target. After then, the substrate temperature and the pressure was set to 200 ^oC and $4.2x10^{-3}$ mbar for both thin films and kept constant during the whole depositions.

The electrical characterization was done to compare the main electrical parameters such as ideality factor, barrier height, series resistance and interface states of MIS-1 and MIS-2 SDs. For the electrical characterization, dot shaped two different rectifier front contacts as Au (1500 Å) and Ni/Au (500/1000 Å) with 2 mm diameter were formed on to $1cm^2$ square pieces of samples at 70 ^oC. After the completion of the fabrication of MIS-1 and MIS-2 SDs, the forward bias *I-V* measurements were performed using Keithley 2400 source-meter at room temperature. The whole electrical measurements were also performed using microcomputer through an IEEE-488 AC/DC converter card.

3. Results and discussion

The experimental *I-V* data are analyzed by the well-known equation at forward bias [33].

$$I = I_o \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \qquad (1)$$

where q is the electronic charge, k is the Boltzmann's constant, T is the absolute temperature in Kelvin and I_o is the saturation current which is obtained from the intercept of *ln(I)* vs *V* plot and is expected as

$$I_o = AA^*T^2\exp\left(-\frac{q\Phi_b}{kT}\right) \qquad (2)$$

where A is the effective diode area, A^* is the effective Richardson constant and equals to 112 A cm^{-2} K^{-2} for n-type Si. The ideality factor is calculated from the slop of the linear region of the forward-bias *ln(I)-V* plot and is given by

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \qquad (3)$$

Fig. 1 shows the semi-logarithmic forward bias *I-V* curves of MIS-1 and MIS-2 SDs at room temperature. As can be seen from the Fig. 1, the similar behavior was observed in both cases, i.e., due to the effects of some factors such as series resistance, interface states and interfacial insulator layers the linear region narrows and it deviates from linearity.

The experimental values of Φ_b and n for MIS-1 and MIS-2 SDs were calculated Eq. (2) and Eq. (3) as 0.88 eV and 0.82 eV and 1.80 and 1.92, respectively, and these values given in Table 1. It is clear that the ideality factors of the SDs are very close to unity. In addition, R_s value was determined from the structure resistance (R_i) versus applied bias voltage (V_i) plot obtained from the *I-V* measurements where $R_i = dV_i/dI_i$. The values of R_s for MIS-1 and MIS-2 SDs were found as 108.12 Ω and 50.13 Ω, respectively, and the values given in Table 1.

(1)

Table 1. Electrical parameters of MIS-1 and MIS-2 SDs obtained from I-V measurements, Cheung's function and Norde's function at room temperature.

	I-V measurements			Cheung's functions				Norde's functions	
T (K)	n	Φ_b (eV)	R_s (Ω)	n (dV/dln(I))	R_s (Ω)	Φ_b (eV) (H(I))	R_s (Ω) (H(I))	Φ_b (eV)	R_s (Ω)
MIS1	1.80	0.88	106.12	3.97	486.50	0.43	642.97	0.94	988.70
MIS2	1.97	0.82	50.13	2.89	294.83	0.58	327.01	0.87	411.08

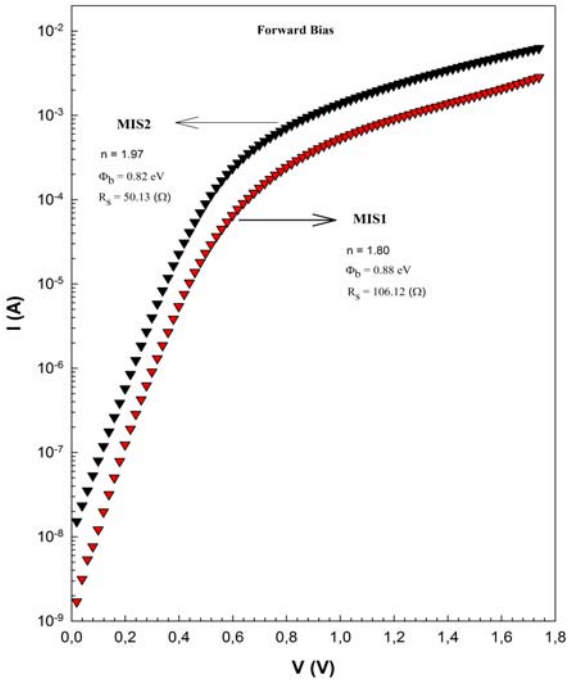

Fig. 1. Forward bias semi-logarithmic I-V measurements of MIS-1 and MIS-2 SDs at room temperature.

The main electrical parameters such as ideality factor, barrier height and series resistance were determined using a method developed by Cheung and Cheung [31]. The Cheung's functions given as

$$\frac{dV}{d(\ln I)} = n\left[\frac{kT}{q}\right] + R_s I \tag{4}$$

$$H(I) = V - n\frac{kT}{q}\ln\left[\frac{I}{AA^{*}T^{2}}\right] = n\Phi_b + \mathrm{R_s I} \tag{5}$$

Here, in Eq. (4) the term IR_s is the voltage drop across the series resistance of the MIS-1 and MIS-2 SDs. The experimental *dV/dlnI* vs *I* and *H(I)* vs *I* plots at room temperature are given in Fig. 2.

In *dV/dlnI-I* plot, the plot's slope gives the R_s value, while the y-axis intercept gives the *n* value. The R_s and *n* values for MIS-1 and MIS-2 SDs were found as 486.50 Ω and 294.83 Ω, and 3.97 and 2.89, respectively. Also, R_s and Φ_b values obtained from *H(I)-I* plot. The R_s and Φ_b values for MIS-1 and MIS-2 SDs were found as 642.97 Ω and 327.01 Ω, and 0,43 eV and 0.58 eV, respectively, and these values given in Table 1.

The R_s values obtained from *dV/dlnI-I* and *H(I)-I* plots were in good agreement with each other. In addition, it is seen that the results regarding R_s of the samples with Ni/Au contact is better than Au contact.

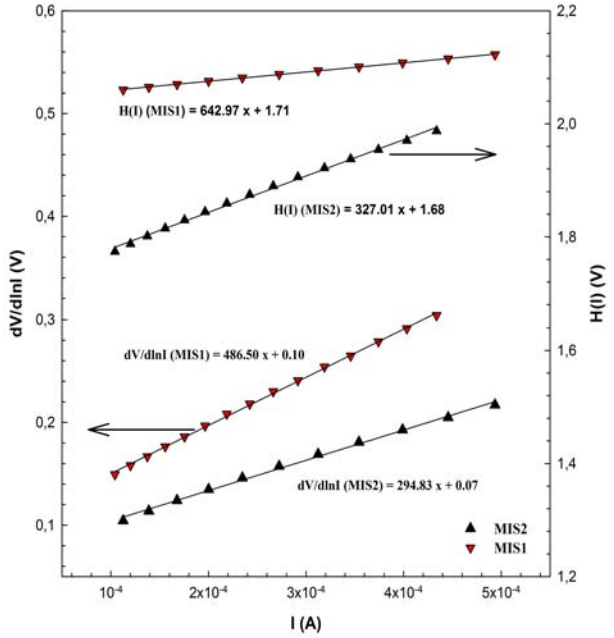

Fig.2. The experimental dV/dlnI vs I and H(I) vs I plots for the MIS-1 and MIS-2 SDs at room temperature.

The values of R_s and Φ_b were obtained from the modified Norde's function developed by Bohlin [34]. While Cheung's functions are only executed for the nonlinear region of the forward bias *I-V* curves, Norde's functions are executed for the whole forward bias region of *I-V* curves of the structure. The modified Norde's function is expressed as

$$F(V,\gamma) = \frac{V}{\gamma} - \frac{q}{kT}\ln\left(\frac{I}{AA^{*}T^{2}}\right) \tag{6}$$

where I is current obtained from the *I-V* curve and γ is a dimensionless value greater than ideality factor. A plot of *F (V)* vs *V* for both samples at room temperature is shown in Fig. 3. From the plot of *F (V)* vs *V,* the value Φ_b and R_s of structure can be determined as follows:

$$\Phi_b = F(V_0) + \frac{V_0}{\gamma} \tag{7}$$

$$R_s = \frac{q}{kT}\left(\frac{kT}{qI}\right)(\gamma - n) \tag{8}$$

where *F(Vo)* is the minimum point of *F(V,γ)* vs *V* and *Vo* is the corresponding bias voltage. The values of Φ_b and R_s obtained from Eqs. (7) and (8) at room temperature. Φ_b and R_s values for MIS-1 and MIS-2 SDs were found as 0.94 eV and 0.87 eV, and 988.70 Ω and 441.08 Ω, respectively, and these values given in Table 1. Similar change of Φ_b and R_s values was observed with the ones obtained from Cheung's function for both samples. Also, it was seen that there is a good agreement between the main electrical parameters values obtained from *I-V* measurements, Cheung's functions and Norde's functions.

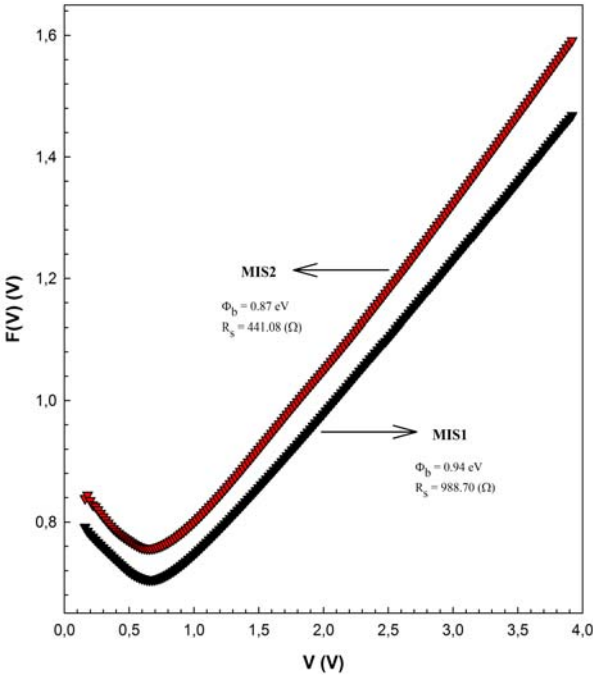

Fig.3. F(V) vs V plot obtained from forward bias I V measurements of the MIS-1 and MIS-2 SDs at room temperature.

Furthermore, voltage dependent ideality factor (n_V), the effective barrier height and density of interface states can be obtained from following equations, respectively [35].

$$n_V = \frac{qV}{kT\ln(I/I_0)} \tag{9}$$

$$\Phi_e = \Phi_b + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \tag{10}$$

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \tag{11}$$

where ε_i and ε_s are permittivity of the interfacial insulator layer and the semiconductor, respectively, δ is the thickness of interfacial insulator layer, W_D is the depletion layer width. Also, in n-type semiconductor, the energy of the surface states E_{ss} with respect to the bottom of the conduction band at the surface of semiconductor is given by

$$E_c - E_{ss} = q(\Phi_e - V) \tag{12}$$

The energy distribution profile of N_{ss} as a function (E_c-E_{ss}) for MIS-1 and MIS-2 SDs were extracted from the forward bias *I-V* measurements by taking the bias dependence of the Φ_e into account and given in Fig. 4. As can be seen from Fig. 4, there is an exponential decrease from bottom of conduction band towards to midgap of Si. In addition, the energy values of the density distribution of N_{ss} has increased exponentially with bias from $2.2\text{x}10^{12}$ $\text{eV}^{-1}\text{cm}^{-2}$ in E_c-0.55 eV to $4.2\text{x}10^{12}$ $\text{eV}^{-1}\text{cm}^{-2}$ in E_c-0.44 eV for MIS-2 SDs and $1.8\text{x}10^{12}$ $\text{eV}^{-1}\text{cm}^{-2}$ in E_c-0.57 eV to $4.2\text{x}10^{12}$ $\text{eV}^{-1}\text{cm}^{-2}$ in E_c-0.46 eV for MIS-1 SDs. The saturation seen in N_{ss} plots is very apparent and this may be due to the presence of series resistance. Thus, this can be ascribed to the interfacial layer deposited on n-type Si surface. Moreover, it is observed that the using of Au as a rectifier contact reduced the density of N_{ss} of structure when compared to that of with Ni/Au rectifier contact.

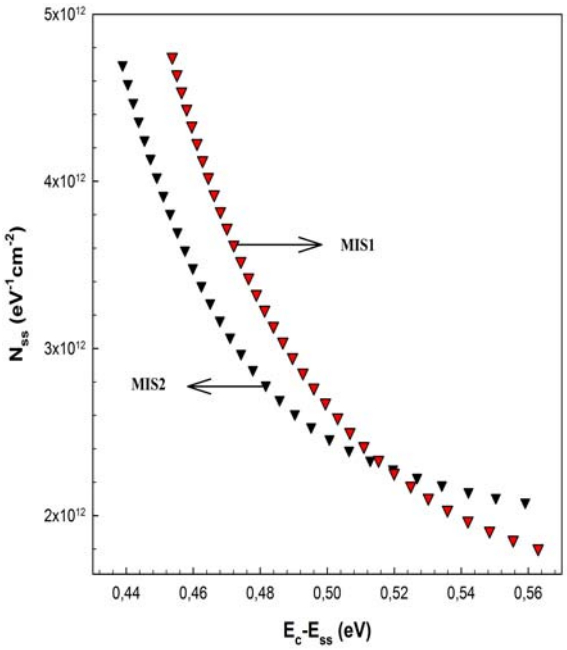

Fig.4. The density of interface states (N_{ss}) as a function E_c-E_{ss} obtained from forward bias I-V measurements of the MIS-1 and MIS-2 SDs at room temperature.

4. Conclusion

In order to investigate the main electrical parameters such as ideality factor, barrier height, series resistance and interface states, we fabricated two types Au/ZnO/TiO_2/n-Si (MIS-1) and (Ni/Au)/ZnO/TiO_2/n-Si (MIS-2) SDs. The electrical properties of MIS-1 and MIS-2 SDs have been analyzed by using the current-voltage measurements at room temperature. The values of n, Φ_b and R_s were calculated as 1.80, 0.88 eV and 106.12 Ω for MIS-1 and 1.97, 0.82 eV and 50.13 Ω for MIS-2 SDs, respectively, from forward-bias *I-V* measurements. The forward bias *I-V* measurements show the downward concave curvature region in the sufficiently high forward bias is due to the effect of R_s. The values of R_s were calculated from high current voltage region of the diodes by using Cheung's functions. The results which were obtained from two Cheung's plots are in good agreement with each other. Also, the values of Φ_b and R_s were obtained by using Norde's functions and these values were compared with the ones calculated from *I-V* measurements and Cheung's functions. In addition, the energy distribution profiles of

N_{ss} for both SDs were obtained from the forward bias *I-V* measurements by taking the bias dependence of the Φ_e into account. There is an exponential decrease from bottom of conduction band towards to midgap of Si. It is observed that the using of Au as a rectifier contact reduced the density of N_{ss} of structure when compared to that of with Ni/Au rectifier contact.

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