Electrical study of alumina properties as a function of the deposition rate and the layers thickness

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In this work, we have analyzed the electrical properties of different layers of alumina deposited on silicon substrate, depending on several experimental parameters. Then, the rate of deposition and the thickness of these dielectric layers are studied. Insulator layer surfaces were characterized by elastic peak electron spectroscopy (E.P.E.S) and X rays photoelectron spectroscopy (X.P.S). These control methods are necessary because the variation of the stoichiometry and of the electronic structure of alumina play an important role in the growth and the stability of the metal overlayers of the MIS structure. Concerning the interface quality, we have observed that a deposition rate equal to 32 nm/h seems to be less convenient than for a smaller one. The great rate deposition induces a number of defects at the insulator /semiconductor interface and in the insulator. The quantities of charges Q_T in the insulator for deposition rates of 1.2 nm/h and 32 nm/h are evaluated to 10^{11}charges per cm^2 and 4.33×10^{12} charges per cm^2, respectively. The values of the interfacial densities of states N_{ss} in the midgap for the structures vary between 9.5×10^{11} $eV^{-1}.cm^{-2}$ and 1.2×10^{13} $eV^{-1}.cm^{-2}$ respectively.

(Received April 17, 2013; accepted June 12, 2013)

Keywords: Alumina - XPS - Electrical measurements - MIS - deposition rate

1. Introduction

The study of phenomena that connect the process of formation and the properties of insulator-semiconductor interface is very important for the realization of MIS structure. Indeed, the performance of the metal-insulator-semiconductor structure depends on the quality of the insulator-semiconductor interface and the insulator layers [1]. As a result, the change of the electronic structure of the sapphire surface is used in the growth and the stability of deposit metal. As well as adherence of a metal on an oxide depends on the electronic structure of the metal and the stoichiometry of the oxide.

In this work, we have studied the deposition of alumina layers on silicon substrate. The deposition is achieved with different rate and different thickness of alumina.

The quality of these layers has been controlled by Elastic Peak Electron Spectroscopy (E.P.E.S) and X-rays Photoelectron Spectroscopy (X.P.S) and by electrical characterization using capacitance-voltage C(V) at high frequency.

2. Experimental procedure

The samples of silicon (100) are p-type wafers at different doping levels (10^{15}-10^{17} $atoms.cm^{-3}$). They were chemically cleaned according to a method based on successive baths of acid, alcohol solution and deionized water[2]. The deposition of alumina was performed in an ultra-high-vacuum (UHV) chamber at a pressure of 10^{-7}–10^{-8} Pa. The chamber was equipped with a RFA analyzer permitting Spectroscopy experiments. Two special deposition sources of alumina were constructed for this study. This deposition operates on the principle of electron bombardment [3]. One cell has a double wall graphite / molybdenum Knudsen crucible (cell n° 1 with v =1.2 nm/h), the other one has a simple graphite crucible (cell n° 2 with v = 32 nm/h). A third kind of alumina films has been made by reactive sputtering:

- the first deposit of alumina has been elaborated with deposition rate equal to 1.2 nm/h during 390 min, the structure is called Al_2O_3/Si-1;
- the second deposit has been done with deposition rate equal to 1.2 nm/h during 390 min but with substrate heated to 300 °C during the condensation, named Al_2O_3/Si-2;
- the structure Al_2O_3/Si-3 is obtained by deposition rate of 32 nm/h during 19 min;
- the last deposit has been done in two stages, the first deposition of alumina has been made with deposition rate of 1.2 nm/h during 475 min. This operation is followed by a deposit of alumina by cathodic pulverization, this structure is called Al_2O_3/Si-4.

The Al_2O_3/Si structures are characterized electrically using a temporary gate contact constituted with a mercury probe (Hg) (gate surface S = 2×10^{-3} cm^2).

The capacitance C as a function of bias voltage V_G plotted at high frequency (1 MHz), is measured with a PAR 129 A two-phase Lock-in amplifier.

3. Results and discussion

The studied samples are analyzed by X ray photoelectron spectroscopy. The Figs. 1, 2, 3 and 4 displays a wide range spectrum for the studied samples. We notice peaks corresponding to the aluminum, oxygen and carbon. The impurities such as fluor and nitrogen are detected at very low dose. The presence of these impurities is due to the chemical cleaning of our samples and by the liberation of the gas of vacuum pump.

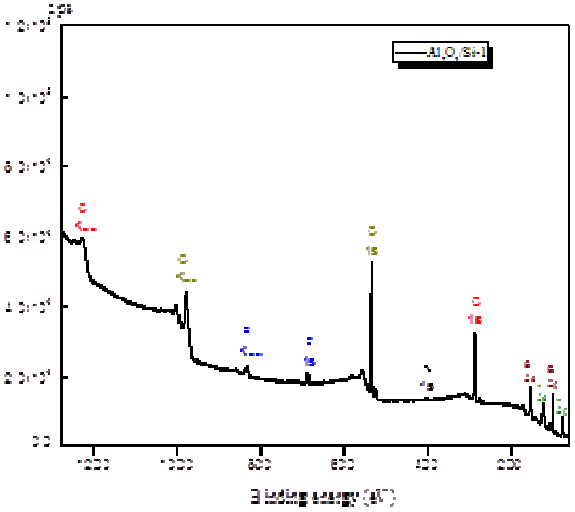

Fig.1. XPS spectrum on an Al_2O_3/Si-1 structure.

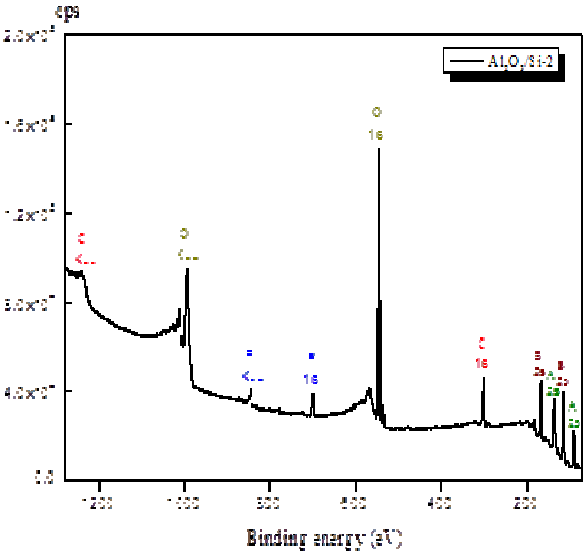

Fig. 2. XPS spectrum on an Al_2O_3/Si-2 structure.

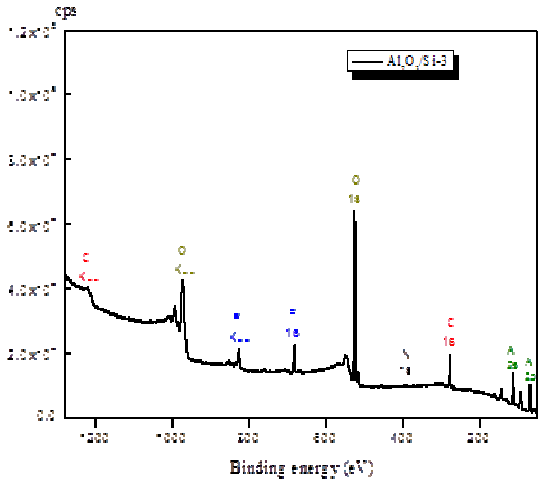

Fig. 3. XPS spectrum on an Al_2O_3/Si-3 structure.

On the other hand, only the sample Al_2O_3/Si-4 shown in Fig. 4 presents an Argon peak. That is easily explain because contrary, at other samples obtained at ultra-high vacuum, this sample has been elaborated by cathodic pulverization in Argon atmosphere.

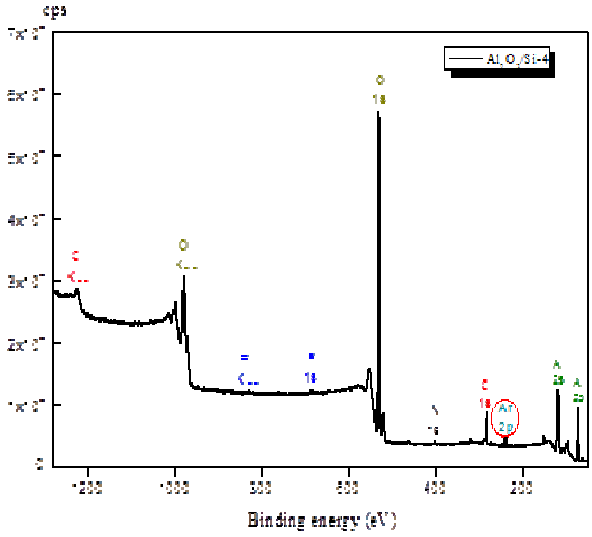

Fig. 4. XPS spectrum on an Al_2O_3/Si-4 structure.

We have analyzed the surface of the samples by elastic peak electron spectroscopy [10].

We compare the value of elastic reflection coefficient for our samples with two reference substrates, aluminum and alumina; we note that the coefficient of the elastic reflection of Al_2O_3 /Si-4 is close to that of pure alumina, prove a best oxidation of the surface, contrary to the other samples [10].

The study of C(V) characteristic at high frequency is an interesting tool for the determination of interface states N_{ss} and the quantity of charges Q_T in the insulator.

The Figs. 5 and 6 show the C(V) characteristics plotted at high frequency and the theoretical curves respectively.

We note that the plot of the theoretical curves is based on the resolution of Poisson equation taking into account the doping N_a concentration the area S of the metallic contact, the thickness of insulators d_i as well as the capacitance C_i of the insulator layer.

We have used C(V) characteristics where the capacitance in the accumulation region is maximum and equal to insulator one. Knowing the dielectric constant of alumina (ε_i = 5 for Al_2O_3 [5]) and gate area S, the thickness of insulator expression is calculated using the following formula [5]:

$$d_i = \frac{\varepsilon_o \varepsilon_i}{C_{acc}} S \qquad (1)$$

The insulator thickness values obtained from C(V) characteristics for the different samples vary between 85 Å and 820 Å (see Table 1).

Table 1.Different parameters obtained for Hg/Al_2O_3/Si structures.

Samples	Hg/Al_2O_3/Si-1	Hg/Al_2O_3/Si-2	Hg/Al_2O_3/Si-3	Hg/Al_2O_3/Si-4
Mode of alumina deposition	Cell n°1	Cell n°1+ heating at 300°C	Cell n°2	Cell n°1+ cathodic pulverization
Deposition rate (nm/h)	1.2	1.2	32	1.2
d_i(Å)	90	110	85	820
V_{FB}(V)	0.2	-2.6	-0.6	0.4
Q_T (charges/cm^2)	1.57×10^{12}	8.42×10^{12}	4.33×10^{12}	10^{11}
N_{ss} (eV^{-1}.cm^{-2})	4.1×10^{12}	3.8×10^{12}	1.2×10^{13}	9.5×10^{11}

For the Al_2O_3/Si-1 and Al_2O_3/Si-4 samples, the form of the experimental curve is close to the theoretical curve. These measurements reflect a very good quality of alumina layers (see Figs. 5 and 6).

We can do some remarks in the case of the Al_2O_3/Si-2 (Fig. 5), the experimental curve is moved, but preserves a good slope, this is due to the presence of charges in the insulator, the quality of the insulator is lower in comparison with other samples [4].

The quantity of charges presents in the interface is given by the relation [6]

$$Q_T = \frac{C_i}{qS}\left(V_{FB} - \phi_{ms}\right) \qquad (2)$$

where ϕ_{ms} is the difference of work functions of metal and semiconductor, and V_{FB} is the flat band voltage measured from the difference between the experimental and the theoretical C(V) curves, without polarization voltage (V_G = 0).

The values of V_{FB} acquired experimentally for different structures, vary between - 2.6 and 0.4V and consequently the quantity of charges is in the range of 10^{11} charges. per cm^2 and 8.4×10^{12} charges. per cm^2 .

The obtained results acquired for different structures are given in the Table 1.

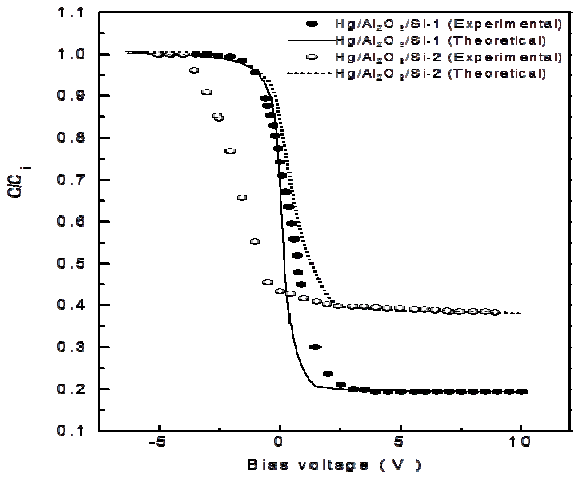

Fig. 5. Experimental and theoretical C(V) curves of Hg/Al_2O_3/Si-1 and Hg/Al_2O_3/Si-2structures.

We note a higher presence of charges in insulator of Al_2O_3/Si-2 structure due to heating of structure during the deposition of alumina. So, we conclude that the heating of the structure during the deposition of alumina not improve the electronic quality of these structures.

One can remark the difference obtained between the samples Al_2O_3/Si-3 and Al_2O_3/Si-1 that permit to underline the interest to use weak rates of deposition.

In the case of the Al_2O_3/Si-3 structure (see Fig. 6), we have observed a more deformation of the experimental C(V) curves compared with classical one. This phenomenon is due to the presence of a higher density of interface state.

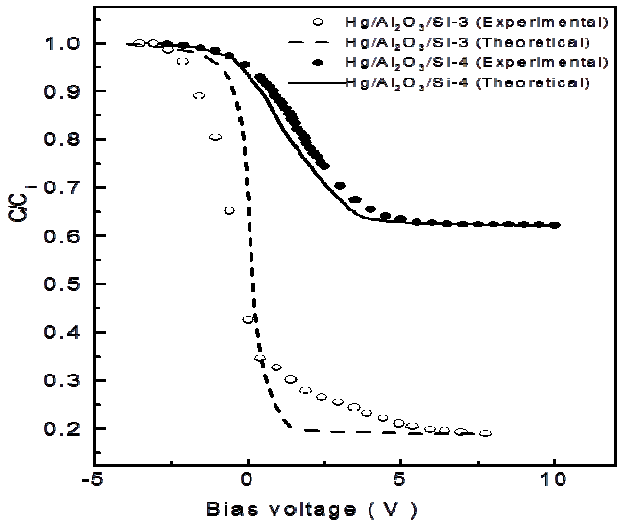

Fig. 6. Experimental and theoretical C(V) curves of $Hg/Al_2O_3/Si$-3 and $Hg/Al_2O_3/Si$-4.

The interface states density N_{ss} has been evaluated by a TERMAN method [6]. This method is based on the comparison at high frequency of the experimental and theoretical C(V) curves obtained for an ideal MIS structure.

The density of interface state at interface is given by [6]:

$$N_{ss} = \frac{C_i}{qS}\frac{d(\Delta V)}{d\psi_s} \qquad (3)$$

ψ_s is the electrostatic potential at the interface.

For plot $N_{ss}(E_{ss}\text{-}E_{vs})$, we have established the correspondence between the surface potential ψ_s and the energy $E_{ss}\text{-}E_{vs}$ using the following relation [7]:

$$E_{ss} - E_{vs} = \frac{E_g}{2} + q(\psi_s - \psi_B) \qquad (4)$$

E_g, E_{vs} are respectively the gap of semiconductor and the energy level in valence band on surface and ψ_B is the potential in the semiconductor bulk.

The Fig. 7 shows the variation of $N_{ss}(E_{ss}\text{-}E_{vs})$ for the four type samples. The density of interface states in the midgap for the different samples varies between 9.5×10^{11} and 1.2×10^{13} $eV^{-1}.cm^{-2}$. The obtained results are comparable with other works described by other authors [8, 9].

The best results are obtained when the alumina is thick that is interesting for the fabrication of the MIS transistors.

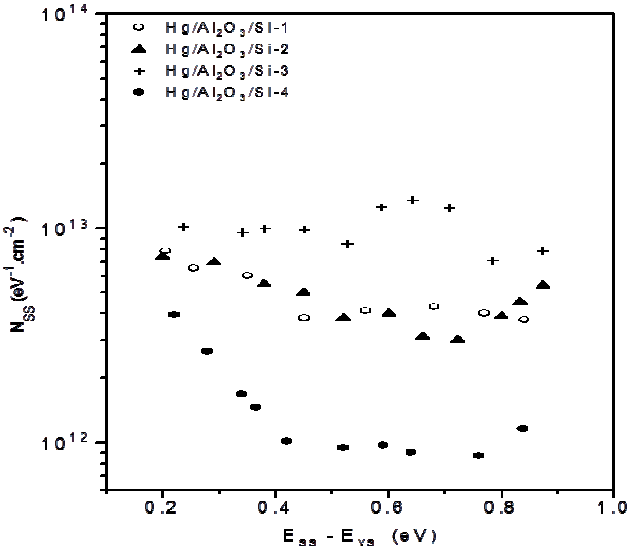

Fig. 7. Distribution of states densities in the band gap of the $Hg/Al_2O_3/Si$ structures.

4. Conclusion

In this work, we have study the electrical properties of different alumina layers made on silicon substrate as function of the deposition rate and the layers thickness.

The elaborated structures were electrically characterized using capacitance voltage C(V) method. The simulation of the theoretical and experimental characteristics allows us to plot the evolution of state density in the bandgap.

It is appeared from the electrical measurements that a heating of the substrate during the alumina deposit destroy the interface and the electrical properties consequently of the structure.

The different studies performed on the Al_2O_3/Si-1 and Al_2O_3/Si-4 samples show that a thick films of alumina improves the electrical parameters of the structure such as the interface states densities and the quantity of charges in insulator. Concerning the quality of alumina, the electrical measurements confirm the presence of few charges in the insulator and at the interface insulator/ semiconductor notably for the Al_2O_3/Si-1 and Al_2O_3/Si-4 samples. In fact the XPS spectrums don't show any contamination in the volume.

In the case of Al_2O_3/Si-1 and Al_2O_3/Si-4 structures, we have noted a strong similarity between the theory and the experiment (nearly identical slope) and a weak shift corresponding to a flat band voltage V_{FB} = 0.4 V and 0.2 V respectively, these data confirm the improvement of the metal/insulator interface.

Indeed, a deposition operated at a rate of 32 nm/h seems to be more harmful for the quality of the interface than a lower rate of deposition. It induces a great number of defects at the insulator /semiconductor interface and in the insulator.

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