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Extraction of the series resistance and interface states in Au/n-Si(111) Schottky barrier diodes (SBDs) with native insulator layer using *I-V-T* and C-V-T measurement methods

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The effect of interface state (N_{ss}) and series resistance (R_s) on the current-voltage (I-V) and capacitance-voltage (C-V) characteristics of Au/n-Si (111) (MIS) Schottky barrier diodes (SBDs) were carried out at 80, 200, 320 and 400 K. The energy distribution profile of N_{ss} was extracted from the forward bias I-V measurements by taking into account the bias dependence of the effective barrier height (Φ_e) for each temperature. Experimental results show that the value of barrier height (Φ_{Bo}) decreases and ideality factor (n) increases with a decrease in temperature. The values of barrier height and N_{ss} are also obtained from I-V and C^{-2}-V characteristics and these two different methods are compared. The high value of n was attributed to the presence of a native insulator layer at metal/semiconductor (M/S) interface and the high value of N_{ss} localized at Si/SiO_2 interface, changing from the ~1x1014$cm^{-2}eV^{-1}$ (at 80 K) to ~5x1013 $cm^{-2}eV^{-1}$(at 400 K).

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1. Introduction

It is well known, the presence of an interfacial insulator layer such as SiO_2, SnO_2, TiO_2 and Si_3N_4, native or deposited, transforms the metal-semiconductor (MS) SBDs into a metal-insulator-semiconductor (MIS) type SBD and its I-V characteristics are considerably deviate from those expected for an ideal SBDs. Also, the particular distribution of interface states (N_{ss}) [1-6], series resistance of device [5,7-11], device temperature [3,6-10] and barrier formation at M/S interface [10-15] are important parameters and they cause deviation from the ideal SBDs. In general, the forward bias I-V plots are linear in the semilogarithmic scale at low voltages ($3kT/q \leq V \leq 0,7V$) but deviate considerably from linearity due to the effect of R_s when the applied bias voltage is sufficiently large ($V \geq 0.7V$) [1,5,12,11-17].

On the other hand, the N_{ss} is effective in both the linear and non-linear regions of these characteristics [1,18]. Therefore, to determine the main electrical parameters such as the reverse saturation current (I_o), n and Φ_{Bo} of these devices, difficulties will arise due to the existence of interfacial insulator layer, N_{ss} and R_s. For instance, when the values of R_s is enough large, the linear part of Ln(I)-V plots will be too small to get a reliable value of BH and ideality factor. There are several suggested methods [23-29] to the determination of the R_s, but they suffer from a limitation of their applicability, in this field, to practical devices with an interfacial insulator layer [30-32]. For example, although the procedure proposed by Cheung et al. [29] requires only one forward bias I-V curve and eliminates the task of determining the minimum of the Norde' s [24] function, it does not give the expected value of R_s of the neutral region as was also indicated by them [29,30].

In addition, the presence of interfacial insulator layer and its thickness, R_s and N_{ss} can affect the *C-V* characteristics of MIS type SBDs, causing a bending of the $1/C^2$-*V* as well as increasing the ideality factor. In general, a *C-V* plot shows an increase in capacitance with an increase in forward bias. However, in recent years, an anomalous peak in forward *C-V* characteristics attributed interface states and series resistance has been reported [19-21]. Ashok [18] derived an expression for the dependence of the *n* on the interface parameter and applied voltage. $1/C^2$ vs *V* plots into linear ones were given by Vasudev et al.[22], where a quantity called "excess capacitance" C_o, which causes a non linearity in the reverse bias region, was introduced.

In this study, we investigate the effects of the R_s and N_{ss}, causing non-ideal behavior I-V and C-V characteristics of Au/n-Si (111) SBD with native insulator layer at 80, 200, 320 and 400 K. Temperature dependence of Φ_{Bo}, R_s and N_{ss} values were obtained by using the standard [1,2], Bohlin [26] and Cheung's [29] methods from the forward bias I-V measurements and Nicollian [23] method from both reverse and forward bias C-V measurements, and the results of these methods were compared. The non-ideal I-V and C-V behavior observed in Au/n-Si (111) SBD were attributed to the presence of R_s of device, a native insulator layer (SiO_2) at M/S interface and a particular distribution of N_{ss} at Si/SiO_2 interface.

2. Experimental procedure

The Au-/n-Si(111) SBDs were fabricated on 2 inch (5.08 cm) diameter n-type (P doped) epilayer silicon wafer

with (111) surface orientation, 0.7 Ω-cm resistivity and 350μm thickness. For the fabrication a process, Si wafer was decreased in organic solvent of $CHClCCl_2$, CH_3COCH, and CH_3OH consecutively and then etched in a sequence of H_2SO_4 and H_2O, %20 HF, a solution of $6HNO_3$:1HF:$35H_2O$, %20 HF and finally quenched in deionized water for a prolonged time. Preceding each cleaning step, the wafer was rinsed thoroughly in deionized water of resistivity of 18 MΩ-cm. After this cleaning process, high purity (99.999 %) Au with a thickness of about 1500 Å were thermally evaporated onto whole back side of Si wafer at a pressure about 10^{-6} Torr in high vacuum system. In order to perform a low resistivity ohmic backcontact, Si wafer was sintered at 500 ^{o}C for 3 min in N_2 atmosphere. After that ~1500 Å thick high purity Au (%99,999) dots of 1 mm diameter were evaporated onto front of Si wafer at in high vacuum system and at same pressure. In this way, the fabrication process of Au-/n-Si (111) SBDs was completed. The native interfacial insulator layer thickness was estimated to be about 30 Å from high frequency (1 MHz) measurement of the oxide capacitance in the strong accumulation region. The *I-V* and *C-V* measurements were performed by the use of a Keithley 2400 sourcemeter an HP 4192 A LF impedance analyser (5 Hz-13 MHz). Small sinusoidal signal of 40 mV peak to peak from the external pulse generator is applied to the sample in order to meet the requirement [23]. All measurements were carried out with the help of a microcomputer through an IEEE-488 AC/DC converter card. The temperature control were carried out using a temperature-controlled Janes vpf-475 cryostat with a Lake Shore model 321 auto-tuning temperature controllers in a vacuum of $5x10^{-4}$ Torr which enables us to make measurements in the temperature range of 77-450 K.

3. Results and discussion

3.1. The forward bias current-voltage-temperature (I-V-T) characteristics

When a MS Schottky barrier diode with a R_s is considered, based on the TE mechanism, it is assumed that the relation between the applied forward bias voltage (V≥3kT/q) and the current, I, can be expressed as [1]

$$I = I_o \exp\left(\frac{q(V - IR_s)}{nkT}\right)\left[1 - \exp\left(\frac{-q(V - IR_s)}{nkT}\right)\right] \quad (1)$$

where the term of IR_s is voltage drop across the R_s of the diode and I_o is the reverse saturation current and it can be derived from the straight-line intercept of the current axis (lnI) at zero bias and is given by

$$I_o = AA^*T^2 \exp(-q\Phi_{Bo}/kT) \quad (2)$$

where, the quantities A, A^*, q, k, T and Φ_{Bo} are the rectifier contact area, the effective Richardson constant and equals to 120 A/cm^{2}K^2 for *n*-type Si [1], the electronic charge, the Boltzmann constant, temperature in K and the zero-bias barrier height, respectively. Fig.1. shows the experimental semi-logarithmic forward and reverse-bias ln(I)-V characteristics of Au/n-Si (111) SBD at 80, 200, 320 and 400 K. It is clear that the forward bias semi-logarithmic ln(I)-V characteristics of the Au/n-Si (111) SBD show a good rectifying behavior. Moreover, the "soft" or slightly non-saturating behavior was observed as a function of bias in the reverse bias branch especially at low temperatures, which may be explained in terms of the image force lowering of SBH [33-35] and the presence of the interfacial layer between the metal and n-Si (111) wafer [17]. Using the values of Io, the values of Φ_{Bo} were calculated from Eq. (2) for each temperature. The values of ideality factor were obtained from the slope of the linear region of the forward bias lnI-V plots for each temperature using the Eq. (1)

$$n = \frac{q}{kT}\frac{dV}{d(L\,n\,I)} \quad (3a)$$

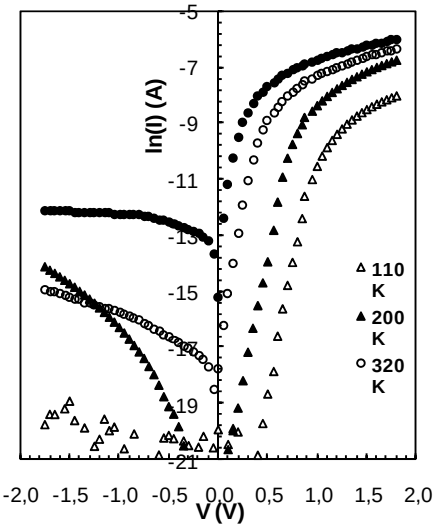

Fig. 1. The forward and reverse bias ln(I)-V characteristic of the Au-/n-Si(111) SBDs with native insulator layer at four different temperatures.

To obtain the interface states (N_{ss}) energy distribution from the forward bias I-V data, the bias dependence of ideality factor n(V) and barrier height are necessary. Furthermore, the bias dependent n(V) can be written from Eq. (1) as

$$n(V) = \frac{qV}{kTLn(\frac{I}{I_o})} \quad (3b)$$

The some main electrical parameters obtained from the forward bias ln(*I*)-*V* characteristic of the Au-/n-Si(111) SBDs at various temperatures are given in Table 1.

As shown in Table 1, the value of Φ_{Bo} and n obtained from the ln(I) vs V plots were found to be a strong function of temperature. The value of n was found to increase while the value of Φ_{Bo} decrease with decreasing temperature (n=5.83 and Φ_{Bo}=0.40 eV at 110 K, n=1.60 and Φ_{Bo}=0.89 eV at 400 K). The high values of n especially at low temperatures are probably due to the

potential drop on the interfacial insulator layer, the presence of excess current at low temperature region, barrier inhomogeneity and a particular distribution of N_{ss} at M/S interface [13-17].

Table 1. Direct determination of R_s, R_{sh}, n, and Φ_B by using the standard and modified Norde method developed by Bolin at four different temperatures for the Au/n-Si (111) SBD.

T (K)	I_o (A)	n	Φ_{Bo} (eV)	V_o (V)	I (A)	F(Vo) (V)	Φ_B (eV)	R_s (Ω)	R_{sh} (Ω)
110	2.54×10^{-13}	5.09	0.40	1.148	6.78×10^{-5}	0.231	0.260	1805	3.7×10^{9}
200	1.55×10^{-10}	3.28	0.60	1.148	3.59×10^{-4}	0.390	0.421	787	2.4×10^{8}
320	5.76×10^{-13}	1.89	0.81	0,869	5.59×10^{-4}	0.616	0.643	621	5.5×10^{5}
400	4.12×10^{-6}	1.60	0.89	0,399	7.30×10^{-4}	0.787	0.802	265	1.3×10^{4}

As can be seen from Fig. 1, the ln(I) vs V plots clearly depict the linear behavior (at the intermediate bias voltages) over a several orders of current and shift towards the high bias side with decreasing in temperature, but deviate considerably from linearity due to the effect of series resistance of the device at efficiently high bias voltages.

Thus, the value of R_s and Φ_{Bo} were obtained from the modified Norde method developed by Bohlin [26]. However, Bohlin only used two different values of arbitrary parameters of γ and thus two experimental data points.

Here, we used the Bohlin method for each temperature as

$$F(V, \gamma) = V/\gamma - kT/q \; Ln\,(I/(AA^*T^2)) \quad (4)$$

where γ is the dimensionless and greater than ideality factor. According this method, once the minimum of the F(V, γ) vs. V plot is determined, the value of BH and R_s can be obtained from Eq.(5) and (6), respectively, as

$$\Phi_B = F(V_0) + V_0/\gamma - kT/q \quad (5)$$

$$R_s = (kT/qI)(\gamma - n) \quad (6)$$

where $F(V_0)$ is the minimum point of F(V, γ) vs V plot, V_o and I are the corresponding bias voltage and current, respectively. Fig. 2 (a) shows the F(V) vs V plots for the Au-/n-Si(111) SBDs with native insulator layer at four different temperatures. The values of Φ_B and R_s obtained from equations (5) and (6), respectively, at four different temperatures are given in Table 1 together with standard method. As shown in Table 1, the value of Φ_B and R_s obtained from the F(V, γ) vs V plots were found to be a strong function of temperature. The value of Φ_B was found to increase, while the value of R_s increase with decreasing temperature (Φ_B =0.213 eV and R_s=2501 Ω at 80 K, and Φ_B =0.802 eV and R_s=265 at 400 K). It is clear that the value of R_s is quite high for all temperatures. Therefore, before any analysis could be done, all the measurements (I-V, C-V and G/w-V) must be corrected for R_s [23-29].

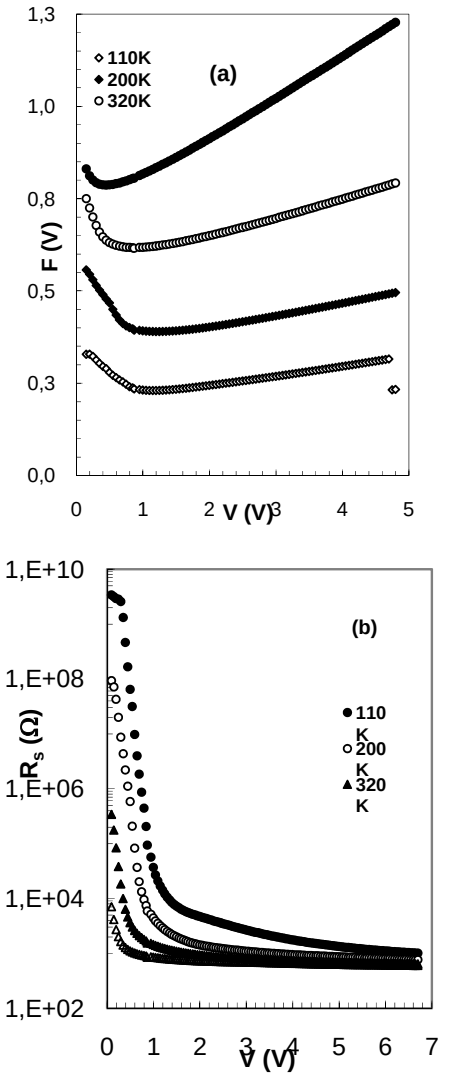

Fig. 2. The F(V) vs V and R_s vs V plots of the Au-/n-Si(111) SBDs with native insulator layer at four temperatures, respectively.

In addition, the bias voltage dependent series resistance profile of the Au-/n-Si(111) SBDs with native insulator layer was obtained from the I-V data as $\delta V/\delta I$ and are given in Fig. 2 (b). As can be shown in Fig. 2 (b), at sufficiently high forward bias region (V≥4 V) the value of series resistance is almost independent of bias voltage. At zero-bias, the value of resistance which is equal to the diode shunt resistance (R_{sh}) decreases rapidly with increasing temperature. It is clear that both the value of R_s and R_{sh} were found strongly temperature dependent and decrease with increasing temperature. Such behavior of R_s and R_{sh} can be explained by the enhanced conductivity of the Si and this is expected behavior. On the other hand, the values of R_{sh} were remains relatively high even at sufficiently high temperatures (320 and 400 K), thus, its effect on the I-V characteristics can be neglected.

3.2. The density distribution of the interface states profile obtained from the forward bias I-V-T characteristics

The non-linearity of the forward bias Ln*I-V* characteristic especially at high bias values indicated a continuum of N_{ss}, which equilibrates with semiconductor [36]. For SBDs with native or deposited interfacial insulator layer, the relation between the density of the interface states (N_{ss}) in equilibrium with the semiconductor and the value of the ideality factor greater than unity can be expressed as [3].

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \tag{7}$$

where δ is the thickness of interfacial insulator layer, W_D is the width of the depletion layer calculated from C^{-2} vs V characteristics at 1 MHz. The energy density distribution of N_{ss} for the Au/n-Si (111) SBD with native insulator layer can be obtained from the forward bias I-V data by taking into account the bias dependence of the n(V) and effective BH (Φ_e). The effective barrier height Φ_e is given as

$$\Phi_e = \Phi_{bo} + \beta(V) = \Phi_{bo} + (1 - \frac{1}{n(V)})V \tag{8}$$

by considering the applied voltage dependence of the BH, where β is the voltage coefficient of the effective barrier height Φ_e used in place of the barrier height Φ_B and it is a parameter that combines the effects of both interface states in equilibrium with the semiconductor [6,10,37]. Thus, the energy profile of N_{ss} in equilibrium with semiconductor was obtained by substituting the voltage dependent *n(V)* values and ε_s=11.8ε_o, εi=3.8ε_o, δ=30Å in Eq. 9 for each temperature and is given in Fig. 3.

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\delta}{\varepsilon_i}\left(n(V) - 1\right) - \frac{\varepsilon_s}{W_D}\right] \tag{9}$$

where ε_i and ε_s are the permittivity of the insulator layer and the semiconductor, respectively.

The interfacial insulator layer (S_iO_2) thickness δ was obtained from high frequency (1 MHz) C-V measurements. Furthermore, in *n*-type semiconductors, the energy of the N_{ss} with respect to the bottom of the conductance band (E_c-E_{ss}) at the surface of semiconductor is given by

$$E_c - E_{ss} = q(\Phi_e - V) \tag{10}$$

Fig. 3 shows the energy distribution profile of N_{ss} as function of E_c-E_{ss} using Eq.10 at 110, 200, 320 and 400 K. As can be seen in Fig. 3, it is very apparent that there is an exponential increase of the N_{ss} towards to bottom of the conductance band for each temperature, and it shifts towards the conductance band (E_c) in the N_{ss} plots due to the effect of temperature and interfacial insulator layer at different temperatures. The value of N_{ss} decreases with increasing temperature due to molecular restructuring and reordering of the M/S interface under the temperature effect. The mean value of the N_{ss} changes from the order of ~1x1014cm^{-2}eV^{-1} (at low temperatures) to ~5x1013 cm^{-2}eV^{-1}(at high temperatures). Similar results have been reported in the literature [38-42].

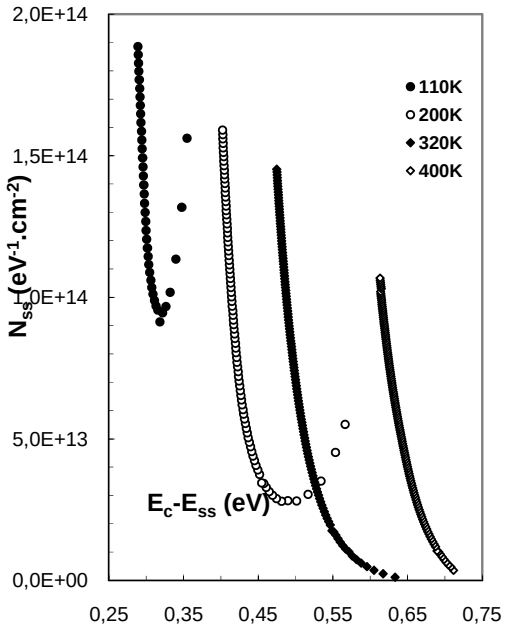

Fig. 3. The energy distribution profile of N_{ss} obtained from the forward bias I-V characteristics of the Au/n-Si SBD with the native SiO_2 layer at different temperatures.

3.3. The capacitance/conductance-voltage-temperature (C/G-V-T) characteristics

The plots of the measured capacitance C_m (V, T) and conductance G_m/ω (V, T) are shown in Fig. 4 (a) and (b),

respectively. As it can be seen in Fig. 4 in the negative bias region the values of C and G/ω increase with increasing both temperature and bias voltage. However, in the forward bias region, C-V and G/ω-V plots show an intersection behavior due to the effect of R_s. Also, Fig. 4 (a) and (b) show an interesting feature at the forward bias C-V and G/w-V plots, which are the common two intersection points at certain bias voltage, and at these points both the value of C and G/w are temperature independent.

The C^{-2} vs V characteristics were illustrated in Fig. 5. As can be seen in Fig. 5, The C^{-2} vs V curves are linear for each temperature in the wide range of bias voltage. The values of Fermi energy (E_F), donor doping concentration (N_D), depletion layer width (W_D) and barrier height (Φ_B(C-V)) were calculated at 110, 200, 320 and 400 K from the Fig. 5, using the following relations [1,2].

$$V_o = V_D - \frac{kT}{q} \tag{11}$$

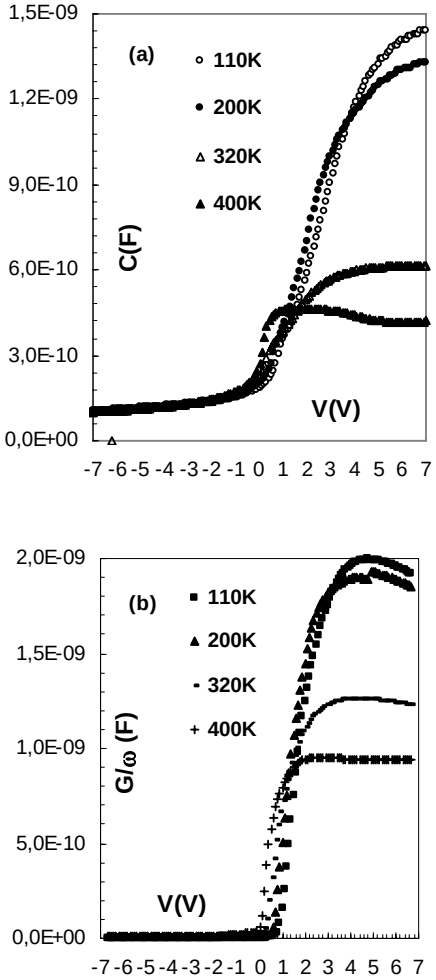

Fig. 4. The voltage-dependent plots of the C-V and G/ω-V characteristic for the Au/n-Si (111) Schottky diode at the four different temperatures.

$$\Phi_B(C-V) = V_o + \frac{kT}{q} + E_F \tag{12}$$

where V_D is diffusion potential, Vo is the intercept voltage and E_F is the Fermi energy level and was obtained from

$$E_F = \frac{kT}{q} Ln(\frac{N_C}{N_D}) \tag{13}$$

with

$$N_C = 4.82x10^{15} T^{3/2} (\frac{m_e^*}{m_o})^{3/2} \tag{14}$$

where N_V is the effective density of states in the Si valance band, m_e*=0.98mo is the effective mass of electrons [1] and m_o is the rest mass of the electron. When C-V measurements were carried out at sufficiently high frequency, the carrier life time τ becomes larger than 1/2πf and in this case the interface states can almost not follow the applied signal [1,23]. The some main electrical parameters such as E_F, N_D, W_D and Φ_B(C-V) obtained from reverse bias C^{-2} vs V plot at four different temperatures are given in Table 2.

The relationship of the theoretical carrier doping density N_A=4.31x10^{16} cm^{-3} and the experimental carrier doping density N_A is known to be c_2= N_A/ N_A [14]. The density of interface states D_{it} was calculated at different temperatures by using

$$c_2 = 1/1+\alpha \tag{15}$$

where $\alpha = q\delta N_{ss}/\varepsilon_i$ [38,39]. The mean density of interface states N_{ss} was calculated at different temperatures from Eq.(15). As shown in Table 2, the obtained Φ_B(C-V) and N_{ss}(C-V) values decrease with increasing temperature and are in close agreement with Φ_B(C-V) and N_{ss}(C-V) calculated from I-V characteristics.

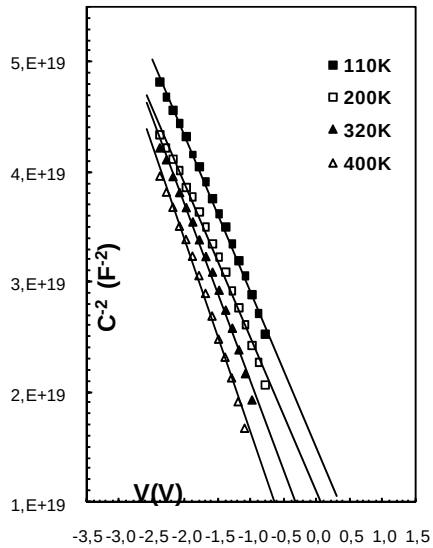

Fig. 5. The C^{-2}-V characteristic for the Au/n-Si (111) Schottky diode at the four different temperatures.

Table 2. Temperature dependent values of parameters determined from the reverse bias C-V characteristics of the studied Au/n-Si (111) SBD.

T (K)	V_D (eV)	N_D (cm^{-3})	N_C	E_F (eV)	W_D (cm)	Φ_B(C-V) (eV)	c_2	N_{ss} ($eV^{-1}cm^{-2}$)
110	1.01	$9.34x10^{14}$	$3.46x10^{18}$	0.057	$3.45x10^{-5}$	1.049	0.217	$2.53x10^{13}$
200	0.85	$1.12x10^{15}$	$1.37x10^{19}$	0.162	$2.89x10^{-5}$	0.995	0.261	$1.99x10^{13}$
320	0.66	$1.54x10^{15}$	$2.77x10^{19}$	0.270	$2.18x10^{-5}$	0.913	0.357	$1.26x10^{13}$
400	0.53	$1.96x10^{15}$	$3.87x10^{19}$	0.341	$1.74x10^{-5}$	0.861	0.454	$8.42x10^{12}$

4. Conclusions

In order to analysis the interface states (N_{ss}) and series resistance (R_s) effect on the conduction mechanism of Au/n-Si (111) (MIS) SBDs, I-V, C-V and G/ω-V characteristics were investigated at 110, 200, 320 and 400 K. The energy density distribution profile of the N_{ss} was extracted from the forward bias I-V measurements by taking into account the bias dependence of the n(V) and Φ_e for each temperature. The values of Φ_{Bo} (I-V), n and R_s were estimated from both standard and Norde function modified by Bohlin. They were found strongly temperature dependent. It was observed that the values of Φ_{Bo} decreases and the n increases with a decrease in temperature. The values of N_D, barrier height (Φ_B (C-V)) and N_{ss} are also obtained from the current-voltage and C^{-2}-V characteristics and compared. The high values of n were attributed to the presence of an interfacial native insulator layer at M/S interface and the high density of N_{ss} localized at Si/SiO_2 interface. It is clear that the temperature dependent I-V characteristics of SBDs are affected by not only N_{ss} and interfacial insulator layer but also in R_s, and these three parameters have a significant influence on electrical characteristics of SBDs.

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