# High performance all optical AND gate using 2D photonic crystals

K. RAMA PRABHA*, S. ROBINSON
*Department of Electronics and Communication Engineering, Mount Zion College of Engineering and Technology, Pudukkottai, Tamil Nadu, India*

Logic gates are essential components that execute Boolean functions by performing logical operations on binary inputs to produce a single binary output. This paper evaluates the performance of an all-optical AND gate designed using two-dimensional photonic crystals. The design is based on a triangular lattice of dielectric rods with specially designed line and point defects to perform the AND logic operation. It operates at a wavelength of 1550 nm and uses the unique ability of photonic crystals to control light for fast and efficient performance. The functionality and performance of the AND gate are studied using simulations with the Finite Difference Time Domain (FDTD) and Plane Wave Expansion (PWE) methods. The proposed two-input and three-input AND gates achieve contrast ratios of 7.435 dB and 10.71 dB, response times of 0.24 ps and 0.56 ps, and bit rates of 4.16 Tbps and 1.78 Tbps, respectively. The compact design makes it ideal for use in optical computing and communication systems.

(Received April 9, 2025; accepted December 4, 2025)

*Keywords:* AND gate, Photonic crystal, Band gap, Finite difference time domain, Plane wave expansion, Optical computing

## 1. Introduction

Optical communication has revolutionized the way information is transmitted over long distances, offering significant advantages over traditional electronic communication systems, including higher bandwidth, faster data rates, and immunity to electromagnetic interference. The use of light as a carrier of information in optical fibres has enabled the development of global communication networks with unprecedented speed and efficiency [1]. As the demand for faster and more reliable communication systems grows, the need for advanced optical devices capable of manipulating light at the nanoscale has become more critical. Optical communication systems require the integration of devices like modulators, switches, and logic gates that can perform complex operations in the optical domain to enable faster and more efficient processing of data [2].

Logic gates are the building blocks of digital electronics, executing Boolean operations on binary inputs to produce corresponding outputs. Traditionally implemented using electronic components like transistors, diodes, and relays, logic gates are essential for performing computations and processing information in digital systems [3]. In the realm of optical communication, logic gates are being reimagined using photonic technologies to handle information in the form of light rather than electrical signals. The development of all-optical logic gates allows for faster, more energy-efficient processing, making them suitable for photonic integrated circuits (PICs). These circuits, which integrate various photonic components such as light sources, modulators, and detectors on a single chip, offer the potential for high-speed data processing and complex computational operations. The use of all-optical logic gates in PICs can significantly enhance the performance of optical communication systems, especially in applications such as signal processing, routing, and encryption [4].

Photonic crystals (PCs) are advanced optical materials that can manipulate light in unique ways, exploiting periodic structures to control the flow of photons. These structures typically consist of a periodic arrangement of dielectric materials that can create band gaps for light, like how semiconductors control the flow of electrons. One of the key mechanisms used in photonic crystals is the creation of line and point defects within the lattice structure [5]. Line defects can be used to guide light along a specific path, while point defects can localize light at points, enabling the design of photonic devices like waveguides, resonators, and logic gates. By carefully engineering the position and nature of these defects, it is possible to design devices with specific optical properties, such as the ability to perform logical operations like AND, OR, and NOT in the optical domain. The manipulation of light through these defects in photonic crystals has opened new possibilities for creating compact, high-performance optical circuits that can operate at the speed of light and enable the next generation of optical communication systems and photonic computing technologies [6].

There are several optical devices are reported using PCs such as sensors [7,8], power splitters [9], multiplexer [10], demultiplexer [11,12], encoder [13-19], decoder [20], directional coupler [21], add drop filter [22], channel drop filter [23], adder [24] optical switches [25], logic gates [26,27]. They are implemented using transistors, diodes, and relays, among other technologies. Logic gates are staples of modern technology, appearing in everything from basic electronic devices to complex computing systems as basic components of digital electronics.

An all-optical AND gate is a device that performs the logical AND operation using light signals instead of electrical ones. In a traditional electronic AND gate, the output is high (1) only when both input signals are high (1). If either input is low (0), the output will be low (0). The operation of an optical AND gate relies on manipulating light in a way that replicates the behaviour of a traditional AND gate; however, instead of electrical currents, the device uses light waves, typically in the infrared or visible range. [28]. The AND gate is a basic logic gate that outputs a high signal (1) only when both of its inputs are high (1). In all other cases, the output will be low (0). This logical behaviour can be replicated in the optical domain by using a 2D photonic crystal structure with appropriately defects. When light enters the structure, it is guided along paths created by the photonic crystal's lattice and defects. The interaction of light at these points determines whether the "output" light can propagate through or is blocked, simulating the logical AND operation. The output will only be a high signal (allowing light to pass through) when both input channels are active (i.e., both inputs have high light intensity) [29].

In a two-dimensional photonic crystal, such as a square lattice or hexagonal arrangement, the structure can be designed to allow light to flow through specific pathways only under certain conditions, which can be controlled by the presence of line and point defects [30,31]. These defects create localized states or channels where light can be manipulated in a desired manner. For the AND gate, the design ensures that light from both input channels must interact at the correct locations and intensities to produce the desired output [32-34].

The nonlinear Kerr effect and a ring resonator inside a two-dimensional photonic crystal are used in this study to propose an all-optical simultaneous OR and AND logic gate. The structure uses 1 kW $\mu m^{-2}$ of power and runs at a resonant wavelength of 1551.3 nm. The finite-difference time-domain method is used to examine the performance of the reported AND gate. All-optical AND gate with three inputs, utilizing a silicon-air medium in a 2D photonic crystal with a T-shaped waveguide. Its performance is examined at a wavelength of 1.55 μm using the finite-difference time-domain (FDTD) approach [35].

All optical AND gate is designed by using the line, point defect, and ring resonator-based structure. The defects were created inside the waveguide by introducing the mechanisms such as self-collimation, Mach-Zehnder Interferometer, multimode interference, and constructive and destructive interference effects. The various functional parameters were estimated and investigated such as contrast ratio, bit rate, response time, cross talk, insertion loss, and steady state time [36].

Priyanka Kumari Gupta et.al investigated a all optical OR and AND gate, the design offers high contrast ratios (26.10 dB for OR and 25.34 dB for AND), ultra-fast response times (2 ps and 0.67 ps), and bit rates of 0.5 Tbps and 1.5 Tbps [37]. Maddala Rachana et al. proposed a three input AND gate using the photonic crystal fiber with the insertion loss of 1.52 dB [38]. Dongxing Meng et al. designed an all optical OR and AND gate achieves an extinction ratio of 8 dB with a response time of 2.42 ps, while the OR gate outputs a value of 0.72 with a response time of 2.41 ps [39]. Mohammad Derakhshan et al. proposed a ultra compact AND, OR logic gate with I shaped defect. The functional parameters such as contrast ratio 6.1 dB and response time 0.5 ps [40]. Jayson K. Jayabharathan et al. designed a Performance Evaluation of Two-Dimensional Photonic Crystal-Based All-Optical AND/OR Logic Gates. The functional parameters contrast ratio, bit rate and delay time. The footprint of the structure calculated as 12.6 μm×11 μm [41]. F. Parandin et al. reported a E shaped NOR and AND gate. Bit rate achieved as 1.54 Tbits/s [42-50].

Fariborz Parandin et al. review recent advancements in all-optical half-subtractors and full-subtractors using photonic crystals (PhCs). The paper highlights key structural parameters such as dielectric rod arrangement, rod radius, lattice constant, resonator type, and compact size suitable for photonic chip integration. It emphasizes the importance of optical power difference between logic states to achieve high contrast ratios and reduce detection errors. Performance analysis shows low delay, rise, and fall times for linear structures and high contrast ratios for nonlinear designs, with reported delay times of 0.06–0.85 ps and contrast ratios up to 25.88. Overall, the study demonstrates that PhC-based optical subtractors provide high-speed, compact, and efficient solutions for integrated photonic logic circuits [51].

S. S. Zamanian-Dehkordi et al. proposed an all-optical RS flip-flop using the nonlinear Kerr effect in photonic crystals. The design includes a core section with two cross-connected resonant cavities at 1586 nm and 1620 nm, where the resonance of one cavity blocks signal coupling through the other. Optical switch sections with a bias port maintain the previous state when inputs are inactive. The structure achieves a compact footprint of 361 $\mu m^2$ and operates at a maximum frequency of 320 GHz, enabling ultra-fast optical memory applications [52]. Jing Chen et al. investigated an all-optical analog-to-digital converter (ADC) using cascaded optical limiters based on nonlinear photonic crystal ring resonators. A single optical limiter is designed using two nonlinear ring resonators, and cascading four limiters enables a 5-bit ADC. The design is validated with two examples demonstrating correct operation. The proposed structure has a total footprint of approximately 1796 $\mu m^2$, making it suitable for compact all-optical data processing applications [53].

Massoudi Radhouene et al. investigated a Rounded Square Ring Resonator (RSRR) based Add-Drop Filter (ADF) using Two-Dimensional Photonic Crystals (2D PhCs) for Dense Wavelength Division Multiplexing (DWDM) applications. The design enhances the quality factor and bandwidth efficiency compared to existing Coarse WDM filters. The structure includes a bus waveguide, drop waveguide, and an inner quasi-square ring resonator formed by silicon rods (dielectric constant 11.68) in air. A line defect in the inner ring minimizes radiation losses, improving performance. Simulated using the 2D Finite Difference Time Domain (FDTD) method, the filter achieves a drop wavelength of 1636.2 nm, bandwidth of

0.7 nm, quality factor of 2337, and 100% dropping efficiency within a compact area of 412.76 μm², making it suitable for future Photonic Integrated Circuits (PICs) [54].

A comprehensive literature review highlights that conventional logic gates often have larger footprints, slower response times, and lower contrast ratio. To address these limitations, we propose an optimized AND gate design that minimizes footprint, enhances response time, and improves contrast ratio. The proposed design utilizes a hexagonal lattice within a two-dimensional photonic crystal (2DPC) structure. Key performance metrics, including contrast ratio, bit rate, response time, and normalized efficiency, are thoroughly evaluated. The study focuses on the design and performance analysis of two-input and three-input AND gates. The paper is structured as follows: Sections II Field Equations and Section III & IV discuss the design and simulated performance results of the proposed two-input and three-input AND gates. Section V concludes with a summary of the findings.

## 2. Field equations

In photonic crystal-based optical logic gates, Perfectly Matched Layer (PML) boundary conditions are used to absorb outgoing electromagnetic waves and prevent artificial reflections at the edges of the simulation domain. The PML acts as an absorbing layer surrounding the photonic crystal structure, ensuring that light leaving the computational region does not reflect and interfere with the internal fields. By gradually increasing the material conductivity within the PML region, electromagnetic waves are attenuated smoothly, in an open or infinite space. This provides accurate simulation of wave propagation, transmission, and logic operation. Thus, PML boundaries are essential for achieving high numerical accuracy and realistic optical performance in photonic crystal logic gate simulations.

The 2D Finite Difference Time Domain (FDTD) works with the Perfect Matched Layer Absorbed Boundary Condition (PML ABC). The PML ABC is an artificial boundary layer to support the simulation in open boundary condition (Free space), the PML strongly absorbs all the incident waves in all directions, angle without any reflection inside the PC lattice (Chew et al. 1996).

To work in FDTD, it is important to choose the proper spatial and temporal grid size and time step to match the simulation output with a real time system (Xiao et al. 1993). The proper grid size is calculated using the a/16=40 nm and time step of A t=0.02203 is used in the FDTD algorithm, it provides stable output and less time leads to oscillation output. The time step calculated by

$$\Delta t \leq \frac{1}{c\sqrt{\frac{1}{\Delta x^2}+\frac{1}{\Delta z^2}}}$$

where denotes the step time. C denotes the speed of light in free space respectively, Δt indicates step time, and Δx and Δz are grid sizes in X-Z axes. The Perfectly Matched Layer (PML) is placed and it acts as the absorbing boundary condition to diminish optical loss in turn provides excellent performance. Two-dimensional photonic crystal (2D-PC) simulations employ Perfectly Matched Layer (PML) boundary conditions to effectively absorb outgoing electromagnetic waves and avoid artificial reflections at the computational domain boundaries. This is especially crucial when analysing the behaviour of photonic crystals numerically using techniques like the Finite Difference Time Domain (FDTD) methodology.

### 2.1. PWE method

The PWE method is a frequency-domain approach that solves Maxwell's equations by expanding the electromagnetic fields and dielectric function in terms of plane waves.[45]

$$\nabla . H(r,t) = 0 \tag{1}$$

$$\nabla \times H(r,t) + \mu_0 \frac{\partial H(r,t)}{\partial t} = 0 \tag{2}$$

$$\nabla . [\varepsilon(r) E(r,t)] = 0 \tag{3}$$

$$\nabla \times H(r,t) - \varepsilon_0 \varepsilon(r) \frac{\partial E(r,t)}{\partial t} = 0 \tag{4}$$

The wave equations for the photonic crystal structure in the frequency domain are derived in Eqs 5 and 6 [46,47].

$$\nabla \times \left(\frac{1}{\varepsilon(r)} \nabla \times H(r)\right) = \left(\frac{\omega}{c}\right)^2 H(r) \tag{5}$$

$$\nabla \times \left(\frac{1}{\varepsilon(r)} \nabla \times E(r)\right) = \left(\frac{\omega}{c}\right)^2 E(r) \tag{6}$$

### 2.2. FDTD method

FDTD is a time-domain numerical technique used to solve Maxwell's equations directly by discretizing both space and time using the finite-difference method [48].

$$f(i\Delta x, j\Delta y, k\Delta z, n\Delta t) = f^n_{i,j,k} \tag{7}$$

$$\frac{\partial f}{\partial x}(i\Delta x, j\Delta y, k\Delta z, n\Delta t) = \frac{f^n_{i+\frac{1}{2},j,k} - f^n_{i-\frac{1}{2},j,k}}{\Delta x} + O[(\Delta x)]^2 \tag{8}$$

$$\frac{\partial f}{\partial t}(i\Delta x, j\Delta y, k\Delta z, n\Delta t) = \frac{f^{n+\frac{1}{2}}_{i,j,k} - f^{n-\frac{1}{2}}_{i,j,k}}{\Delta x} + O[(\Delta x)]^2 \tag{9}$$

where Δx, Δy, Δz are the spatial increments along the x, y, and z axis respectively and Δt is the temporal increment. i, j, k, and n are the integers.

The input and output power are calculated by the time monitor and the power is calculated by using the following equation [44]

$$T(f) = \frac{1/2 \int \text{real}\,(p(f)^{\text{monitor}})dS}{\text{Source Power}} \quad (10)$$

where T(f) is a signal power, dS indicates a surface normal, and p(f) Poynting vector. The FDTD method separates the electric or magnetic fields into time and space by Maxwell's equation.

### 2.3. Design of two input AND Gate

The silicon rods are used in the reported all-optical two-input AND logic gate, which has a 21x21 hexagonal lattice. The proposed structure has line and points defects to reduce structural design and signal power loss. The refractive index is 3.46, the lattice constant is 560 nm, and the rod radius is 0.11 nm. Fig. 1 shows the reported logic gate band diagram.

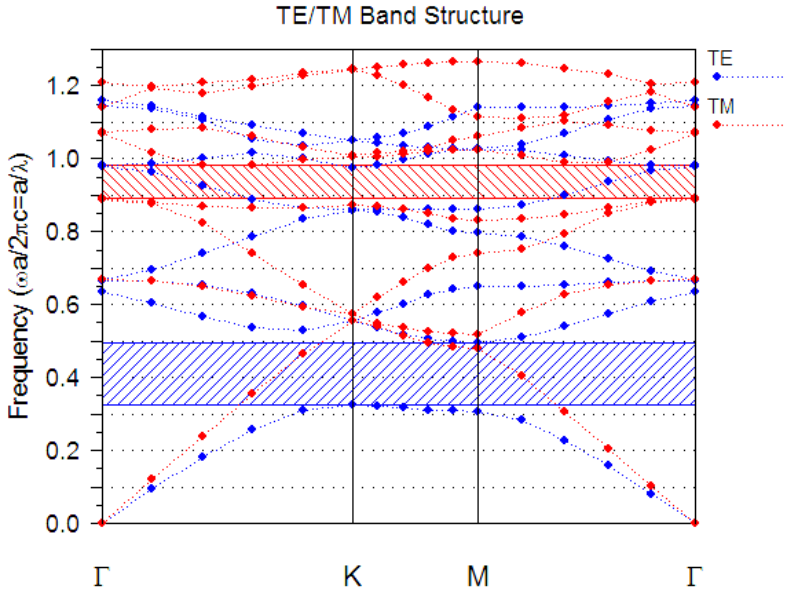



*Fig. 1. PC Band diagram of periodic structure (colour online)*

The Plane Wave Expansion (PWE) method is used to determine the band structure prior to the creation of the defects. The proposed all-optical logic gate construction consists of Transverse Magnetic (TM) PBG and Transverse Electric (TE) PBG components. The PBG region for TE mode varies from $0.324<a/\lambda<0.495$, which is equal to $1365\text{nm}<\lambda<1795$ nm. Similarly, the TM PBG is calculated $0.892<a/\lambda<0.983$, which is equal to $590\text{nm}<\lambda<650$ nm. Here, the first TE PBG is considered for this structure. Fig. 2a shows the proposed two-input AND gate, which has one output port (Port Y) and input ports (Ports A and B). The structure combines with a Y-shaped waveguide, where a row of rods is removed to create the input and output ports.

The silicon material used for the operating wavelength of 1550 nm is selected by the author from the literature [16]. For two-dimensional photonic crystal (2D-PC) based logic gates, silicon's refractive index (3.46) is selected due to its high contrast in refractive index compared to materials such as air, which is necessary to create strong photonic bandgaps needed for efficient light manipulation and confinement. An inner rod is created in between the two waveguides.to increase the transmission efficiency and to optimize the better functional parameters. Most integrated circuits use silicon as a substrate. Fig. 2(a) shows the schematic structure of AND gate, and (b) depicts the 3D view of the proposed AND gate.

The main idea of the proposed work is based on the interference pattern generated by the optical signals arriving from the two input ports (A and B). In the designed structure, the logic operation is realized through the constructive and destructive interference of light waves within the photonic crystal waveguide region. When both input signals are present (logic '1'), their interaction leads to constructive interference at the output port, resulting in high output power corresponding to logic '1'. In contrast, when only one or neither of the inputs is active, destructive interference occurs, causing the output intensity to drop to a low-level representing logic '0'. The optimized placement of line and point defects, as well as the inclusion of an inner defect rod between the two waveguides, ensures that the phase matching and modal overlap between the inputs are properly maintained to achieve the desired interference behaviour. This interference-based mechanism is essential for improving signal transmission efficiency, contrast ratio, and overall performance of the AND logic gate. Thus, the design not only utilizes the refractive index contrast and biperiodicity for light confinement but also effectively exploits the interference phenomenon to realize accurate and efficient all-optical logic operation.

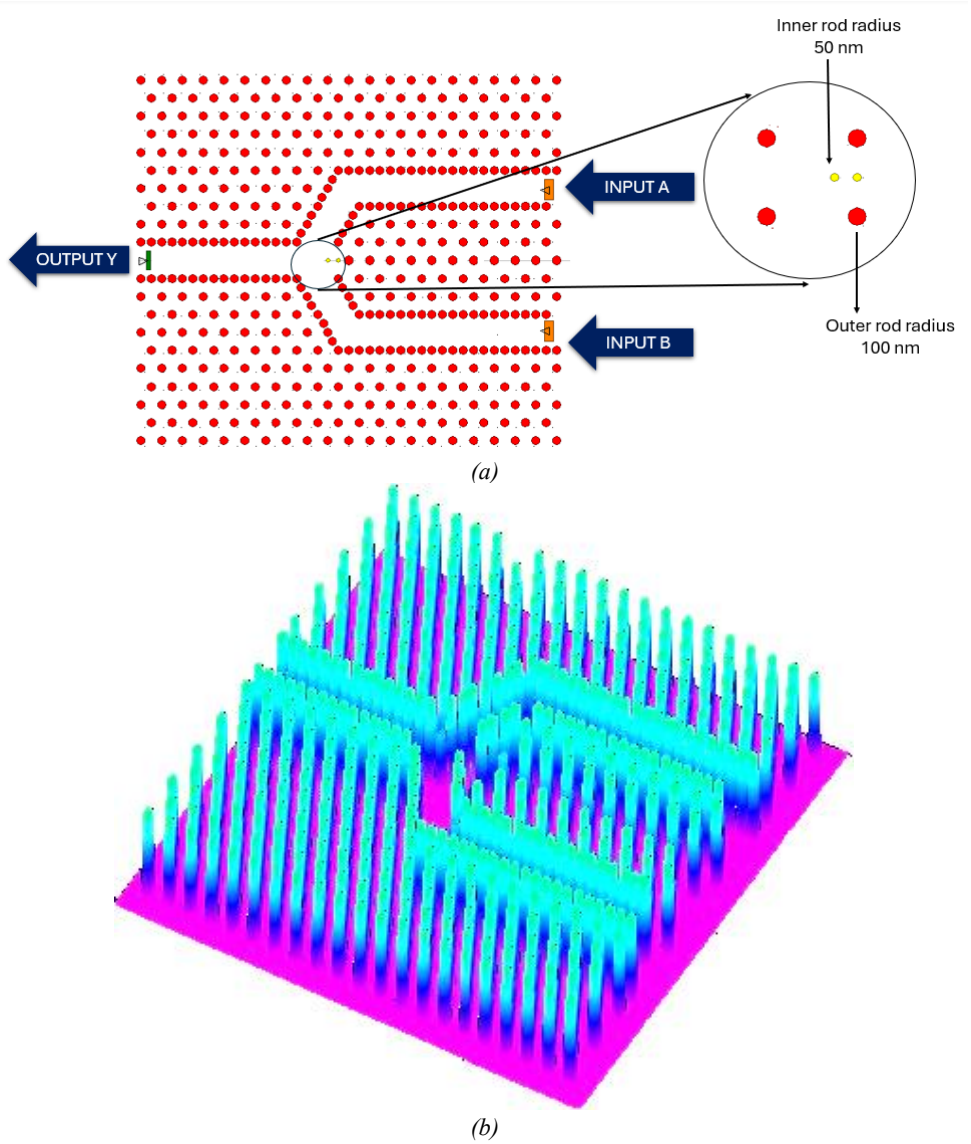



*Fig. 2. (a) Schematic structure of two input AND gate (b) 3D view of the proposed AND gate (colour online)*

The defects are selected by optimization techniques. Initially, the structural parameters of the proposed device, such as, radius of the rod, lattice constant and refractive index of the materials, are selected through a gap map. Generally, the gap map provides variation of TE/TM PBG by varying the structural parameters. The gapmap shown in Figs. 3 (a), (b), and (c) represent variation of TE/TM PBG, which is obtained by varying the defect size (a), the radius of the rod and lattice constant (b) and refractive index difference (c). In these Figs., the blue region indicates the variation of TE PBG with respect to the radius of the rods, period and delta, similarly red region indicates for TM PBG. The vertical yellow line over the blue region shows the TE PBG region of the structure without introducing defects. The values to design the proposed device in the first reduced TE PBG are optimized through gapmap, which are rod radius (0.11μm), refractive index (3.46) and period (560 nm) is indicated in the below gapmap.

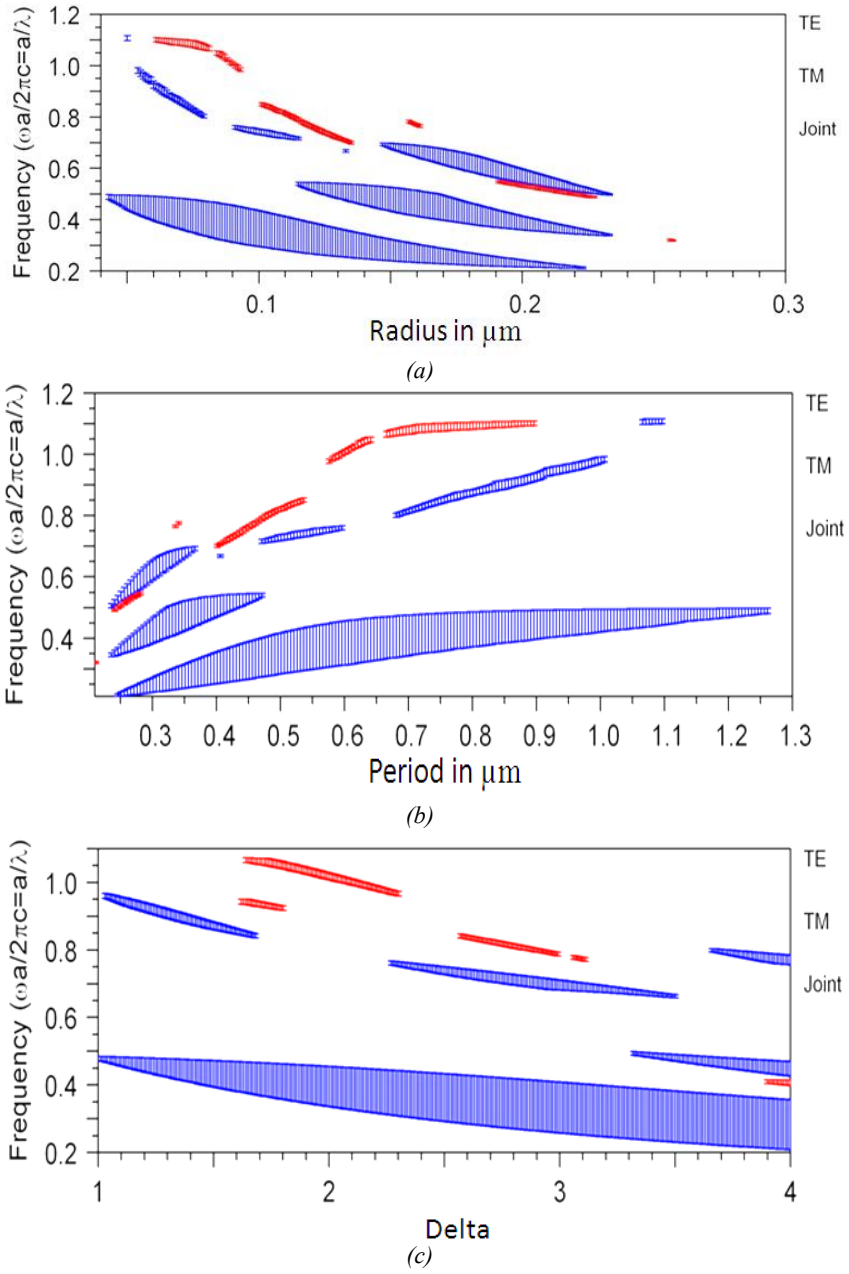



*Fig. 3. Effect of gapmap by varying (a) Radius of the rod, (b) Period (Lattice constant), and (c) Delta (Index contrast) (colour online)*

The defects in the proposed all-optical AND logic gate were chosen through parametric analysis. The inner and outer rod radii were varied systematically to study their effect on transmission efficiency, output power, and contrast ratio for both two-input and three-input AND gates. The optimization process focused on achieving the best interference condition and maximum light confinement inside the waveguide. The inner defect rod was introduced between the two waveguides to enhance coupling and improve signal transmission, while the outer rods were adjusted to reduce scattering and back-reflection. Through this parametric optimization, the structure achieved better functional performance and higher output efficiency compared to unoptimized configurations.

To enhance light confinement and minimize scattering losses, the concept of biperiodicity is introduced in photonic crystal waveguides. By using two different periodicities along perpendicular directions, biperiodic structures help in controlling light propagation more effectively. This improves the efficiency of the waveguide by reducing unwanted radiation losses and enhancing the photonic bandgap. The anisotropic nature of biperiodic photonic crystals allows better mode confinement, leading to lower dispersion and improved transmission. Such designs are particularly useful in high-performance optical communication and sensor applications. The modified periodic structure helps in reducing back-reflection and increasing waveguide robustness. As a result, light signals travel with higher efficiency, making biperiodic waveguides ideal for integrated photonic circuits.

The radius of the rod varied from its original position and adjusting structural characteristics like the refractive

index and rod radius to maximize transmission efficiency. In particular, the outer rod has a refractive index of 3.46 and a radius of 0.05μm. To increase efficiency, a defect rod is positioned carefully between the waveguide and resonator. Two input ports, A and B, receive the input signal, while output port Y receives the output signal. The power is computed using the time monitor to determine the input and output power.

*Table 1. Truth table of two input AND gate*

| INPUT A | INPUT B | OUTPUT Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Table 1 lists the truth table for the two input AND gate. The input signal is given to two input ports A and B and the output is obtained at output port Y for different logics.

*Table 2. The structural parameters of the proposed AND gate*

| Sl. No | Parameter | Value |
|---|---|---|
| 1 | The lattice constant (a) | 560nm |
| 2 | The radius of rods (r) | 110nm |
| 3 | The refractive index of rods (Si) | 3.46 |
| 4 | Operating Wavelength | 1550 nm |
| 5 | Input Power | 1mW |
| 6 | No of silicon rods in x & z direction | 21 x 21 |
| 7 | The radius of Nano cavity rods 1 & 2 | 50 nm |
| 8 | No of input waveguides | 2 |
| 9 | No of output waveguides | 1 |
| 10 | Footprint of the encoder | 129.32 μm². |

Table 2 depicts the structural parameters of AND gate. In the designed all-optical AND logic gate, the contrast ratio represents the difference between the output power levels of logic '1' and logic '0'. When the contrast ratio is not high, it means the difference between these two output states is small. This happens due to incomplete interference, scattering losses, or slight leakage of light in the waveguide. Low contrast causes unclear signal distinction, making it difficult to identify whether the output is logic '1' or logic '0'. As a result, when this structure is coupled with other photonic devices or circuits, the weak signal difference may lead to signal distortion or loss of information. To overcome this issue, the structure needs to be optimized by adjusting parameters such as rod radius, defect position, and refractive index, or by introducing a reference signal to stabilize the interference and improve light confinement. This helps to achieve a higher contrast ratio, ensuring better coupling and more efficient operation in integrated photonic circuits.

CASE 1: A signal propagates inside the bus waveguide and the output power reached at the port Y, when any one of the inputs is ON (A=1, and B=0) illustrates in Fig. 4(a).

CASE 2: Light travels toward the point defect formed at the centre of the structure when one of the inputs is ON (A=0 and B=1) and the input power is delivered to Port A. Based on the logic the power not resonated inside the waveguide which depicts in Fig. 4(b).

CASE 3: Under certain resonant conditions, the input power enters through Ports A and B when both inputs are ON (A=1 and B=1). It then propagates across the structure and signal reached at the output port in Fig. 4(c). The output power for logic 0 reached at the output port as 0 and for logic 1 as 1.00.

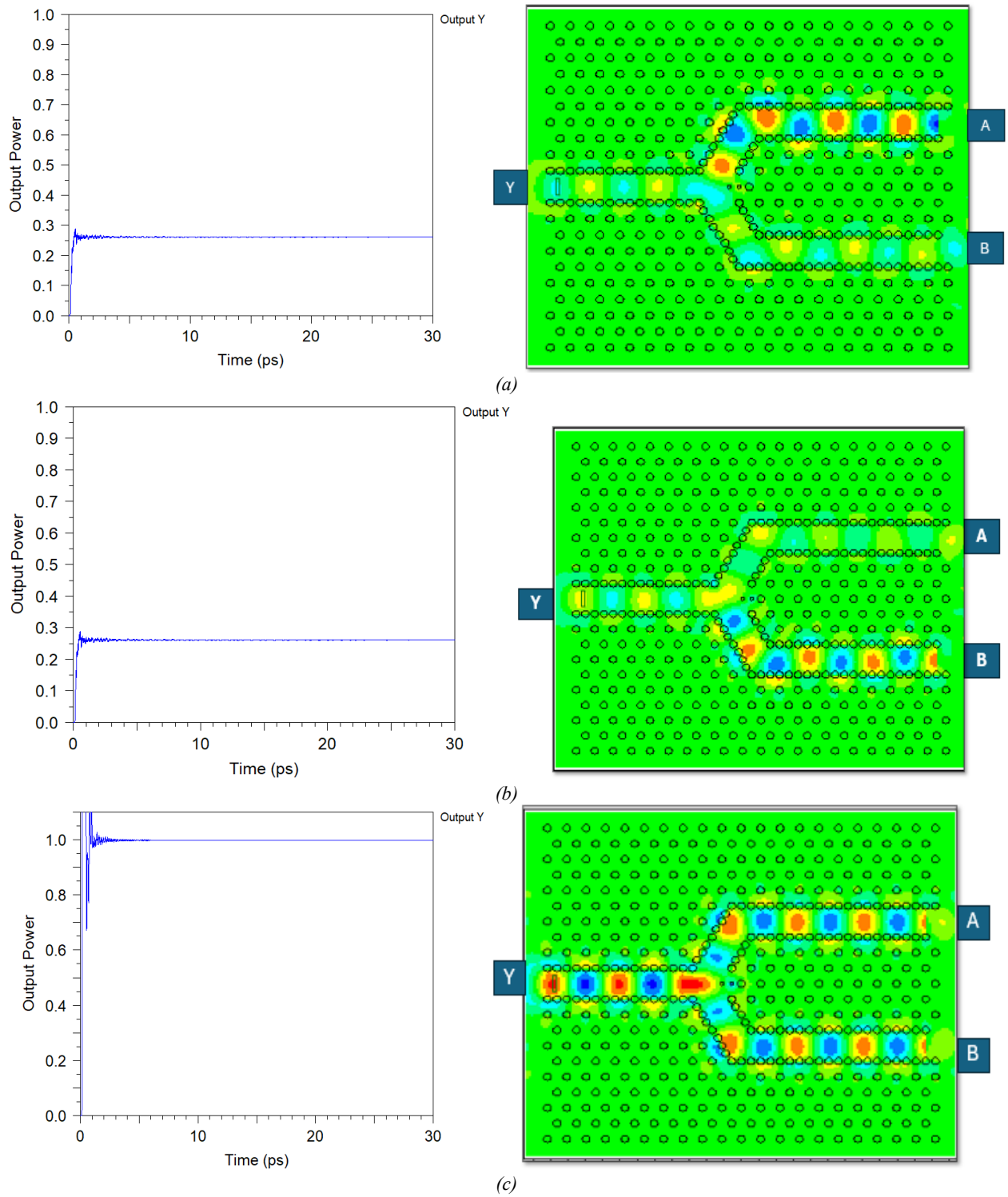



*Fig. 4. Field distribution and output of two input AND gate (a) A=1,B=0and Y=0, (b) A=0, B=1 and Y=0 and (c) A=1,B=1and Y=1 (colour online)*

### 2.4. Response time and steady-state time

Response time $t_r$ is signal initiation, and steady-state time $t_s$ evaluates stability. The response time $t_r$ is calculated between 10% and 90% of normalized power, which reflects the device's transition speed to stability. Steady-state time signifies system equilibrium, and steady-state time denotes the duration to reach this equilibrium.

#### *2.4.1. Bit rate*

Bit rate defines information transfer speed, directly impacting data transmission capacity. It is calculated from the output signal's time response, being the reciprocal of the response time.

$$Bit\,Rate = \frac{1}{\mathrm{Re}sponse\ \ Time}$$

### *2.4.2. Contrast ratio*

The contrast ratio in an all-optical logic gate represents the difference between the output powers corresponding to logic '1' and logic '0'. When a reference signal is used, it provides a stable phase and amplitude reference that helps control the interference pattern between the input signals. This improves phase matching and reduces unwanted fluctuations or background noise within the waveguide. As a result, constructive interference for the logic '1' state becomes stronger, and destructive interference for the logic '0' state becomes deeper. The reference signal essentially enhances the signal-to-noise ratio and stabilizes the power levels at the output port. Therefore, by minimizing residual leakage during logic '0' and amplifying the transmitted signal during logic '1', the contrast ratio significantly improves, leading to more distinct and reliable logic operation.

The contrast ratio defines the distinction between different optical signal intensities, which is crucial for signal accuracy. The contrast ratio indicates the power margin between logics 1 and 0. which is defined by

$$Contrast\ Ratio = 10\log\frac{P_{High}}{P_{Low}}\ \ in\ dB$$

where $P_{high}$ and $P_{low}$ represent the highest and lowest power levels at output ports for each logic state, respectively.

*Table 3. Functional parameters of all optical two input AND gate*

| Input A | Input B | Output Y | Pout/ Pa | Response Time | Contrast Ratio | Bit Rate |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0.00 | 0.24 ps | 7.435 dB | 4.16 Tbps |
| 0 | 1 | 0 | 0.20 | | | |
| 1 | 0 | 0 | 0.20 | | | |
| 1 | 1 | 1 | 1.00 | | | |

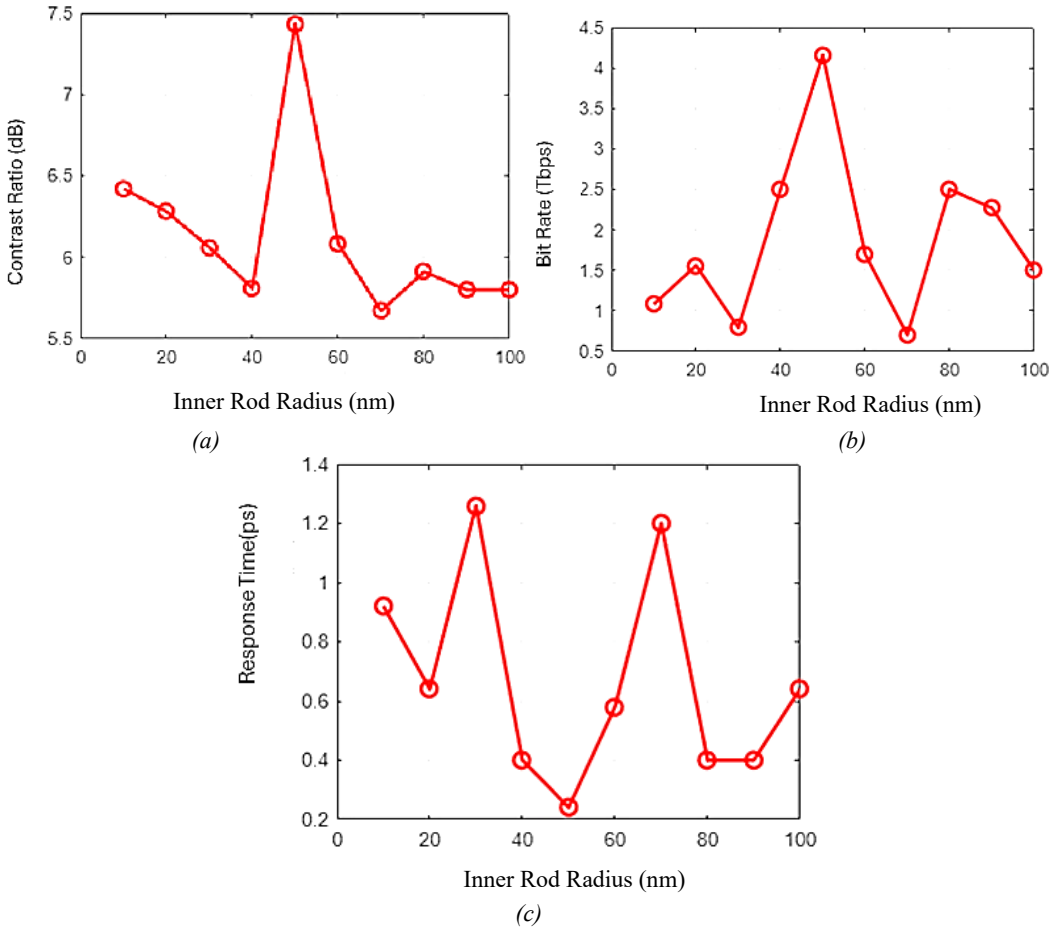


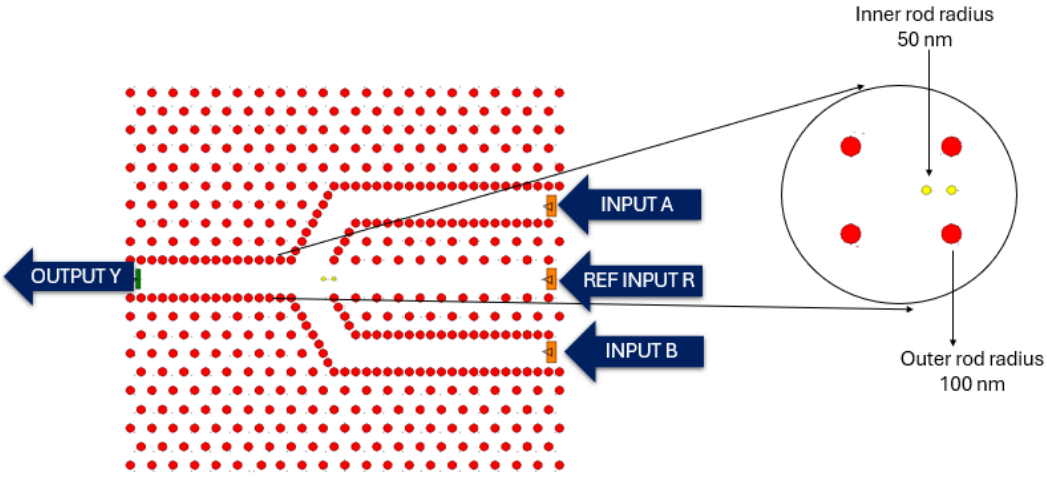

*Fig. 5. Impact of inner rod radius of two input AND gate (a) Contrast ratio vs Inner rod Radius (b) Bitrate vs Inner rod Radius (c) Response time vs Inner rod Radius (colour online)*

Table 3 depicts the functional parameters of the optical two input AND gate. The response time achieved as 0.24 ps, bit rate achieved as 4.16 Tbps and it offers a contrast ratio as 7.435 dB. To increase the transmission efficiency and improve the better performance of the device parametric analysis has been done for the inner rod. In Fig. 4, A graphical response curve was plotted to analyze functional parameters, including contrast ratio, bit rate, and response time, concerning the inner rod radius. The maximum values for contrast ratio, bit rate, and response time were determined. The relationship between these parameters and the inner rod radius was observed. The results highlight the optimal inner rod radius for enhanced performance. The study provides insights into improving photonic crystal designs. These findings are crucial for optimizing photonic device efficiency.

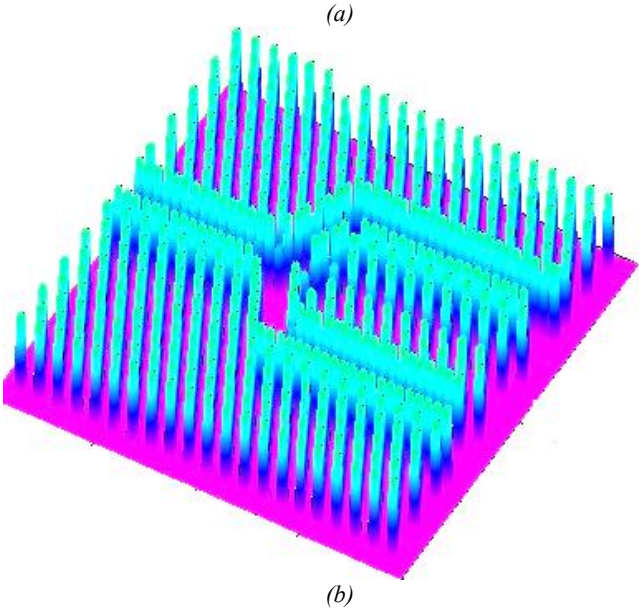
Optimizing the functional parameters by varying the inner rod radii, initially set at 50 nm, enables a high bit rate. A maximum bit rate of 4.16 Tbps and a response time of 0.24 ps are achieved. Based on the parametric analysis the inner rod radius varied by 5 nm step index in order to attain the maximum efficiency. To optimize accuracy, the inner rod radius is varied in 5 nm step increments. Various functional parameters, including contrast ratio, bit rate, and response time, will be analysed. The impact of radius variation on optical performance is assessed systematically. Higher contrast ratios ensure improved signal clarity. Bit rate variations determine data transmission efficiency. Response time evaluation aids in optimizing system speed. The study provides insights into design enhancements. Fig. 5 depicts the response curve of (a) Contrast ratio vs Inner rod Radius (b) Bitrate vs Inner rod Radius (c) Response time vs Inner rod Radius.

### 2.5. Design of three input AND gate

A 21 × 21 hexagonal lattices embedded with silicon rods makes up the suggested all-optical three-input AND logic gate depicts in Fig. 6 a and 3D view of three input AND gate depicts in Fig. 6 b.



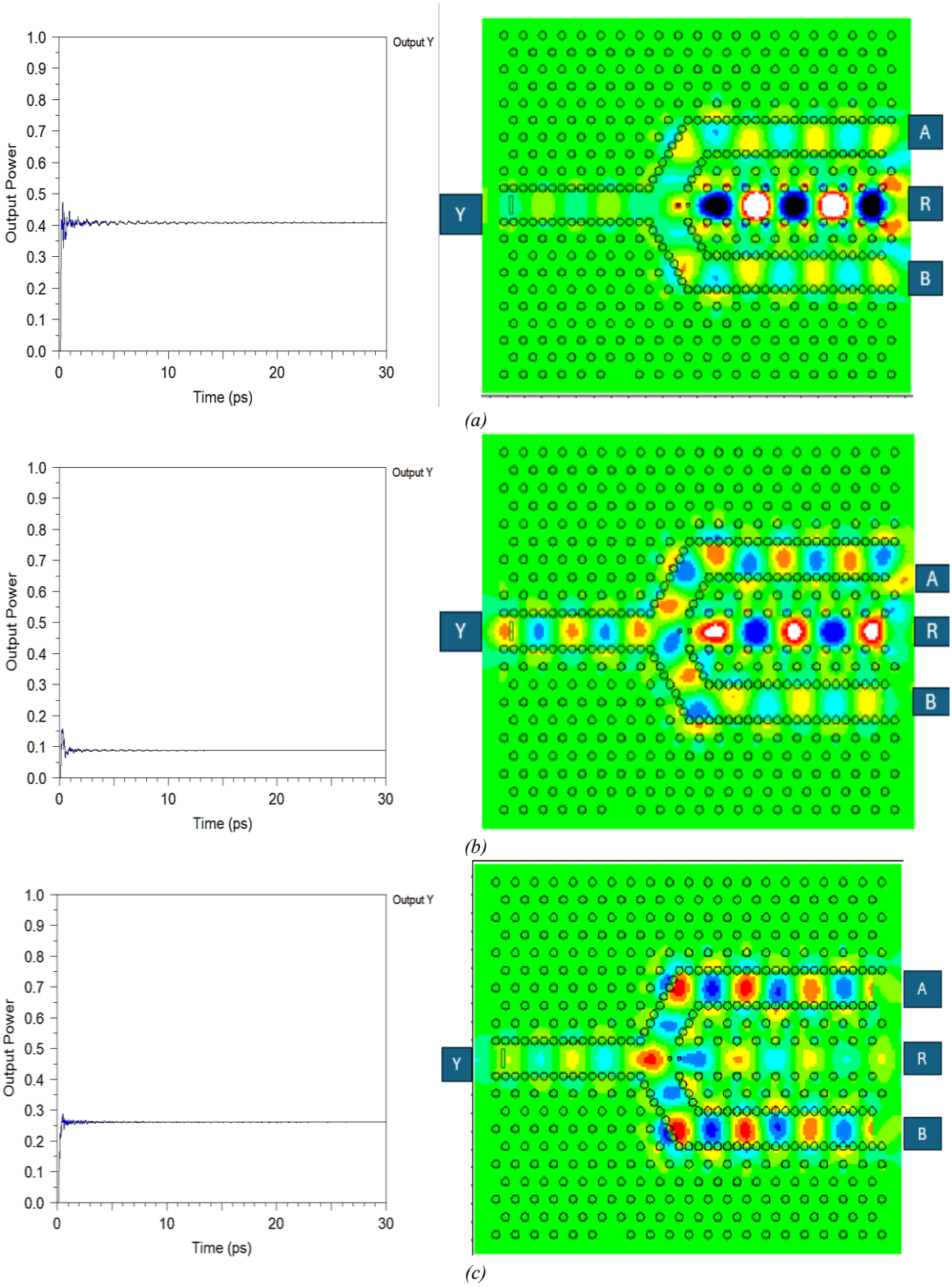

*(a)*

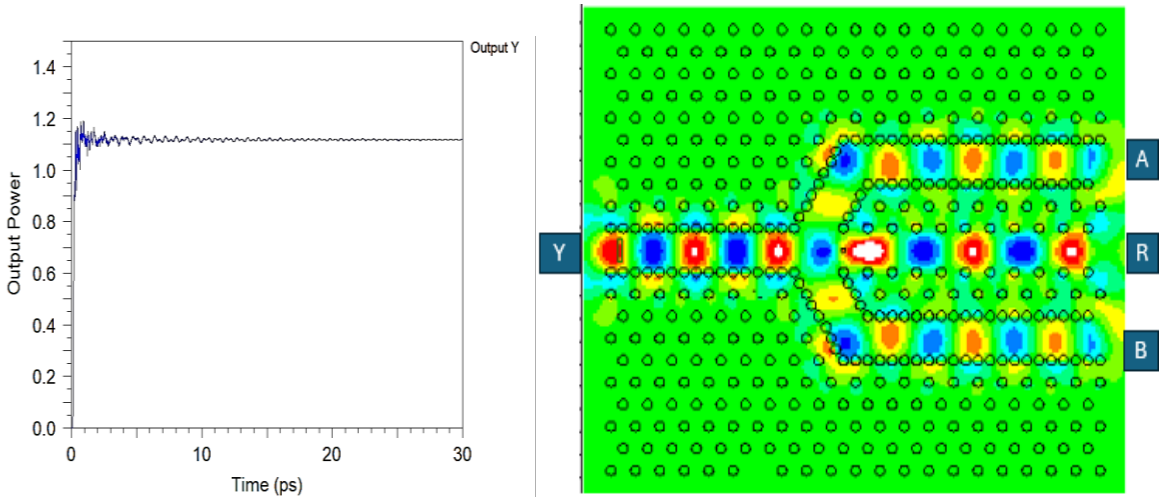


*(b)*

*Fig. 6. (a) Schematic structure of three input AND gate and (b) 3D View of three input AND gate (colour online)*

This structure is made up of line and point defects, and its structural properties, including the lattice constant, the rods' refractive index, and the radii of the rods and defect rods, are all the same as those of the two-input AND gate. The three-input AND gate, which was added to the original two-input design, has three input ports: input port A, input port B, and a reference input port R. The output response significantly improves when the reference input is compared to the two-input AND gate.






*(d)*

*Fig. 7. Signal propagation and output of three input AND gate (a) A=0, R=1, B=0 and Y=0, (b) A=1, R=1, B=0 and Y=0, (c) A=1, R=0, B=1and Y=0 and (d) A=1, R=1, B=1and Y=1 (colour online)*

The structure's design incorporates both line and point defects. Its structural parameters, including the rod's radius, lattice constant, refractive index, and defect rods, are similar to those of two-input AND gates. The proposed three-input AND gate configuration consists of three input ports: input ports A and B, along with a reference input R. Compared to a two-input AND gate, the output response improves when the reference input is included. Fig. 6b depicts the three-dimensional view of proposed three input AND gate.

Compared to applying inputs through ports A and B in the suggested configuration, the total system performance is improved when the reference input is used. In the proposed design, the reference input is set to 1. The output remains zero when the reference input is 1. When both input ON along with the reference input the power reaches the output port. The structural parameters of three-input AND gate is shown in Table 4. The three-input AND gate's electric field distribution is shown in Fig. 7.

*Table 4. Functional parameters of three input AND gate*

| Input A | Input B | Ref Input R | Output Y | Pout/Pa | Response Time | Contrast Ratio | Bit Rate |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0.1 | 0.56 ps | 10.71 dB | 1.78 Tbps |
| 0 | 1 | 1 | 0 | 0.2 | | | |
| 1 | 0 | 1 | 0 | 0.2 | | | |
| 1 | 1 | 1 | 1 | 1.00 | | | |

Table 4 presents the functional parameters of the three-input AND gate, including contrast ratio, response time, and bit rate. The response time, bit rate, and contrast ratio for the three-input AND gate are 0.56 ps, 1.78 Tbps, and 10.71 dB, respectively.

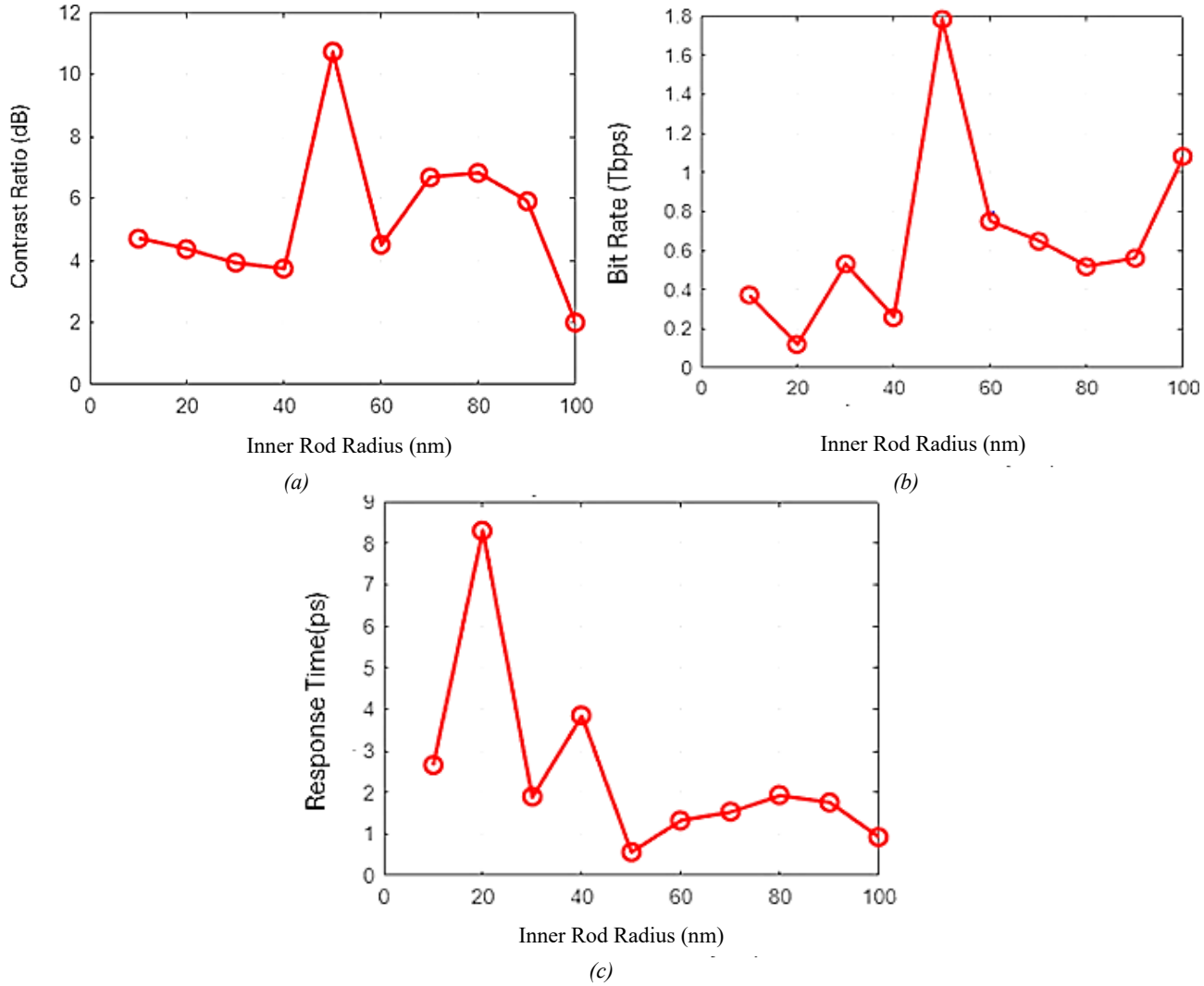



*Fig. 8. Impact of inner rod radius of three input AND gate (a) Contrast ratio vs Radius (b) Bit rate vs Radius (c) Response time vs Radius (colour online)*

By iteratively adjusting the inner rod radii, set initially at 50 nm, a high bit rate is achieved. Notably, as the rod radii are increased, the contrast ratio shows a linear improvement, leading to a significant reduction in response time. The optimization results in functional parameters yielding a maximum bit rate of 1.78 Tbps and a response time of 0.56 ps Fig.7 shows the response curve of three input AND gate. During the parametric analysis of the inner rod radius, optimization was carried out to achieve accurate logic operation and enhance transmission efficiency. The study focused on improving key functional parameters, including contrast ratio, bit rate, and response time. By varying the inner rod radius in systematic increments, the impact on these parameters was thoroughly examined. As shown in Fig. 8, it is evident that a rod radius of 50 nm provides the most favourable results. At this optimized radius, all functional parameters exhibited significant improvements, ensuring better optical performance. The contrast ratio was enhanced, leading to improved signal clarity and reduced noise. The achieved bit rate was higher, supporting efficient data transmission. Additionally, response time was optimized, contributing to faster processing and reduced latency. These findings demonstrate the effectiveness of radius optimization in improving overall system performance. The results provide valuable insights for designing high-performance optical logic gates.

*Table 5. Comparison of Functional parameters of the reported AND gate with proposed one*

| Authors | Lattice | Gates | Defect | Size | Contrast Ratio | Bit Rate | Response Time |
|---|---|---|---|---|---|---|---|
| Marziyeh Moradi et al., 2024 [28] | Square | AND | Non linear effect | 175 $\mu m^2$ | 13.17 dB | *** | 2ps |
| Parisa Andalib et al., 2009 [30] | Square | AND | Line and point defect | *** | *** | *** | 120Gbits/s |
| Yuhei Ishizaka et al., 2011 [31] | Triangular | AND | X shaped line defect | *** | 6.79dB | *** | *** |
| Aryan Salmanpour et al., 2015 [32] | Triangular | AND.XOR | Ring Resonator | *** | 16.7dB | 333Gbits/s | 3ps |
| Mohammad Danaie et al., 2012 [33] | Triangular | AND | Y shaped line defect | $100\mu m^2$ | *** | *** | 1ps |
| Parandin et al., 2017 [34] | Triangular | NOT & AND | E shaped line defect | *** | *** | 1.54Tbit/s | *** |
| EH. Shaik et al., 2015[35] | Cubic | AND | Y shaped line defect | *** | 5.74dB | 6.26Tbps | *** |
| Jayson K. Jayabharathan et al. [41] | Triangular | AND | Diagonal shaped line defect | *** | 6.64 dB | 2.06 Tbps | 0.48 ps |
| Proposed Work | Triangular | AND | E shaped line defect | 129.32 $\mu m^2$ | 2 input – 7.435dB 3 input- 10.71 dB | 2 input- 4.16 Tbps 3 input- 1.78 Tbps | 2 input – 0.24 ps 3 input – 0.56 ps |

Table 5 The functional parameters of the proposed AND gate is compared with previously reported logic gates. Aryan Salmanpour et al. designed an all-optical AND gate, evaluating functional parameters such as contrast ratio, bit rate, and response time. Although their design achieved a higher contrast ratio, it exhibited a longer response time [32]. Meanwhile, E. H. Shaik et al. also designed an AND gate, where investigations revealed a higher bit rate but a lower contrast ratio compared to the proposed work. Similarly, Jayson K et al. developed an all-optical AND gate with a high bit rate, though the contrast ratio remained minimal. Additionally, Mariyeh Moradi et al. designed an AND gate with a longer response time than the reported work. These gates were designed using cubic or hexagonal lattices with various defect shapes (E, F, T, H, Y) and ring resonators. The proposed AND gate exhibits superior performance over existing designs, featuring a higher bit rate but a reduced contrast ratio. While some reported designs show improvements in contrast ratio, bit rate, and response time, they are larger in size, not specifically designed for an AND gate. Due to its compact size and rapid response time, the proposed AND gate is well-suited for high-speed computing, photonic integrated circuits, and switching devices.

## 3. Conclusion

In this paper two-dimensional photonic crystals based all optical AND gates with two and three inputs are designed and analyzed. The AND gate has a resonance wavelength of 1550 nm. Utilizing the FDTD approach, the functional parameters such as contrast ratio, bit rate and response time were determined. The suggested two input and three input AND gate has a contrast ratio, response time, and bit rate of 7.435 dB, 0.24 ps, 4.16 Tbps, and 10.71 dB, 0.56 ps, 1.78 Tbps, respectively. For next-generation optical computing and communication systems, the gate is a viable option due to its small size and quick functioning. Its efficiency in handling fast data processing demonstrates its appropriateness for sophisticated optical networks. This design paves the way for future advancements in all-optical logic gate technologies, contributing to the development of reliable and highly efficient photonic integrated circuits.

## References

[1] Aryan Salmanpour, Shahram Mohammad Nejad, Ali Bahrami, Optical and Quantum Electronics **47**(7), 2249 (2015).
[2] M. Pirzadi, A. Mir, D. Bodaghi, IEEE Photonics Technology Letters **282**(1), 2387 (2019).
[3] Lila Mokhtari, Hadjira Abri Badaoui, Mehadji Abri, Moungar Abdelbasset, Farah Lallam, Bachir Rahmi, Progress in Electromagnetics Research C **106**, 187 (2020).
[4] Preeti Rani, Yogita Kalra, R. K. Sinha, Optik **126**(9), 950 (2015).
[5] Jeevan Jot Singh, Divya Dhawan, Neena Gupta, Optics and Laser Technology **165**, 109624 (2023).
[6] D. Saranya, Rajesh Anbazhagan, Optical and

Quantum Electronics **52**(8), 370 (2020).
[7] R. Arunkumar, T. Suganya, S. Robinson, International Journal of Photonics and Optical Technology **3**(1), 30 (2017).
[8] T. Suganya, S. Robinson, ICTACT Microelectron **3**(1), 349 (2017).
[9] T. Betsy Saral, S. Robinson, R. Arunkumar, International Journal of Photonics and Optical Technology **2**(4), 1 (2016).
[10] Taiyo Zhao, Mehrnoush Asghari, Ferhad Mehdi Zadeh, Journal of Electronic Materials **48**(4), 2482 (2019).
[11] K. Venkatachalam, S. Robinson, S. K. Dhamodharan, Opto Electronics Review **25**(2), 74 (2017).
[12] Hamed Alipour Banaei, Photonic Networks Communications **29**(2), 146 (2015).
[13] Fatemeh Haddadan, Mohammad Soroosh, Photonic Network Communications **37**(1), 83 (2019).
[14] R. Rajasekar, R. Latha, S. Robinson, Materials Letters **251**, 144 (2018).
[15] Fariborz Parandin, Gailan I. Kareem Chimawi, Saeed Olyaee, Scientific Reports **14**, 1 (2024).
[16] R. Arunkumar, S. Robinson, Silicon **16**, 4997 (2024).
[17] K. Latha, R. Arunkumar, K. Rama Prabha, S. Robinson, Silicon **14**, 3245 (2021).
[18] Fatemeh Haddadan, Mohammad Soroosh, Photonic Network Communications **37**(1), 83 (2019).
[19] S. Khosravi, M. Zavvari, Photonic Network Communications **35**(1), 122 (2018).
[20] Amir Hosein Esmaeili, Shadi Daghighazar, Iman Chaharmahali, Ramin Zohrabi, Kiyanoush Goudarzi, Optical and Quantum Electronics **56**, 1 (2024).
[21] Hojjat Sharifi, Seyedeh Mehri Hamidi, Keivan Navi, Photonics and Nanostructures **27**(1), 55 (2017).
[22] S. Robinson, R. Nakkeeran, Optical Engineering **51**(11), 114001 (2012).
[23] S. Robinson, R. Nakkeeran, Optics and Photonic Journal **1**(3), 142 (2011).
[24] Aref Rahmani, Farhad Mehdizadeh, Optical and Quantum Electronics **50**(1), 30 (2018).
[25] R. Rajasekar, K. Parameshwari, S. Robinson, Plasmonics **14**(6), 1687 (2019).
[26] Enaul Haq Shaik, Nakkeeran Rangaswamy, Optical and Quantum Electronics **48**(3), 335 (2016).
[27] K. Rama Prabha, S. Robinson, Silicon **13**, 3521 (2020).
[28] Marziyeh Moradi, Mohammad Danaie, Ali Asghar Orouji, Optical and Quantum Electronics **127**, 1 (2021).
[29] H. M. E. Hussien, T. A. Ali, H. N. Rafat, Optic Communication **41**(1), 175 (2018).
[30] Parisa Andalib, Nosrat Granpayeh, Journal of the Optical Society of America **26**(1), 10 (2009).
[31] Yuhei Ishizaka, Yuki Kawaguchi, Kunimasa Saitoh, Masanori Koshiba, Optics Communications **284**(14), 3528 (2015).
[32] Aryan Salmanpour, Shahram Mohammadnejad, Ali Bahrami, Journal of Modern Optics **62**(9), 693 (2015).
[33] Mohammad Danaie, Hassan Kaatuzian, Optical and Quantum Electronics **44**, 27 (2012).
[34] F. Parandin, M. M. Karkhanehchi, Superlattices and Microstructures **101**, 253 (2016).
[35] Enaul Haq Shaik and Nakkeeran Rangaswamy, Journal of Modern Optics **63**(10), 941 (2015).
[36] Enaul Haq Shaik, Nakkeeran Rangaswamy, Journal of Optics **47**(1), 8 (2017).
[37] Priyanka Kumari Gupta, Punya Prasanna Paltani, Shrivishal Tripathi, Physica Scripta **99**(11), 115541 (2024).
[38] Maddala Rachana, Sandip Swarnakar, Sabbi Vamshi Krishna, Santosh Kumar, Applied Optics **61**(1), 77 (2022).
[39] Dongxing Meng, Yaqi Hu, Yule Xue, Proc. SPIE **12162**, International Conference on High Performance Computing and Communication (HPCCE 2021), 121620J (18 February 2022).
[40] Mohammad Derakhshan, Ali Naseri, Maryam Ghazizadeh, Reza Talebzadeh, Photonic Network Communications **36**, 338 (2018).
[41] Jayson K. Jayabharathan, G. Subhalakshmi, S. Robinson, Journal of Optical Communications **39**(3), 1 (2018).
[42] F. Parandin, M. M. Karkhanehchi, Superlattices and Microstructures **101**, 253 (2016).
[43] Ashkan Pashamehr, Mahdi Zavvari, Hamed Alipour-Banaei, Frontiers of Optoelectronics **9**(4), 578 (2015).
[44] D. J. Joannopoulos, G. Steven Johnson, N. J. Winn, R. D. Meade, Photonic Crystals: Modeling the Flow of Light, second ed., Princeton University Press, 2008.
[45] Kabilan Arunachalam, Susan Christina Xavier, Photonic Crystals - Introduction Applications and Theory, InTech Publishers, 2012.
[46] K. M. Ho, C. T. Chan, C. M. Soukoulis, Physical Review Letters **65**(25), 3152 (1990).
[47] K. Yee, IEEE Transactions on Antennas and Propagation **14**(3), 302 (1996).
[48] Nitish Kumar, Mohd Mansoor Khan, Ramesh Kumar Sonkar, Results in Optics **18**, 1 (2025).
[49] Fariborz Parandin, Salah I. Yahya, Mehdi Rezaeenia, Asghar Askarian, Saeed Roshani Sobhan Roshani, Yazeed Yasin Ghadi, Mohammad Behdad Jamshidi, Sahar Rezaee, Journal of Optical Communications **45**(s1), s2627 (2024).
[50] Yuhao Huang, Menghang Shi, Aodi Yu, Li Xia, Applied Optics **62**(3), 774 (2023).
[51] Fariborz Parandin, Saeed Olyaee, Farsad Heidari, Mohammad Soroosh, Ali Farmani, Hamed Saghaei, Rouhollah Karimzadeh, Mohammad Javad Maleki, Asghar Askarian, Zahra Rahimi, Arefe Ehyaee, Journal of Optical Communications **45**, 2589 (2024).

[52] S. S. Zamanian-Dehkordi, M. Soroosh, G. Akbarizadeh, Optical Review **25**(4), 523 (2018).
[53] Jing Chen, Farhad Mehdizadeh, Mohammad Soroosh, Hamed Alipour-Banaei, Optical and Quantum Electronics **53**(9), 510 (2021).
[54] Massoudi Radhouene, V. R. Balaji, Monia Najjar, S. Robinson, Vijay Janyani, M. Murugan, Optical and Quantum Electronics **53**, 1 (2021).

*Corresponding author: ramaprabhakrishna8@gmail.com