Improved electrical and photosensing properties of CuPc phtalocyanine/p-silicon diode by nanostructure

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The electrical and photovoltaic properties of metal/nanostructure CuPc phtalocynine organic layer /semiconductor diode have been investigated. The diode indicated a good rectifying behavior with non-linear behavior due to the organic and inorganic interfacial layers. The barrier height (0.77 eV) and ideality factor (1.99) of the studied diode is higher than that of conventional Al/p-Si Schottky diode. This indicates that barrier height could be increased by using CuPc phtalocynine organic layer on p-type silicon by changing the space charge region of p-type silicon. The photovoltaic parameters of the diode were found to be Voc=0.25 and J_{sc}=607.2 μA under AM1.5. The obtained results indicate that the barrier height of conventional Al/p-Si Schottky diode can be increased by organic modification and metal/nanostructure CuPc/semiconductor diode can be used for optoelectronic device applications as a photosensor.

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1. Introduction

The control mechanism of electrical characteristics of a Schottky diode is substantially based on its interface properties [1,2,3]. The contaminants formed during or after metallization of contact metals onto the surface and clean procedure may cause the interface states in the forbidden gap at metal/semiconductor interface which can effect the mechanical, electrical properties, performance, reliability and stability of metal–semiconductor (MS) devices [4-8]. Due to possessing a thin interfacial native oxide layer at metal/semiconductor interface, an ideal Schottky barrier diode (SBD) can never be acquired. The presence of such an insulating layer causes a deviation of electrical parameters of ideal diode to non ideal diode [3]. The deep and detailed studies on interface states are therefore so important for the comprehension of the electrical properties of SBDs. This might be overcome through formation of various layers that will present us an opportunity to observe its effect on electrical parameters. This layer can be obtained by oxidation like SiO_2 or formation of organic semiconductor films. In this study we have concentrated on the formation of the organic semiconductor film at metal/semiconductor interface. Organic semiconductor films have a wide application in electronic technology. The modification of the electrical properties of metal-semiconductors contacts is expected through the formation of an organic compound layer at the inorganic semiconductor/metal interface. It has been seen that barrier height of metal/organic compound/semiconductor structures could be either increased or decreased by using organic thin layer at metal/ inorganic semiconductor interface [9-13]. To see the effect of the interfacial layer at metal/semiconductor on the electrical properties of the diode, different interfacial layer should be stimulated for using by means of the choice of suitable organic semiconductor. In present study, the copper phtalocyanine (CuPc) organic semiconductor was chosen as an interfacial layer at metal/semiconductor interface due to its stability property. Our aim is to investigate the electrical and photovoltaic properties of Al/nanostructure CuPc /p-Si Schottky diode by the formation of CuPc organic semiconductor layer at metal/semiconductor interface using the forward-bias current-voltage (*I-V*), capacitance-frequency (*C-f*) and conductance-frequency (*G-f*) measurements. The *C-f* and *G-f* measurements give the important information about the interface state energy distribution of Au/nanostructure CuPc/p-Si Schottky diode. We used conductance method to obtain valuable information about the parameters of interface states of the device.

2. Experimental

The samples were prepared using mirror cleaned and polished (as received from the manufacturer) p-type Si wafers with (100) orientation and 5-10 Ω-cm resistivity.

The wafer was chemically cleaned using the RCA cleaning procedure [i.e., a 10 min boil in $NH_4OH+H_2O_2+6H_2O$ followed by a 10 min boil in $HCl+H_2O_2+6H_2O$]. The ohmic contact was made by evaporating Al on the back of the substrate in the vacuum system of 10^{-5} Torr, followed by a temperature treatment at 570 ^{o}C for 3 min in N_2 atmosphere. The native oxide on the front surface of the substrate was removed in $HF:H_2O$ (1:10) solution and finally the wafer was rinsed in de-ionised water for 30 s before forming organic layer on the p-type Si substrate. The organic layer is directly formed adding a CuPc solution in n-methylpyrrolidone on the front surface of p-type silicon substrate, and then waiting for the solvent to evaporate at room temperature. Al was evaporated through a shadow mask in the vacuum system of 10^{-5} Torr. In this way, an Al/nanostructure CuPc/p-Si Schottky diode was obtained. The area of circular Schottky contact was $3.14x10^{-2}$ cm^2. All metallic surfaces were cleaned by acetone and methanol before processes. The *I-V* and *C-V-f* measurements of the device were performed using KEITHLEY 4200 Semiconductor characterization system. The structural properties of CuPc deposited on p-type silicon were analyzed by a Park System XE 100E atomic force microscopy (AFM).

3. Results and discussion

3.1. Morphology of CuPc film and current-voltage characteristics of Al/nanostructureCuPc /p-Si Schottky diode

Fig.1 shows AFM image of CuPc deposited on p-type silicon. As seen in Fig.1, the CuPc film is consisted of CuPc nanoparticles with 65-130 nm. This suggests that the CuPc film is nanostructure organic material. The roughness of the CuPc film was found to be 26.88 nm.

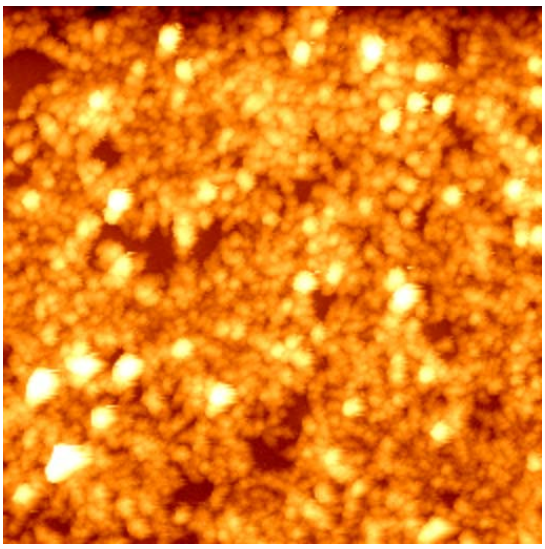

Fig.1 AFM image of CuPc deposited on p-type silicon

The current-voltage characteristics of Al/nanostructure CuPc/p-Si Schottky diode are shown in Fig. 2 and diode shows a good rectifying behavior. The current passing through a Schottky contact with series resistance is due to the thermionic emission and it can be expressed as [1],

$$I = I_o \exp\left(\frac{q(V - IR_s}{nkT}\right) \quad (1)$$

where V is applied voltage and the saturation current I_o is expressed as

$$I_o = AA^* T^2 \exp\left(-\frac{q\Phi_{b,o}}{kT}\right) \quad (2)$$

where q is the electron charge, A^* is the Richardson constant and equals to 32 A/cm^2K^2 for *p*-type Si [14], A is the diode area, T is the absolute temperature, k is the Boltzmann constant, n is the ideality factor, $\Phi_{b,o}$ is the zero bias barrier height. For values of V greater than $3kT/q$, the ideality factor from Eq (1) can be written as

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \quad (3)$$

Where n is a measure of the conformity of the diode to pure thermionic emission. The n value of the Al/nanostructure CuPc/p-Si Schottky diode was calculated using Eq. (3) from the linear region of the forward bias I-V plots (Fig. 2) and was found to be 1.99. This value indicates that the effect of the series resistance in the linear region is important. The value of the barrier height of the Al /nanostructure CuPc/p-Si Schottky diode was found to be 0.753 eV, from the y-axis intercepts of the semilog-forward bias *I-V* plots with the help of Eq. (3). The existence of interfacial layer and series resistance affects the ideality factor of the diode. The determination of ideality factor from I–V characteristics is only reliable if one can be confident that the current is determined by thermionic emission (TE) theory, because according to TE theory, forward current-voltage characteristic gives a good straight line and in turn, one obtains a reliable value of ideality factor.

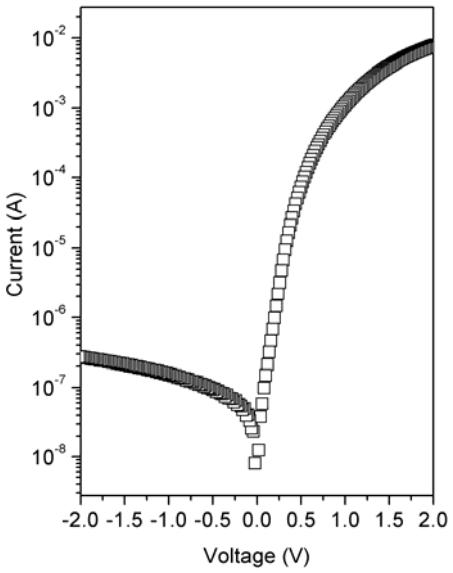

Fig.2 Forward and reverse bias current vs voltage characteristics of the Al/nanostructure CuPc film/p-Si structure at room temperature.

The barrier height (0.753 eV) and ideality factor (1.99) of the studied diode is higher than that of the Al/p-Si/copper phthalocyanine photodiode (0.71 eV and n=3.01) [15]. This indicates that the diode performance of Al/nanostructure CuPc film/p-Si Schottky diode is improved by the nanostructure of CuPC. The increase in barrier height with organic layer is due to the the energy level alignment of energy bands of the organic and inorganic semiconductors at interface of the junction. Furthermore, the realignments take place between the lowest unoccupied molecular orbital (LUMO), highest occupied molecular orbital (HOMO) of the organic semiconductor and work function of the metal. These realignments change the electron affinity of the semiconductor at the organic/inorganic semiconductor interface and in turn, the barrier height increases by modification of semiconductor surfaces by molecules. The presence of an organic layer at interface of the junction causes the non-ideal I–V behavior and this behavior was confirmed by obtained ideality factor higher than unity. The studies in literature have shown that **e**ffective Schottky barrier could be either increased or decreased by using organic thin layer on inorganic semiconductor [8-12,14]. It is evaluated that the interface between metal and p-Si semiconductor is passivated by using organic layer surface to reduce the interaction between metal and Si. Indeed, modification of semiconductor surfaces by molecules can lead to the changes in the electronic properties of the metal-semiconductor devices. The presence of an oxide film plus the organic CuPc layer at Al/p-Si interface causes the non-ideal I-V behavior. The CuPc organic layer increases the barrier height and the series resistance. The non-ideal behavior was analyzed by $I \propto V^m$ relation. For this, the I-V characteristics of the diode were plotted in double logarithmic scale. The plotted I-V curve shows two current regions. For the first and second regions, m values found to be 4.44 and 3.15, respectively. The obtained m values suggest that the current in the first region is controlled by trap-charge-limited conductivity mechanism (TCLC), suggesting that the higher voltages make a significant contribution to current-voltage characteristics. This confirms that the barrier height of the studied diode is increased by using CuPc phtalocyanine organic layer on p-type silicon by changing the space charge region of p-type silicon. But, in series resistance case, in order to determine the diode parameters, the various models can be used to determine the series resistance effect. The lower interface state density and the series resistance, the greater is the range over which lnI-V yields a straight line. In order to check effect of series resistance on I-V characteristics, we used Norde method given by the following relation [16],

$$F(V) = \frac{V_0}{\gamma} - \frac{kT}{q}\left(\frac{I(V)}{A^* A T^2}\right) \tag{6}$$

where γ is the integer greater than n. I(V) is the current obtained from the I–V characteristics. The plot of F(V) vs. voltage for the diode is shown in Fig.3. The (FV) gives a minimum point and thus, the barrier height is calculated by the relation,

$$\Phi_b = F(V_0) + \frac{V_0}{\gamma} - \frac{kT}{q} \tag{7}$$

Where$F(V_o)$ is the minimum point of F(V). The barrier height was found to be 0.777 eV. The series resistance is determined as

$$R_s = \frac{kT(\delta - n)}{qI_o} \tag{8}$$

The R_s value for the diode was determined using Eq.7 and was found to be 17.7 kΩ. This is considerable higher due to organic and oxide layers. This causes a non-linear region of forward bias I–V curve of the diode.

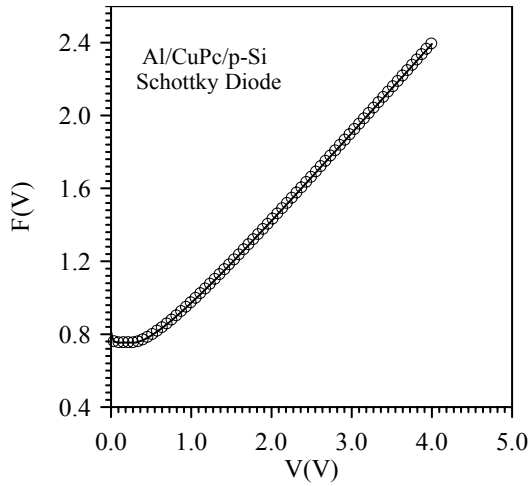

Fig.3 Plot of F(V)-V for Al/nanostructure CuPc film/p-Si structure

The obtained n value to be higher than unity may be attributed to the chemical structures of organic layer and native oxide layer on the semiconductor and series resistance.

We can evaluate that the value of ideality factor obtained for the diode studied is reliable because of the non-ideal behavior of the Al/nanostructure CuPc/p-Si Schottky diode. The ideality factor higher than unity results from several effects for examples, distribution of the interface states, tunnelling, recombination-generation and image force effect [19-20].

3.2 Interface state density properties of the Al/nanostructure CuPc/p-Si Schottky diode

Figs. 4-5 show the capacitance-frequency and conductance-frequency plots of Al/nanostructure CuPc film/p-Si Schottky diode at different bias voltages with step of 0.02 V. It can be seen very easily that the capacitance increases with decreasing frequency possibly caused by the continuous interface states distribution leading to a successive decrease of the response of the interface states to the applied alternating voltage [20-21]. Due to excess capacitance resulting from the interface states in equilibrium with the p-Si, the capacitance has higher values at lower frequencies. Being the capacitance not dispersive at higher frequency makes it not to have any contribution from the interface states in equilibrium with the semiconductor. This situation can be attributed to charges at the interface states not being able to follow the fast alternating current. For this reason, the total capacitance is equal to the sum of space-charge capacitance and interface capacitance at lower frequencies, in the other hand the total capacitance arises mostly from the space-charge capacitance at higher frequencies [22-23]. To analyze interface state properties of Al/nanostructure CuPc/p-Si Schottky diode, we have used the conductance technique described by Nicollian and Brews [24]. This method is the most accurate method to evaluate the density of interface states. In the method, the parallel conductance is measured as a function of frequency at a gate bias and it is expressed as [24],

$$\frac{G_p}{\omega} = \frac{qAD_{it}\tau_{it}}{2\omega\tau_{it}} \ln(1+\omega^2\tau_{it}^2) \tag{9}$$

Where D_{it} is the density of the interface states, q is the charge of the electron, ω is the angular frequency, τ is the time constant of the interface states. The relation between parallel conductance and measured capacitance-conductance is expressed as,

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{10}$$

The interface state density can be calculated by the following relation,

$$N_{ss} = \frac{(G/\omega)_{\max}}{0.402qA} \tag{11}$$

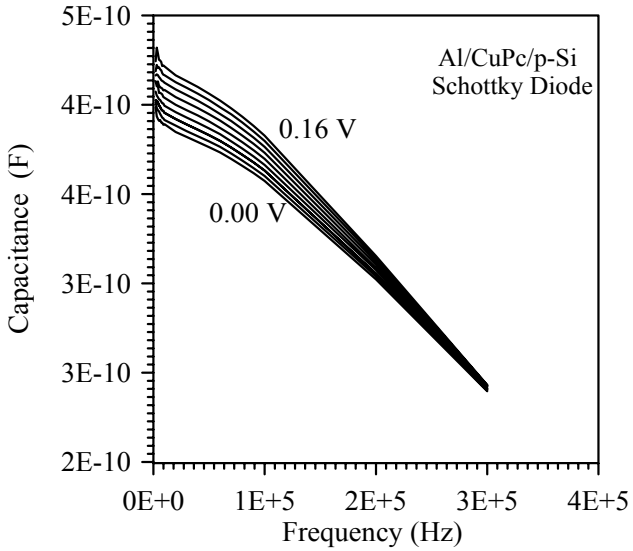

Fig.4 Experimental forward bias capacitance plot as a function of the frequency with bias voltage as a parameter of the Al/nanostructure CuPc film/p-Si structure (0.00 to 0.16 V with steps of 0.02 V) at room temperature.

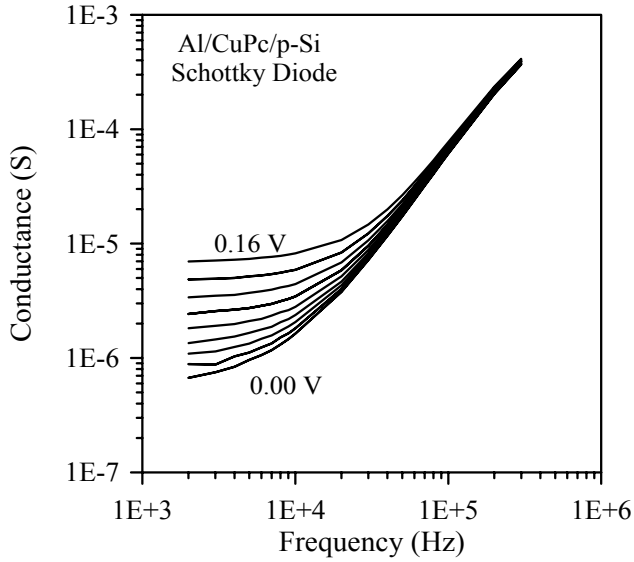

Fig.5 Experimental forward bias conductance plot as a function of the frequency with bias voltage as a parameter of the Al/nanostructure CuPc film/p-Si Schottky diode (0.00 to 0.16 V with steps of 0.02 V) at room temperature.

Fig.6 shows the plots of (G/ω) versus f of the diode at different voltages. The plots of G_p/ω-f indicate a peak. The origin of this peak is due to the presence of interface charges and these charges are present at interface of the silicon–oxide layer plus organic layer, which are contributing to the total charging current and in turn a peak

appears in G_p/ω-f plot [24]. The peak position shifts to higher frequencies with bias applied. This indicates that the traps are distributed inside the Si band gap. The plots of N_{ss} versus E_{ss}-E_v of the diode are shown in Fig. 7. The N_{ss} values change with E_{ss}-E_v values. The interface time constant of the diode increases with increasing E_{ss}-E_v values. It is evaluated that the chemical interaction between organic semiconductor and p-silicon gives new interface states. When a small alternating potential to the system swings in one direction, the electrons will be promoted from the interface states into unoccupied states in Si band and then demoted back to them as it swings in the other sense [24].

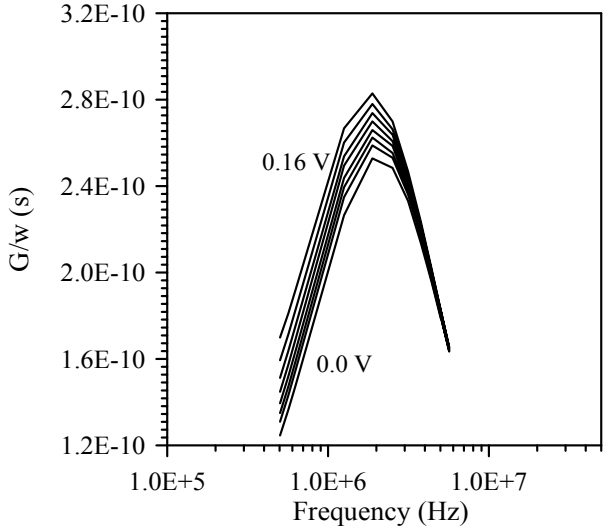

Fig.6 Plots of the G/ω-ω the Al/nanostructure CuPc film/p-Si Schottky diode

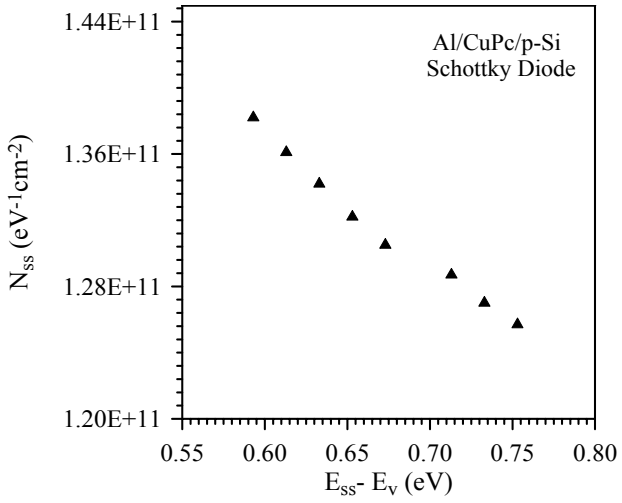

Fig.7 Energy distribution curves of the interface states and their time constants obtained from the experimental G_{ss}/w versus w characteristics for the Al/nanostructure CuPc film/p-Si structure at room temperature.

3.3. Photovoltaic properties of the Al/nanostructure CuPc/p-Si Schottky diode

The current-voltage characteristics of the Al/nanostructure CuPc/p-Si Schottky diode under different illuminations are shown in Fig.8. As seen in Fig.8, the reverse current of the diode increases strongly with illumination intensity and the diode shows a photovoltaic behavior with a maximum open circuit voltage V_{oc} and short-circuit current I_{sc}. The reverse current value at a given voltage for the diode under illumination is higher than that in the dark due to the generated charge carriers and these charges contributes photocurrent as a result of the light absorption. The magnitude of generation of photoelectrons depends on a difference in electron affinities between the p-Si and CuPC semiconductors. The best values of V_{oc} and J_{sc} of Al/nanostructure CuPc film/p-Si Schottky diode were found to be V_{oc}=0.25 and J_{sc}=607.2 μA under AM1.5, respectively. The obtained photovoltaic parameters of Al/nanostructure CuPc film/p-Si Schottky diode are higher than that of Al/p-Si/copper phthalocyanine photodiode [15]. These values suggest that the photovoltaic properties of the Al/nanostructure CuPc film/p-Si are improved by nanostructure. The fabricated Al/p-Si/copper phthalocyanine can be used for optoelectronic device applications as a photosensor.

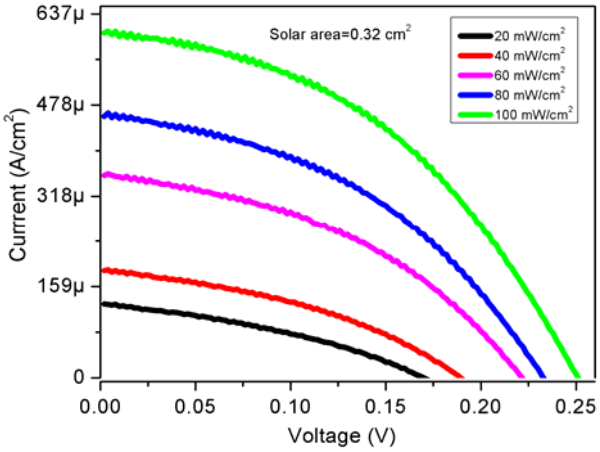

Fig.8 Photovoltaic characteristics of Al/CuPc/p-Si Schottky diode

4. Conclusions

The electrical and interface state density properties of the Al/nanostructure CuPc film/p-Si Schottky diode were investigated by current-voltage, capacitance-voltage and conductance-frequency methods. The ideality factor and barrier height of the Al/nanostructure CuPc film/p-Si Schottky diode are higher than that of Al/p-Si Schottky diode. The photovoltaic parameters of the Al/nanostructure CuPc/p-Si Schottky diode were found to be V_{oc}=0.25 and J_{sc}=607.2 μA under AM1.5. It is evaluated that the diode can be used in optoelectronic applications as a photodiode.

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