Investigation of interface states in Al/SiO_2/p-Si (MIS) structures with 50 and 826 Å SiO_2 interfacial layer using admittance spectroscopy method

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In order to achieve a better understanding of the effects of interface states (N_{ss}) and their relaxation time (τ),thickness of interfacial oxide layer (SiO_2) and series resistance (R_s) on the electrical characteristics, two type Al/SiO_2/p-Si (MIS) structures were fabricated with thin (50 Å) and thicker (826 Å) and they called as sample A and sample B, respectively. The energy density distribution profile of the N_{ss} and their τ and capture cross section (σ_p) of these structures have been investigated using admittance spectroscopy method which is concluding capacitance-voltage (C-V) and conductance-voltage (G/ω-V) in the wide frequency range of 10 kHz-1 MHz. The increase in capacitance especially at low frequencies and the peak behavior in G/ω-V plots in the depletion region can be attributed to the existence of N_{ss} located Si/SiO_2 interface and interfacial oxide layer. The values of N_{ss}, τ and σ_p changed from $9.55x10^{13}$ to $5.82x10^{13}$ $eV^{-1}cm^{-2}$, $6.31x10^{-6}$ to $1.58x10^{-6}$ s, and $3.55x10^{-21}$ to $1.27x10^{-15}$ cm^{-2} for sample A, $4.29x10^{13}$ to $3.36x10^{12}$ $eV^{-1}cm^{-2}$, $6.31x10^{-6}$ to $1.58x10^{-6}$ s, and $6.65x10^{-21}$ to $6.69x10^{-15}$ cm^{-2} for sample B, respectively. It is clear that the values of N_{ss} in sample A are almost one order higher than that in sample B. This indicate that a thick insulator layer at M/S interface can be considerably reduced the magnitude of N_{ss}. In addition, the measured C-V and G/ω-V characteristics of these devices were corrected as C_c-V and G_c/ω-V to eliminate the effect of R_s.

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Keywords: MIS structure, Admittance-spectroscopy method, Interfacial layer, Relaxation time and capture cross section

1. Introduction

Silicon is still dominating material in the electronic industry because of the excellent properties of its oxide and the Si/SiO_2 interface. Used in semiconductor technology, Si is a source amply found in nature; moreover, one another important characteristic of Si is that it allows the formation of a SiO_2 on the Si surface. Therefore, the growth of an oxide layer on the semiconductor is more important process step in the MIS or MOS device fabrications [1-8, 12]. The formation of ohmic contacts is also important because of the reaction between metal and semiconductors depending on the nature of the interfacial insulator layer, its thickness, and the specific metal used [9]. There are many studies on the properties at the interface between the Si and the thermally grown insulator/oxide in the literature in the last four decades [12, 11-17], but the non-ideal behaviour of C-V and G/ω-V characteristics have not clarified in detail yet. At high frequencies for accurate determination of the electron concentration the measurement data must be corrected the existence of R_s. When an insulator layer formed native or deposited at M/S interface, MS structure converts the MIS structure. Both the value of insulator layer thickness and Rs will alter the device characteristic. Low frequencies capacitances alone are not sufficient to characterize conduction mechanisms. However, the complete frequency-dependent admittance has to be analysed within a self-consistent model such as was used to characterize interface states in these structures. In order to determine energy density distribution profile of N_{ss}, there are several suggested methods in the literature such as high-low frequency capacitance [1-6], quasi-static capacitance [7], surface admittance [8] and conductance [9, 12] methods. Among them, Nicollian and Goetzberger conductance method [9, 12] is considered more accurate than the others. This method consists of measuring capacitance (C_m) together with conductance (G_m/ω) as a function of various parameters such as dc bias voltage, ac voltage modulation frequency. In addition, this method provides measurement of the interface states and their relaxation time (τ) and capture cross section (σ) over a specific energy range. The admittance method requires larger amount of data and analyses them more efficiently. The data required are: (i) low-frequency capacitance vs applied bias to get surface potential curve, (ii) C-V and G/ω-V curves at various frequency to get capacitance-frequency (C-f) and conductance-frequency (G/ω-f) curves at fixed voltages and (iii) parallel conductance (G_p/ω) vs f curves form C-f and G/ω-f data to get N_{ss}, τ and σ.

In general, the C-V and G/ω-V curves in ideal case are frequency independent and C-V curves show an increase in capacitance values with an increase in forward bias [9, 11-17]. The N_{ss} can be created by crystal lattice discontinuity (dangling bonds), inter-diffusion of atoms or the large density of crystal lattice defects at Si/SiO_2 interface. It is well known that the magnitude of the measured C and G/ω are related to interface states capacitance (C_{ss}) and conductance (G_{ss}/ω) and these values

are relatively high at low frequencies. Because, at low frequencies the charges at the interface can easily follow an ac signal so, the magnitude of N_{ss} increases with the decreasing frequency values.

A number of experimental studies were done in the recent years to observe the characteristics of interface states in MIS structures with different interfacial layer material such as SiO_2, SnO_2, Al_2O_3, ZrO_2, HfO_2 and organic layers [18-34]. When the insulator thickness was in the range of 40-60 Å, the direct current flowing across the MIS structures became considerable for large electric fields in the insulator [18]. As far as we know, a detailed investigation of the various features of interface states in these structures with interfacial layer thickness in the range of 50-826 Å has not been reported in the literature until now. Therefore, in this study, two type Al/SiO_2/p-Si (MIS) structures were fabricated with thin (50 Å) and thicker (826 Å) and they called as sample A and sample B, respectively. The energy density distribution profile of the N_{ss} and their τ and capture cross section (σ_p) of these structures have been investigated using admittance spectroscopy method in the wide frequency range of 10 kHz-1 MHz.

2. Experimental Procedure

The Al/SiO_2/p-Si (MIS) type structures were fabricated on the p-type (boron-doped) single crystal silicon wafer with (100) surface orientation, having thickness of 350 μm, 2" diameter and 1 Ω.cm resistivity. For the fabrication process, Si wafers were degreased in organic solutions of $CHClCCl_2$, CH_3COCH_3 and CH_3OH, then etched in a sequence of H_2SO_4 and H_2O_2, 20% HF, a solution of 6 HNO_3: 1HF: 35 H_2O, 20% HF and finally quenched in de-ionized water with resistivity of 18 MΩ.cm for 10 minutes. The oxidation procedure was carried in a resistance heated furnace in dry oxygen with a flow rate of 1.5 lt/min. The oxide layers thickness values of 50 Å and 826 Å were grown at the temperatures of 750 ^oC for 1.5 hours and 900 ^oC for 4 hours, respectively. Following oxidation, circular dots of 1.2 mm diameter high purity (99.999 %) Al with a thickness of ~2000 Å were deposited in order to form the rectifier contacts on the oxidized surface of the wafer through a Cu shadow mask in a liquid nitrogen trapped vacuum system with ~ $2x10^{-6}$ Torr vacuum pressure. Finally, Al with a thickness of ~2000 Å is also thermally evaporated on the whole back surface of the wafer after etching away the oxide layer (SiO_2) from the back surface in HF in order to form ohmic/back contacts. The thickness of metal layers and the deposition rates were monitored with the help of quartz crystal thickness monitor. In order to C-V and G/ω-V measurements, the electrical contacts are made on to the upper electrode on the oxide with the help of fine phosphor-bronze spring probe. The measurements were carried out at room temperature in electrically shielded metal box. The C-V and G/ω-V measurements have been performed using a computerized HP 4192A LF impedance analyzer (5 Hz-13 MHz).

The capacitance and conductance values as a function of the applied bias voltage have been measured at room temperature in the frequency range of 10 kHz -1 MHz, where small sinusoidal signal of 40 mV peak to peak from the external pulse generator is applied to the sample in order to meet the requirement [9,12]. All measurements were carried out with the help of a microcomputer through an IEEE-488 AC/DC converter card.

3. Results and discussions

Frequency dependent C-V and G/ω-V measurements of MIS or MOS type-structures can give us more detailed and accurate information about N_{ss} and their τ and σ in the energy band gap of semiconductor. There are several methods to obtain the energy dependent N_{ss} distribution profile [1-9,12]. Among them, the conductance method [9,12] yields more accurate and reliable results, especially when the density of N_{ss} is low as in the thermally grown oxidized systems. The density of states over most of the Si band gap in the oxidized systems is usually not much greater than 10^{13} $eV^{-1}cm^{-2}$ or smaller than 10^{10} $eV^{-1}cm^{-2}$ depending on the method of oxide layer preparation. This method can identify both bulk and interface defects when used on MIS or MOS structures, particularly when the structures are based in depletion, and superimposed ac signal is applied across the structure terminals [9,12,17]. The density of interface states can be obtained with subsequent calculation of the parallel conductance (G_p/ω) from measured capacitance and conductance values as a function of the frequency (f) for certain dc biases in depletion and weak inversion regions and suitable modeling. The lifetime of charges at interface, referred also as time constant or relaxation time (τ), can also be determined.

The C-V and G/ω-V measurements of samples A and B were performed in the frequency range of 10 kHz- 1 MHz at room temperature and are given in Figs. 1 (a,b) and 2 (a,b), respectively. As clearly shown in Figs. 1 (a) and 2 (a), the C-V measurements have three regimes of accumulation, depletion and inversion, verifying a typical MIS behaviour, for each ac frequency. Also it is clear that significantly larger frequency dispersion in C-V and G/ω-V curves, especially in the accumulation region, indicates the existence of the interface states in thermal equilibrium with the semiconductor and interface states cannot communicate with the metal. Such behaviour of the C-V plots at the intermediate region arises from a random distribution of surface charges. The fluctuating surface potential causes dispersion in the interface state time constants in the depletion regions. It is well known that when the C-V or G/ω-V measurements are carried out at low frequencies such that carrier lifetime (τ) is much lower than the period ($T=1/2\pi f$), the interface states can easily follow ac signal [12, 24-34] and yield an excess capacitance especially in the depletion region and at low frequencies.

As can be seen in Fig. 2 (b), the G/ω-V plots at various frequencies give a peak in the depletion region

because of the exchange of majority carriers in low quantity, between the localized interface states and the relevant band. The peak located at depletion region due to the N_{ss} contribution shifts from the low forward bias voltage to the high bias voltage as the frequency increases. Contrary to the low frequency values, the R_s become significant at high frequency values because of the low impedance of the capacitor. However, as can be seen in Fig 1 (b), G/ω-V plots at various frequency values do not show a clear peak in the depletion region. Such behaviour of G/ω-V plots can be attributed to the special density distribution of interface states at M/S interface and their relaxation time and the thickness of interfacial layer.

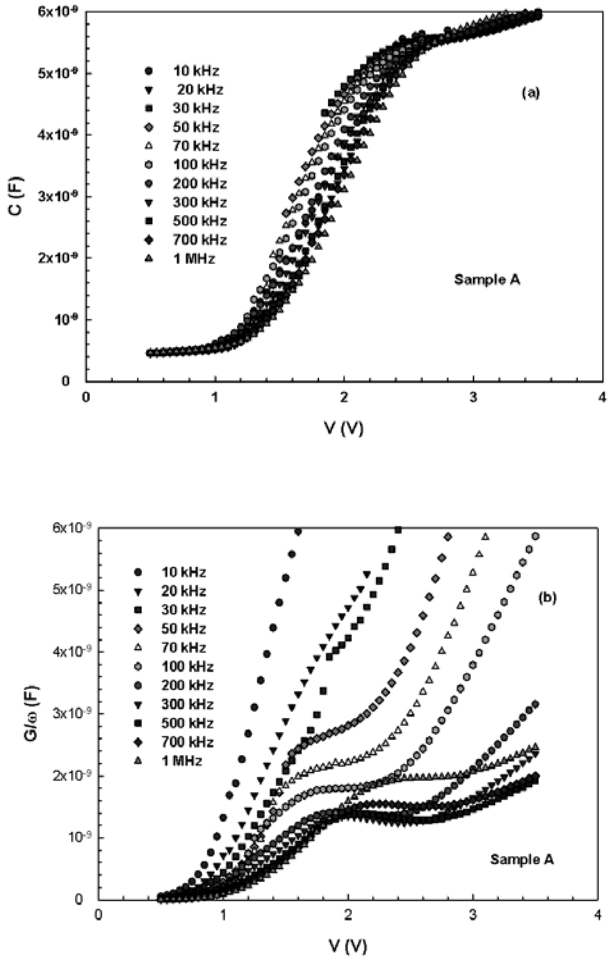

Fig. 1. The experimental values of (a) C-V and (b) G/ω-V plots of Al/SiO_2/p-Si structure with thin insulator layer (sample A) at various frequency values.

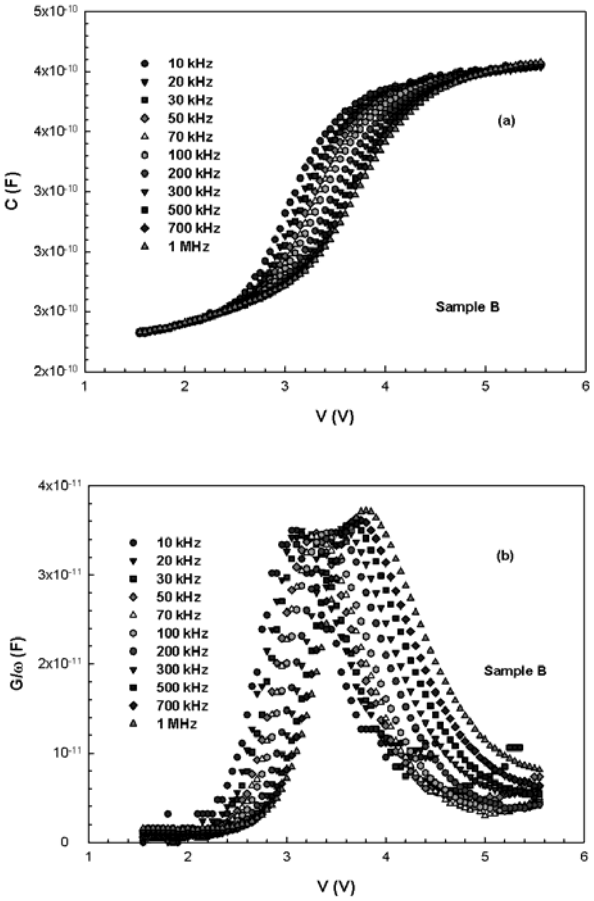

Fig 2. The experimental values of (a) C-V and (b) G/ω-V plots of Al/SiO_2/p-Si structure with thick insulator layer (sample B) at various frequency values.

The measured C and G/w values in the Figs. 1 (a,b) and 2 (a,b) were corrected in order to eliminate the series resistance (R_s) effect according to the equivalent circuit of the structures [9]. The real R_s of samples A and B were subtracted from the measured capacitance (C_{ma}) and conductance (G_{ma}) in the strong accumulation region. The corrected values of capacitance (C_c) and conductance (G_c/ω) for the samples A and B were determined from the following equations and the plots of C_c and G_c vs V at 1 MHz, for sample A, were given as an instance in Figs 3 (a) and (b), respectively.

$$C_c = \frac{\left[G_m^2 + (\omega C_m)^2\right] C_m}{a^2 + (\omega C_m)^2} \tag{1a}$$

$$G_c = \frac{[G_m^2 + (\omega C_m)^2)]\, a}{a^2 + (\omega C_m)^2} \tag{1b}$$

where $a = G_m - \left[G_m^2 + (\omega C_m)^2\right]R_s$, and C_m and G_m are the capacitance and the conductance values measured across the terminals of the Al/SiO_2/p-Si structure. As can be seen in Figs 3 (a) and (b), the series resistance is effective on the admittance-based measured methods (C-V and G/ω-V) characteristics, so the greatest error in the C and the G/ω occurs in the accumulation and depletion regions. However, in the inversion region there is no significant change in C and G/ω. In other words, in the inversion region there is a minor error in the C because C_c has become so small such that $(\omega R_s C_c)^2 << 1$. Therefore, R_s must be taking into account in calculations.

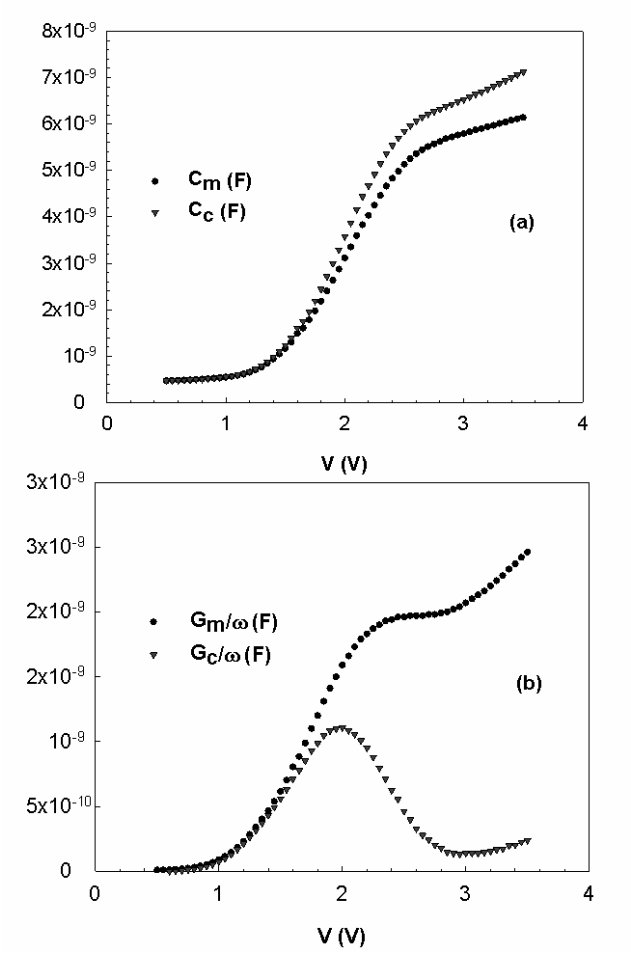

Fig 3. The corrected values of (a) C_c-V and (b) G_c/ω-V plots of Al/SiO_2/p-Si structure with thin insulator layer at 1 MHz.

In order to extract the values of the N_{ss}, we used conductance method [9,12]. The interface state admittance $Y_p (= 1/Z_p) = (G_p + j\omega C_p)$ and especially G_p / ω may be derived from the experimentally measured admittance $Y_m (= G_m + j\omega C_m)$, first by removing the contribution stemming from the insulator layer capacitance (C_{ox}) and the R_s according to the equivalent circuit of the Al/SiO_2/p-Si structure. According to the method of Nicollian and Goetzberger [9,12], the interface states conductance for MIS or MOS structures can be described as:

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 (G_m - \omega^2 C_m^2 R_s - R_s G_m^2)}{(\omega^2 C_{ox} R_s C_m - G_m)^2 + \omega^2 (C_{ox} - C_m - C_{ox} R_s G_m)^2} = \frac{qAN_{ss}}{2\omega\tau_p} \ln(1 + \omega^2 \tau_p^2) \quad (2)$$

with

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2}$$

and

$$C_{ox} = C_{ma}(1 + (G_{ma} / \omega C_{ma})^2) \quad (3)$$

angular frequency, τ is the time constant of the interface states which presents the characteristic time required to fill and empty the N_{ss} at various energy levels and it can be written as;

$$\tau = \frac{1}{\sigma v_{th} N_A} \exp(qV_d / kT) \quad (4)$$

Here, σ is the capture cross section of N_{ss}, v_{th} is the thermal velocity of carrier, N_A is the doping concentration and A is the rectifier contact area. In a p-type semiconductor, the energy position of N_{ss} with respect to the top of valance band and the surface of the semiconductor was calculated as:

$$E_{ss} - E_v = q(\varphi_s - E_F) \quad (5)$$

where E_F is the position of Fermi energy level [$E_F = \frac{kT}{q} \ln(N_V / N_A)$]. The surface potential as a function of applied bias voltage was found from the numerical integration of the lowest measurable frequency capacitance-voltage curve according to following equation as [25]:

$$\bar{\varphi}_s = \int_{V_a}^{V_G} \left(1 - \frac{C_{LF}}{C_{ox}}\right) dV_G + \varphi^* \quad (6)$$

where V_a is the bias voltage in strong accumulation when the capacitance is equal to the oxide capacitance C_{ox} and the integration constant φ* was found by extrapolating the C_{sc}^{-2}- φ_s curve in the depletion region to $C_{sc}^{-2} = 0$ [12, 25]. Surface potential vs. applied bias voltage plots for the samples A and B are shown in Fig 4.

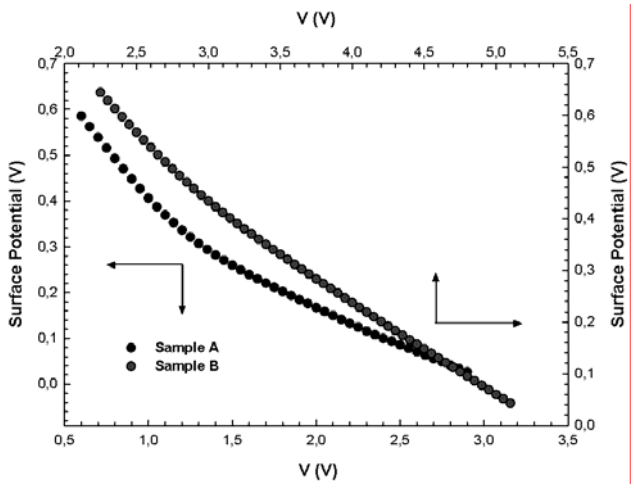

Fig 4. The surface potential vs V plot of the Al/SiO$_2$/p-Si structures at room temperature

The derived G_p/ω vs dc gate voltage and frequency plots are given in Fig 5 and 6 respectively.

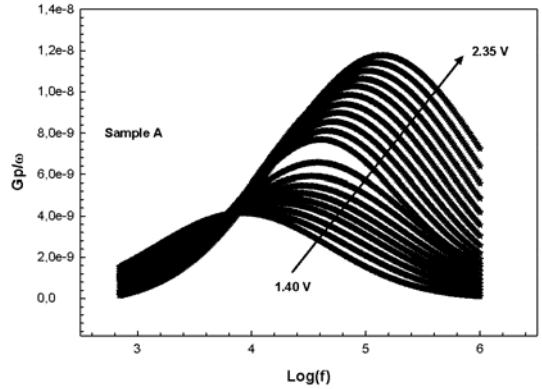

Fig 5. The equivalent parallel conductance G_p/ω vs frequency at various gate biases for the Al/SiO$_2$/p-Si structure at room temperature for sample A.

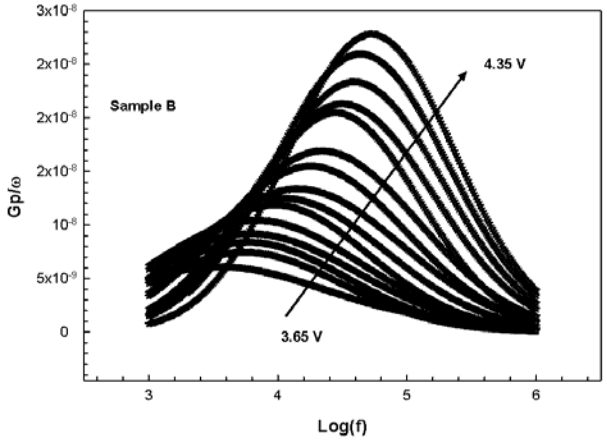

Fig 6. The equivalent parallel conductance G_p/ω vs frequency at various gate biases for the Al/SiO$_2$/p-Si structure at room temperature for sample B.

Figs 5 and 6 show a series of G_p/ω vs. log(f) characteristics measured at various applied bias voltages in the depletion region from Eq 2. All of the G_p/ω vs log(f) plots for various bias voltages give a peak and the magnitude of the peaks increase with the increasing applied bias voltage and the peak positions shift towards to high frequency region. Such behavior of G_p/ω vs log(f) can be explained with the existence of an almost continuous distribution of interface state energy levels. The localized electronic states around the SiO_2/Si interface should be distributed throughout the insulator energy band gap. For the peak values (Figs. 5 and 6), $d(G_p/\omega)/d(\omega\tau)$ is equal to 0 and this case represent maximum through which we calculated $\omega\tau$ as 1.98. Substituting these values in the above Eq. 2 one gets $N_{ss} = (G_p/\omega)_{max.}/(0.402qA)$ and $\tau=1.98/\omega_p$. The ordinates and frequencies of the maxima, therefore, yield N_{ss} and τ. Then, the dependency of N_{ss} and τ on the bias was converted to a function of energy (E_{ss}-E_v) using Eq. (5). The values of N_{ss} and their relaxation time for samples A and B were shown in Figs. 7 (a) and (b).

It is observed that both interface state density N_{ss} and their time constant τ for the samples A and B show an increase with an increase in energy and from the bottom to the valance band toward the mid-gap of Si. In addition, the capture cross-section of hole (σ_p) can be expressed as

$$\sigma_p = \frac{1}{(v_{th}\tau n_i)}\exp(-q\varphi_i/kT) \qquad (7)$$

where v_{th} is the thermal velocity of carriers (= 10^7 cm/s at room temperature), n_i is the intrinsic carrier concentration in Si ($1.55\text{x}10^{10}$ cm^{-3}), φ_s is the interface potential corresponding to bias at which G_p/ω shows a peak and T is temperature in K (300 K). The dependency of σ_p as a function of interface energy is shown in Fig. 8. As can be seen in Fig. 8, the values of σ_p decrease with energy towards the mid-gap and they were found to be $3.55\text{x}10^{-21}$ cm^2 at (0.397-E_v) and $1.27\text{x}10^{-15}$ cm^2 at (0.157-E_v), $6.65\text{x}10^{-21}$ cm^2 at (0.381-E_v) and $6.69\text{x}10^{-16}$ cm^2 at (0.173-E_v) for samples A and B, respectively. Similar results have been reported in the literature [14, 26-34].

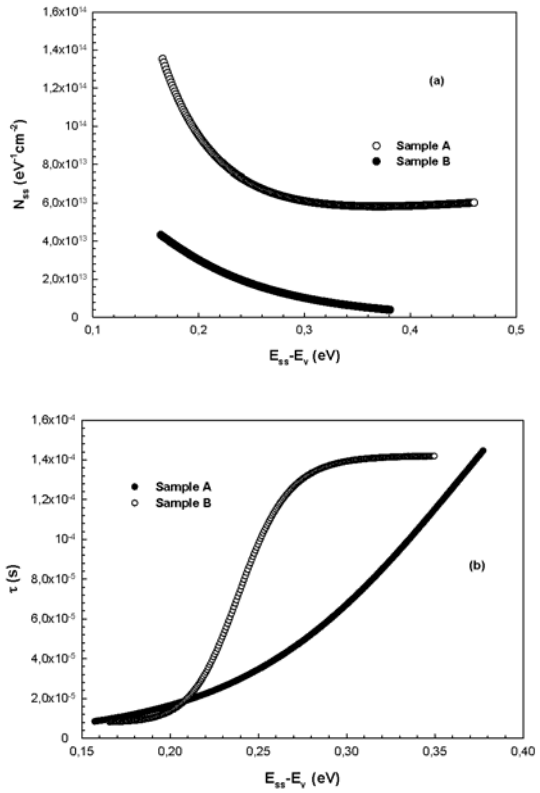

Fig 7. (a) The energy distribution profiles of interface states and (b) their time constants obtained from conductance method for the Al/SiO_2/p-Si structures at room temperature.

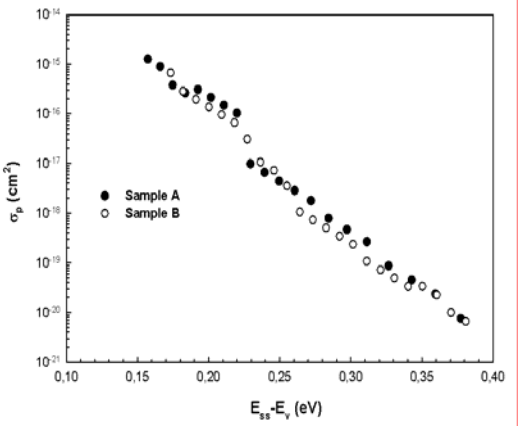

Fig 8. The hole capture cross sections as function of energy obtained from conductance method for the Al/SiO_2/p-Si structures at room temperature.

3. Conclusions

In this study, to achieve a better understanding of the effects of N_{ss} and their τ, interfacial oxide layer (SiO_2) thickness and Rs on the C-V and G/w-V characteristics two type Al/SiO_2/p-Si (MIS) structures were fabricated with thin (50 Å) and thicker (826 Å) interfacial layer and they called as sample A and sample B, respectively. The energy density distribution profile of the N_{ss} and their τ and capture cross section (σ_p) of these structures were obtained from the admittance spectroscopy method in the wide frequency range of 1 kHz-1 MHz at room temperature. The decrease in capacitance with frequency and the peak behavior in G/w-V plots in the depletion region was attributed to the existence of N_{ss} located Si/SiO_2 interface and interfacial oxide layer. The experimental values of N_{ss}, τ and σ_p changed from $9.55x10^{13}$ to $5.82x10^{13}$ $eV^{-1}cm^{-2}$, $6.31x10^{-6}$ to $1.58x10^{-6}$ s, and $3.55x10^{-21}$ to $1.27x10^{-15}$ cm^{-2} for sample A, $4.29x10^{13}$ to $3.36x10^{12}$ $eV^{-1}cm^{-2}$, $6.31x10^{-6}$ to $1.58x10^{-6}$ s, and $6.65x10^{-21}$ to $6.69x10^{-15}$ cm^{-2} for sample B at room temperature, respectively. These results show that the values of N_{ss} in sample A are almost one order higher than that in sample B. Thus, a thick insulator layer at M/S interface can be considerably reduced the magnitude of N_{ss}. In addition, the measured C and G/ω values for two type diodes were corrected by taking into account the R_s. In conclusion, the interfacial oxide layer and its thickness and homogeneity are important parameters on the diode performance.

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