Isothermal annealing time effects on dielectric parameters of Au/SnO_2/n-Si/Al structure

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This work examines some electrical parameters of metal/oxide/semiconductor devices (Au/SnO_2/n-Si/Al). For this purpose, SnO_2 thin films were deposited via spin coating process on n-type silicon wafer with the orientation of (100). Four samples were fabricated with different isothermal annealing time. Dielectric parameters of dielectric loss (ε''), dielectric constant (ε'), dc conductivity (σ_{dc}) and dielectric loss tangent (tan δ) of Au/SnO_2/n-Si/Al devices were investigated as a function of thermal annealing time using capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) measurements at a frequency of 1MHz in the dark and at room temperature. The dielectric constant was found to lie between 7.00 and 11.96. The dielectric properties of metal/oxide/semiconductor structures have been determined to be seriously impacted by the thermal annealing time. The values of dielectric parameters showed a strong dependence on the applied voltage. In addition, the dielectrical data has been analyzed considering electric modulus formalism. Using electric modulus and complex permittivity the experimental data were analyzed. AFM images show that intensive thin films of SnO_2 were obtained by spin coating. Experimental results show that the isothermal annealing time is an effective way to increase the dielectric constant and to decrease the dielectric loss of electronically devices such as Au/SnO_2/n-Si diodes.

(Received February 25, 2014; accepted September 11, 2014)

Keywords: Thin films, SnO_2, dielectric, Spin coating

1. Introduction

The metal–semiconductor (MS) contact, also called Schottky, is one of the most widely used rectifying contacts in device technology. These diodes are the principle of a major number of electronic devices, such as solar cells, photo detectors, field effect transistors and microwave diodes [1–4]. The existence of an oxide layer (e.g. SiO_2, Si_3N_4 or SnO_2) transforms the MS diode to a metal–oxide–semiconductor (MOS) diode [5–7]. The MOS structures constitute a type of capacitor which stores the electric charge by impact of the dielectric property of insulator or oxide layers. Given the importance of Si technology, the insulator-semiconductor interface and defects on its neighborhood have been extensively studied [8-19]. The oxide layer may have a strong influence on the diode characteristics as well as a change of the interface state charge with bias which will give rise to an additional field in the interfacial layer [7].

In various fields of technology and materials science, it is useful to search for alternative metal oxide films (such as ITO, SnO_2) to improve optical applications and some detector (such as gas detectors) systems. Because of their features and potential applications, tin oxide films have been one of the most important metal oxides for a wide variety of novel and special applications [5-6,20-27]. SnO_2 films are appealing for utilize in the fabricating of gas sensors [22,24-25], flat panel displays [26], and solar cells [27]. These films can be fabricated by different methods such as evaporation [28], sonochemical [29], sol–gel [30-31], sputtering [32], spin coating [33], chemical vapor deposition (CVD) [34-35] and spray deposition [36]. Due to the simplicity of operation, and uniformity and thinness of coated layers, spin coating has been used in this work to develop SnO_2 films on n-Si devices.

If a silicon substrate covered with tin oxide film, it is recommended that this form behaves like a Schottky contact [5-6,23]. It seems that the tin oxide acts a more important role than serving as a contact and is likely to effect the various parameters as a dielectric layer. This dielectric layer cannot only prevent inter-diffusion between metal and semiconductor substrate, but also reduce the electric field drop issue in metal/oxide/semiconductor structures.

The main aim of this work was to obtain some electrically properties of the Au/SnO_2/n-Si/Al devices and determine the relationship between the isothermal annealing time using capacitance–voltage and conductance–voltage techniques. Starting from this, the dielectric properties of the thin films are studied as a function of isothermal annealing time and reported dielectric enhancement in SnO_2 thin films prepared on n-Si substrates. Due to scarce of the publications about the dielectrically properties of SnO_2/n-Si structures, the outcome of the work are waited to be useful in predicting the behavior of metal-oxide-semiconductor based devices

with improved dielectric properties. Because, the dielectric loss and dielectric constant are the significant parameters in the choice of materials for device application.

2. Results and discussion

2.1 Experimental procedure

The n-type single crystal Si (100) wafer with 1-10 Ω-cm resistivity and thickness of 280μm was used as starting materials. The producing process of $Au/SnO_2/n\text{-}Si/Al$ devices first began with cleaning of the Si wafers. Therefore silicon wafer was degreased for 10 minutes in boiling trichloroethylene and acetone consecutively and then immersed in methanol. The oxidizing process was started using a solution of H_2O: 27%NH_4OH: 30%H_2O_2 (5:1:1) to remove organic residues from the silicon surface. This process utilizes the organic residues on silicon surface to create an oxide layer. Finally, a solution of 49% hydrofluoric acid: water (1:10) was used to remove local oxide layer from silicon surface. The Si crystal was rinsed in deionized water by using a conventional ultrasonic cleaner and then dried in N_2 atmosphere. After chemical cleaning, ohmic contact of thickness 600 Å was formed immediately by thermal evaporation of high-purity aluminum on the back side of n-Si wafers. In order to obtain a low resistivity ohmic contact, wafer was annealed at 600 ^oC for 5 min in high purity nitrogen atmosphere. The native oxide on the front surface was removed using the solution of 49%HF: H_2O (1:10) before forming an oxide layer on n-Si wafer. The tin oxide film to the front surface of the n-Si wafer was formed using the solution consist of 32.21wt% of C_2H_5OH, 40.35wt% of H_2O and 27.44wt% $SnCl_4.5H_2O$ by a spin coating method at a spinning rate of 1200 rpm for 30s at room temperature. After formation of the film, wafer was then placed a furnace at 300 ^oC for 30s to produce as-processed $SnO_2/n\text{-}Si/Al$ structures. Before isothermal annealing process, the wafer was cut into four pieces. One of them was as processed sample. The others of wafer were annealed at the temperature of 500 ^oC for 60, 180 and 300 minutes, respectively. After isothermal annealing process, high-purity gold circular dots with a diameter of 1.5 mm and thickness of 600 Å was formed by evaporating at a pressure of 10^{-6} Torr through a metal shadow mask onto the SnO_2 surface to produce Schottky rectifiers. The deposition rate of 5–10Å/s and the thickness for both Au and Al were observed with the help of a FTM6 thickness monitor. Typical schematic representation of the $Au/SnO_2/n\text{-}Si/Al$ diodes is shown in Fig. 1. Electrical measurements were carried out at room temperature and dark environment by using computer controlled HP 4192A LF impedance analyzer for capacitance-voltage (*C-V*) and conductance-voltage (*G-V*). Atomic force microscopy (AFM) measurements were performed in order to study the effect of the isothermal annealing time on the SnO_2 layer.

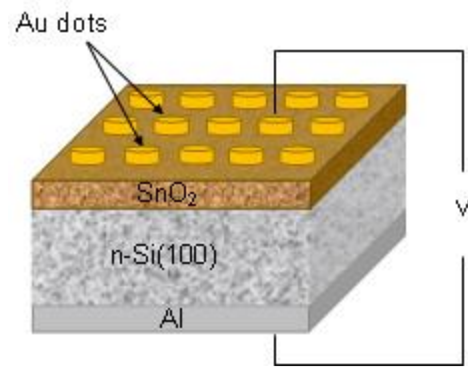

Fig 1. Schematic view of $Au/SnO_2/n\text{-}Si/Al$ Schottky diodes.

2.2 Dielectric spectroscopy

A sample is defined by a complex dielectric constant (ε^*) in an alternating electric field [37]:

$$\varepsilon^* = \varepsilon' - i\varepsilon'' \tag{1}$$

where ε' is the real dielectric constant and ε'' is the imaginary dielectric constant. The *i* is the imaginary root of (-1). The real dielectric constant indicates the capacitive conduct or polarizability of material, while the imaginary dielectric constant indicates the energy losses due to conduction and polarization [38-39]. In accumulation mode, the electrical properties of metal/oxide/semiconductor devices define basically dielectric properties of the oxide at high frequencies. For this reason the real dielectric constant of the SnO_2 film was determined from the accumulation capacitance. The dielectric properties of $Au/SnO_2/n\text{-}Si/Al$ diodes were determined from capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) measurements at a frequency of 1MHz and at room temperature and dark environment. The reduction of impact of interface states (N_{ss}) can be done when the capacitance and conductance curves according to voltage are obtained at adequately high-frequency [6,7], since the charges at the N_{ss} cannot follow an ac signal. This makes the contribution of N_{ss} capacitance to the total capacitance negligibly small [13,17]. The real part of the dielectric constant (ε') was calculated using the measurement capacitance values at the strong accumulation region from the relations [40],

$$\varepsilon' = \frac{C_i}{C_o} \tag{2}$$

and

$$C_o = \varepsilon_o \frac{A}{d_i} \tag{3}$$

where C_i is the maximal capacitance of the structure corresponds to the insulator capacitance ($C_i = \varepsilon_i \varepsilon_o A/d_i$) in strong accumulation region. C_o is the capacity of free space, *A* is the area of the sample, d_i is

the interfacial layer thickness (258 nm) determined from *C–V* data (1 MHz) in accumulation and ε_o is the permittivity of free space (ε_o = 8.854x10^{-14} F/cm). The isothermal annealing time changes in the computed ε' are given in Fig. 2 as a function of applied voltage. It can be seen that ε' remains almost invariant up to 0.2V after which the rate of increase becomes faster and reaches a maximum value and then shows an annealing dispersion in the accumulation region for all samples. As can be seen in Fig. 2, the ε' values have been calculated to be strongly voltage dependent. This result shows that four feasible mechanisms may be contribute to the dielectric behavior of metal/oxide/semiconductor structures; dipole-orientation, charge carriers, electrode interface and ac conductivity [41].

In addition, in the absence of applied voltage, the charge carriers that are bounded at different localized states show different dipole orientations. When a voltage applied to the gate an electron can hop between these localized centers and cause reorientation of an electric dipole. This case gives rise in the dielectric constant. From the figure, as the applied voltage increases toward high (to 2V), the magnitude of dielectric constant is slightly reduced. It is also observed that the dielectric constant increases with increasing thermal annealing time. The calculated dielectric constant value of as-processed diode is lower than the annealed diodes. In other words, the annealing process has increased the dielectric constant of diodes. This is presumably related with the effect of an inhomogeneity of Si/SnO_2 structure coming from structural defects. In addition, the increase in the value of the dielectric constant obtained for annealing time up to 300 min is due to an increase of total polarization arising from dipoles and trapped charge carriers. The ε' have values of 6.97, 9.50, 10.25 and 11.44 at +1V for the samples as-processed, 60, 180 and 300 min annealed, respectively.

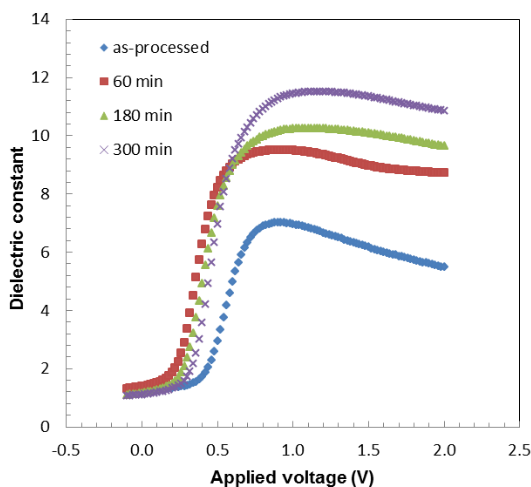

Fig 2. Voltage dependence of the dielectric constant for all the specimens: as-processed, 60, 180 and 300 min.

The imaginary dielectric constant shows the energy losses ε'' due to polarization and conduction and was determined by the values of conductance at accumulation region from the relation [40],

$$\varepsilon'' = \frac{d_i}{A\varepsilon_o} \frac{G_{ma}}{w} \tag{4}$$

where *w* is the angular frequency and G_{ma} is the conductance of metal/oxide/semiconductor structure at any strong accumulation region. Fig. 3 depicts the isothermal annealing time changes in the calculated ε'' as a function of applied voltage. From the figure, ε'' remains almost invariant up to 0.2V for all samples and then shows an annealing dispersion in the accumulation region. The dispersion observed in the dielectric loss ε'' for as-processed sample is quite high as compared to the thermal annealed ones. For thermal annealed samples, the reactions of the grains cause the small dispersion of curves. On the other hand, free charges and neutral dominates can cause

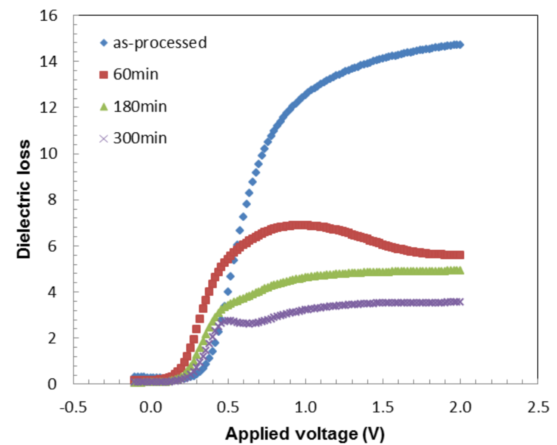

Fig 3. Voltage dependence of the dielectric loss for all the specimens: as-processed, 60, 180 and 300 min.

more dispersion for as-processed sample. It can be also seen from Fig. 3 that dielectric loss decreases with increasing thermal annealing time. The ε'' has values of 12.53, 6.88, 4.61 and 3.21 at +1V for the samples as-processed, 60, 180 and 300 min annealed, respectively.

The dissipation factor (dielectric loss tangent, tanδ) was obtained from the relation [40,42],

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} \tag{5}$$

The variation of the tan δ vs. voltage is given in Fig. 4 before and after isothermal annealing time. In Fig. 4, a significant variation with applied voltage was observed (especially in the voltage range of 0.6 to 2V) for sample as-processed. It is evident that tan δ is in close relation with the conductivity. The increase of the conductivity (as

seen in Fig. 5) with increasing of applied voltage is accompanied by an increase of the eddy current, which in turn increases the energy loss tanδ [43]. The change of annealing time has effects on the values (decreasing of tan δ values with increasing thermal annealing time) and peak positions of these curves. It can be seen from Fig. 4 that the dielectric loss tangent values almost unchanged as the voltage increases from 0.6 to 2V for thermal annealed samples. From these plots, it can be also seen that a small decrease in peak height and a shifting of peak position toward higher voltage with the rise in annealing time. The tan δ peak values are 0.71 (at 0.30V), 0.58 (at 0.34V) and 0.55 (at 0.38V) for annealed samples of 60, 180 and 300 min, respectively.

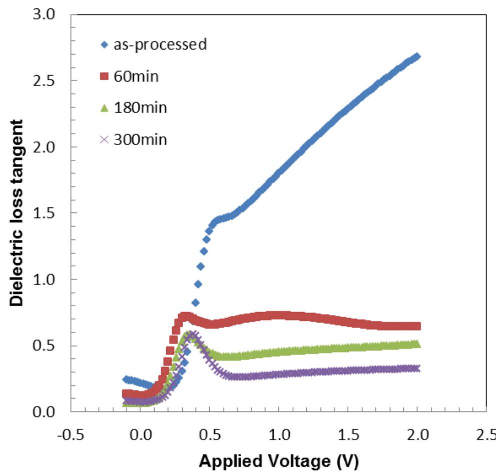

Fig 4. Voltage dependence of the dielectric loss tangent (tan δ) for all the specimens: as-processed, 60, 180 and 300 min.

The dc conductivity (σ_{dc}) of the samples was obtained by the following formula

$$\sigma_{dc} = \frac{G_{ma} d_i}{A} \quad (6)$$

where G_{ma} is the measured conductance values. Fig. 5 illustrates the behavior of σ_{dc} with voltage for various annealing times. According to Fig. 5, the σ_{dc} values showed a powerful dependence on the applied voltage. It is shown from Fig. 5 that σ_{dc} remains almost invariant up to 0.2V for all samples and then increases with the applied voltages. At room temperature, σ_{dc} against voltage curves showed strongly decrease with annealing time. The σ_{dc} have values of 6.97, 3.83, 2.57 and 1.78x10^{-6} Scm^{-1} at +1V for the samples as-processed, 60, 180 and 300 min annealed, respectively. The decrease of σ_{dc} leads to a decrease of the eddy current. This behavior can be attributed to a gradual increase in series resistance with increasing temperature.

The dielectric mechanism of materials can be expressed, to extract as much information as possible, using different representations such as electric modulus, inverse complex permittivity or complex modulus, M^*.

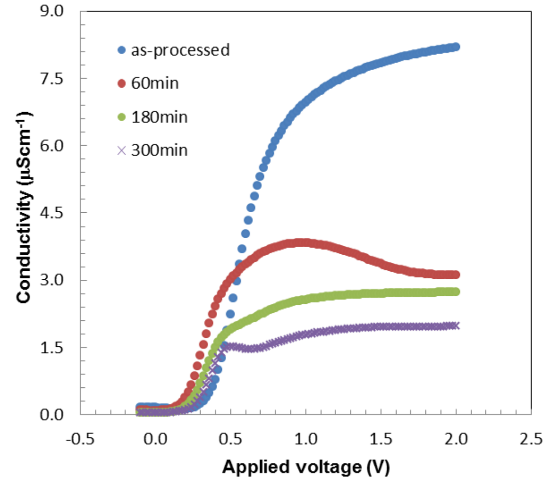

Fig 5. Voltage dependence of dc conductivity for all the specimens: as-processed, 60, 180 and 300 min.

These representations allow us to allocate the local dielectric relaxation from long-range electrical conductivity. The dipole-reorientation spectroscopy data are analyzed using M^* formalism reported by Macedo et al. [44]. The M^* is given by

$$M^* = M' + iM'' \quad (7)$$

where i is the imaginary root of $(-1)^{1/2}$. M' and M'' are the real and imaginary part of electric modulus and given by

$$M' = \frac{\varepsilon'}{\varepsilon'^2 + \varepsilon''^2} \quad (8)$$

and

$$M'' = \frac{\varepsilon''}{\varepsilon'^2 + \varepsilon''^2} \quad (9)$$

The complex modulus expression has been reported by different authors [45-47]. Fig. 6(a) and (b) show the voltage dependence of the M' and M'' before and after annealing. It is seen from Fig. 6(a), the M' versus voltage curves have several maxima under applied voltage. The M' has values of 0.73, 0.71, 0.85 and 0.90 at 0V for the samples as-processed, 60, 180 and 300 min annealed, respectively. It can be also seen from Fig. 6(a) that M' first decreases with increasing applied voltage at all annealing times and then stays actually constant as the voltage increases between 0.5 and 2V. From Fig. 6(b) it is known that the M'' first decrease continually as the voltage

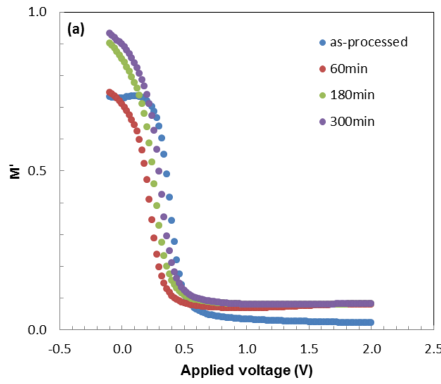

Fig 6. Plot of electric modulus (M^*) versus applied voltage for all the specimens: as-processed, 60, 180 and 300 min. (a) real part of electric modulus and (b) imaginary part of electric modulus.

increases between -0.1 and 0.1V, second increase as the voltage increases between 0.1 and 0.5V, third achieves a peak value, fourth decrease continuously up to 0.6V and then stays actually constant as the voltage increases between 0.6 and 2 V at all isothermal annealing times.
Three-dimensional surface morphology of SnO_2 thin films grown on n-type silicon substrates for the specimens of as-processed, 60, 180 and 300 min annealed are presented in Fig. 7(a) - (d) using AFM over a 10×10 μm^2 area on the film surface. The images show that intensive thin films of SnO_2 were obtained by spin coating. The root-mean-square surface roughness (R_{MS}) and arithmetic mean surface roughness (R_a) are good parameters to give an idea about the quality of the surface. The values of R_{MS} and R_a have been determined by using AFM images in Fig. 7(a) - (d) and given in Table 1. As shown in Table 1, the R_{MS} values of as-processed SnO_2 thin film is about 4.20 nm and it decreases to about 0.19 nm after thermal annealing. The arithmetic mean surface roughness (R_a) of as-processed SnO_2 thin film is about 1.24 nm and it decreases to about 0.13 nm after thermal annealing. From the values obtained, a reduction in surface roughness is observed by annealing. We concluded that the annealing process is an important parameter that could influence the surface roughness behavior

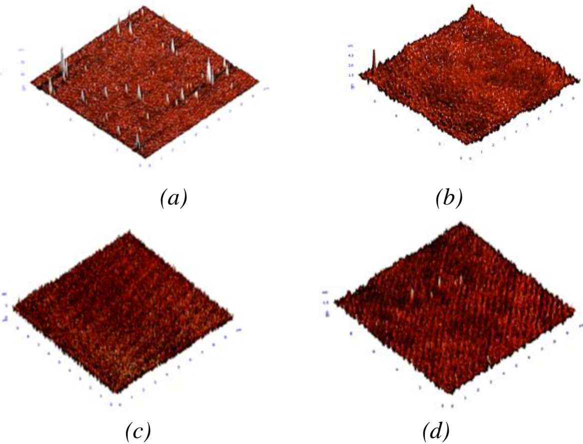

Fig 7. The AFM images (10×10 μm) of SnO_2 thin films grown on n-type silicon substrates for the specimens: (a) as-processed, (b) 60 min, (c) 180 min and (d) 300 min.

Table 1. The root-mean-square surface roughness (R_{MS}) and the arithmetic mean surface roughness (Ra) values calculated using AFM images shown in Fig. 7(a)-(d) for Au/SnO_2/n-Si/Al diodes.

Samples	R_{MS}(nm)	Ra(nm)
as-processed	4.20	1.24
60 min	0.22	0.28
180 min	0.28	0.23
300 min	0.19	0.13

The values obtained for ε' are shown as a function of isothermal annealing time in Fig. 8. We found that ε' is strongly dependent on the annealing time. The initial value of dielectric constant (7.00ε_o [5-6,48]) of oxide layer for as-processed sample has increased with thermal annealing to 11.44ε_o. The voltage values of the samples are 0.98, 0.87, 1.05 and 1.12V for as-processed, 60, 180 and 300 min, respectively.

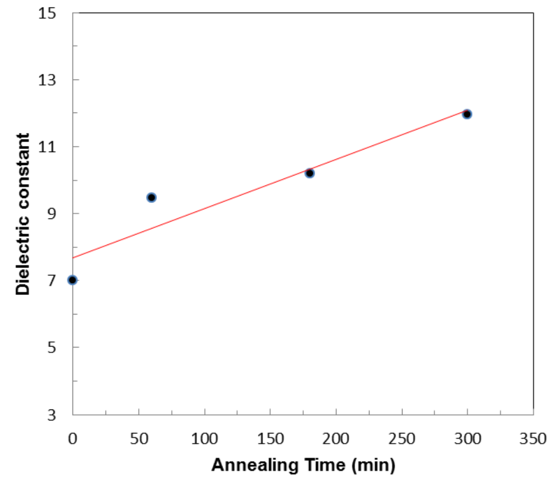

Fig 8. Variation of dielectric constant with isothermal annealing time.

Consequently, the isothermal annealing is a powerful way to increase the dielectric constant of oxide of the devices made from Au/SnO_2/n-Si/Al structures. These devices may be attractive to have a high dielectric tunability in a certain applied voltage range and low dielectric loss. High dielectric constant is important when a good capacitive coupling is required in the case of metal/oxide/semiconductor devices such as filters, tunable oscillators and phase shifters [49].

The annealing time dependence of ε'' for Au/SnO_2/n-Si/Al diodes is shown in Fig. 9. It is clearly seen in Fig. 9, dielectric loss decreased monotonically with increasing thermal annealing time from 0 to 300 min. Therefore, it is suggested that the dielectric loss is strongly dependent on the quality (improving with annealing process after fabrication) of SnO_2 films. In addition, impurities in the SnO_2 films may also be affected the dielectric loss. From the figure, the values of ε'' are changed from 11.39 to 3.29 with increasing of annealing time. Consequently, the

isothermal annealing is a powerful way to decrease the dielectric loss ε'' of oxide for the devices made from Au/SnO_2/n-Si/Al structures.

The annealing time dependence on tan δ is shown in Fig. 10. As shown in Fig. 10, dielectric loss tangent were found to be strongly dependent on thermal annealing time. It is seen from Fig. 10, tan δ decreases with increasing thermal annealing time. The values of tan δ are changed from 1.63 to 0.28 with increasing of annealing time.

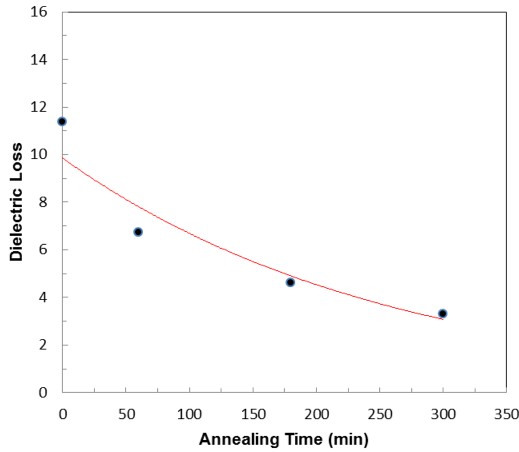

Fig 9. Variation of dielectric loss with isothermal annealing time.

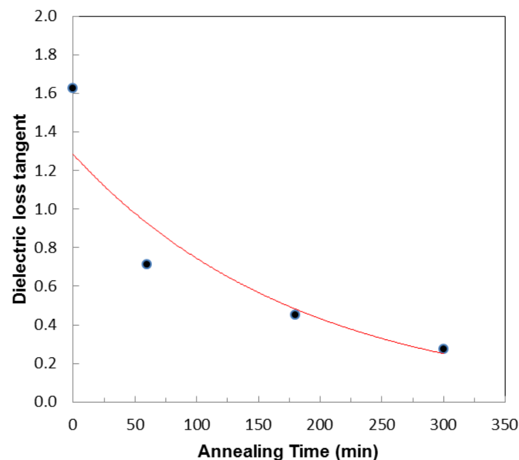

Fig 10. Variation of dielectric loss tangent with isothermal annealing time.

Fig. 11 shows the annealing time dependence of dc conductivity σ_{dc} of Au/SnO_2/n-Si/Al diodes. According to Fig. 11, it is calculated that the σ_{dc} values decrease with increase in thermal annealing time. The impurities that lie below the bottom of the conduction band are re-ordered with the thermal annealing and responsible for the reduction in conductivity. From the figure, the values of σ_{dc} are changed from 6.33 to 1.83x10^{-6} Scm^{-1}. This results show that the defects are created in the lattice and then carrier concentration is decreased with increasing of annealing time. This may be attributed to the cracks that tend to be highly enhanced along the grain boundaries and degrade the mobility of charge carriers. This cracks can be generated within films were increased by vacancies between the clusters of grains [50].

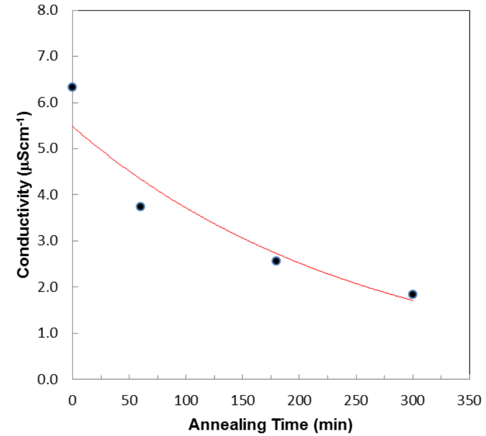

Fig 11. Variation of dc conductivity with isothermal annealing time.

3. Conclusions

The basic goal of this study was to evaluate isothermal annealing time effects on some electrical parameters of the devices made from Au/SnO_2/n-Si/Al structures. The presence of oxide layer causes changes in dielectrical properties of metal/oxide/ semiconductor structures. AFM images show that intensive thin films of SnO_2 were obtained by spin coating and surface morphology of SnO_2 thin films can be modified by means of isothermal annealing time. We determined that the ε', ε'', tanδ and σ_{dc} of the devices are extremely dependent on the voltage and isothermal annealing time. The voltage dependence can be ascribe to voltage dependent charges, mobile oxide charge oxide trapped charge and interface trapped charge of SnO_2/Si interface. The decrease in dc conductivity with thermal annealing time may be attributed to change centers created. We found that the dielectric constant was completely sensitive to thermal annealing time and increase with increasing annealing time. The increase in dielectric constant may be due to the polarization effect. On the other hand, dielectric loss was strongly decreased with increasing annealing time. These are consequences that the isothermal annealing time is an effective way to increase the dielectric constant and to decrease the dielectric loss of electronically devices.

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