Low frequency noise as a tool for diagnostic of ESD degraded GaAs mesfets

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In order to investigate degradation under ESD handling condition, commercial GaAs MESFET's were stressed with high voltage pulses of 0.7 to 3 kV applied to the gate or to the drain in an ESD experiment using standard ESD simulator test (Human Body Model - HBM). MESFET degradations were identified by I-V characteristics changes and low frequency (LF) noise measurements used as a tool for degradation diagnostic. Two modes of degradation: drain current increase (CI) and drain current decrease (CD) were observed. LF noise results have shown that most of the degradation originate by defects generated during ESD stress in space charge region of Schottky gate contact.

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1. Introduction

Electronic systems with very strong demands on high frequency, signal-noise ratio, output power and linearity, such as power radars, wide bandwidth communications or optoelectronic circuits, need to be implemented as microwave integrated circuits (MWIC). To achieve these targets MWIC are based on GaAs, InP, GaN or other heterostructure materials transistors. III-V MESFET's and HEMT's are basic components for wide bandwidth power amplifiers [1]. In these applications compound semiconductor transistors can operate under critical conditions [2], such as electrical overstress (EOS) or electrostatic discharge (ESD). Also, these devices can be sensitive to ESD stresses during handling.

In the case of MESFET, reliability is strongly influenced by the integrity of the Schottky gate barrier and the ohmic contacts. Recently, several experiments have been performed on SiC Schotky diodes to get more understanding of ESD stress applied on compound hetero-interface [3].

Depending of purpose of investigation, different stress conditions could be chosen as DC step stress, hot electron stress, transmition line pulse (TLP) measurements [2], RF overdrive test [4], electrical cycling as in life tests [5] or temperature accelerated testing [6] ESD is one of the leading causes of problems by compound devices reported by customers. 24% of root cause failures are related to EOS/ESD events [7]. ESD is a one of the major concerns also for MESFETs [8,9]. III-V based devices could be vulnerable to ESD, due to the insulating nature of sapphire substrates. In the discrete compound devices it could be additionally integrated zener or pn junction as ESD protection element [10]. In all cases the first possible source of ESD stress is the ESD stress during device handling. The effects of this kind of ESD stress we have investigated using HBM stress test. Influence of the ESD stress on the Schottky contact was analyzed under condition of stress over different MESFET terminals: ESD pulses were separately applied to gate and to drain in our experiments. The results of this kind of test and analysis of degraded samples are presented in this paper.

It is known that low frequency noise can be used as a diagnostic or screening tool in quality and reliability analysis of compound semiconductor transistors [11,12]. For example, it was observed increase by two orders of magnitude of the low frequency noise (LFN) level when MESFETs are submitted to RF life test [13], in which traps have a significant role. Also, it is shown that the 1/f noise in gate current is effective as a diagnostic tool to detect hot spot and device failures. This has been explained by the contributions of fluctuations of the leakage currents between the gate and source and fluctuations of the total gate current between the gate and drain [14]. Under ESD conditions the latent defects in the interface and channel can have a significant role in degradation of device. The latent defects are statistically distributed between devices, and therefore it may expect that the degradation of a device is not always correlated with the ESD pulse shape and amplitude only, but with the presence of defects in the device also. According to our knowledge this aspect of ESD stress was not investigated enough. One of our primary goals was to examine how low frequency noise measurements can be used as a tool for diagnostic during this kind of test. Therefore, in our research we have used one of standard ESD stress methods (ESD handling stress) and selected such voltage amplitudes by which test samples will be degraded without catastrophic failures. At this stage of investigation we did not have the goal to analyze in details the energy aspect of ESD stress (for example by change of current pulse shape).

In this paper the results of our investigation of the ESD stressed GaAs MESFETs are presented. The role of

the defects in device degradation and their statistical distribution between devices was analyzed. The experimental details are described in Section 2, and the results, model and discussion are presented in Sections 3 and 4.

2. Experimental details

Commercial GaAs MESFETs used in our ESD experiments are capable of delivering 3W of output power with high linear gain, high efficiency and excellent linearity. In manufactur's data sheet [15] is written the MESFETs are fabricated in 0.7μm-technology with Ti/Al gate. The transistor's pinch off voltage has typical value of –2.6V with variations between -1.6V and -3.6V. A simplified transistor structure is shown in Fig.1. For the purpose of our experiments we have selected the units with approximately same I-V characteristics prior the ESD test. To stress the devices, we used a commercial ESD simulator based on the ESD standard – Human Body Model (HBM). It defines the current waveform used for the discharge of a 100pF capacitor through a 1.5 kΩ resistor for different discharge voltages. This a standard method used in many companies in device qualification process related to device handling.

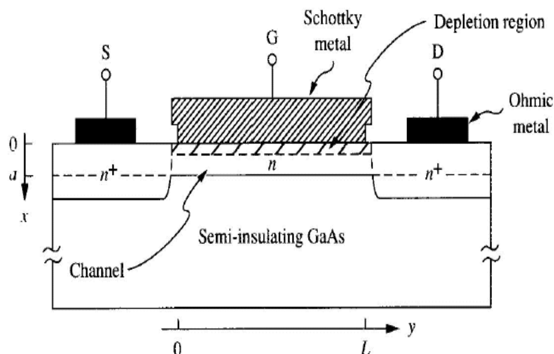


Fig 1. Simplified cross-section of GaAs MESFET (n^+-gate regions at source and drain sites are negligible).

The MESFET structure consists of a lateral channel limited with space charge region reversely biased gate Schottky contact, n-semi-insulating (n-n^-) junction related to substrate and l-h (low-high doped n-n^+) junctions at the source and drain sides. During normal operating conditions, the channel current is controlled with reverse biased Schottky contact and leakage current of Schottky contact could be observed as a contact quality measure. With «+» voltage at the drain contact, electrons are injected from n in n^+ region of l-h junction at drain side. The electrical field of the n-n^- junction (floating substrate) blocks for the electrons, because of the contact potential difference. The ESD stress effect could be connected with metal-semiconductor contact degradation and with charge transport conditions through the channel. To separate these effects, we made experiments by applying «+» voltage impulses (0.7 and 1kV) on the gate (between gate and source) with a floating drain and substrate (experiment A), and applying «+» voltage impulses (1 and 3kV) on the drain (between drain and source) with the gate and substrate floating (experiment B). A sample of 20 items in each of the experiments (A and B) was used. The voltage pulses were selected after preliminary experiments which have shown that under these stress conditions the probability of catastrophic failures was reduced significantly. Lower voltages are selected to be enough to induce degradation, and higher voltages are selected to induce degradation without the device destruction. During experiment A, the Schottky contact is directly exposed to the ESD pulse and during experiment B it is indirectly exposed to the ESD pulse.

Measurements of current-voltage (I-V) characteristics were used to detect degradations. In order to obtain more information about degradation we have measured the low frequency noise in degraded MESFETs. The power spectral density of the current fluctuations was measured by a measurement system based on Dynamic Signal Analyzer (HP3562A) and low noise preamplifier (Keithley 103A), in the frequency range between 10Hz and 100kHz at room temperature.

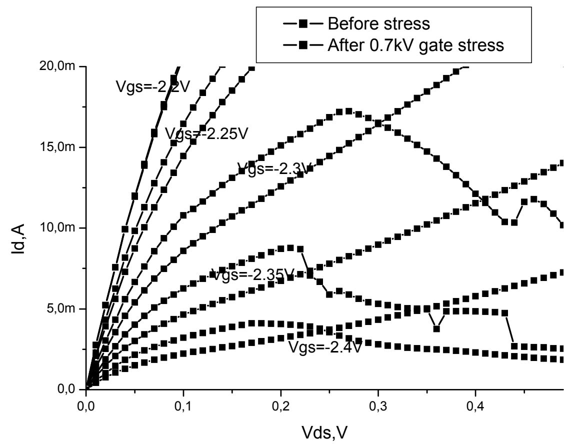
3. Experimental results

The experiments follow the steps: selection of 40 transistors with approximately same I-V characteristics (referent curves), separation selected transistors into two groups for experiments A and B, exposure of items to the given ESD stress condition and identification of degraded items using a criteria: changed I-V characteristics. This was followed by detailed measurements of I-V characteristics and noise of degraded transistors in other to analyze degradations and to examine effectiveness of noise measurements as an un-destructive method for analysis of ESD (HBM) stress test effects.

3.1 Degradation of I-V characteristics

After stressing the gate with high voltage pulses, two different modes of I-V characteristics degradation were observed (Fig.2): increase of the drain current, current increase (CI) degradation mode, for stress voltages of 0.7 kV – Fig.2a and decrease of drain current, current decrease (CD) degradation mode, for stress voltages of 1 kV – Fig.2b. This indicates two potential types of degradation which may be caused by defects of different nature and location.

The presence of latent defects [16] in devices has a statistical characteristic and the CI or CD degradation mode is not necessarily correlated with stress voltage amplitude only, but also with the defects present in the device.



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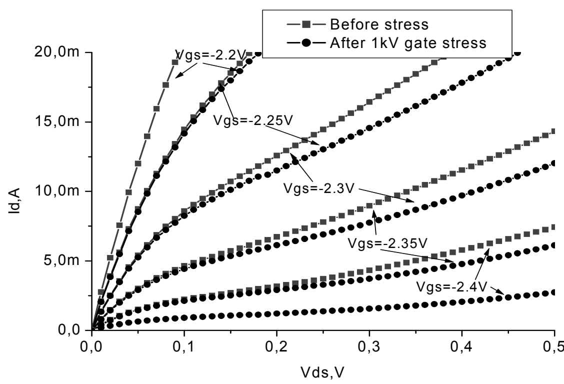

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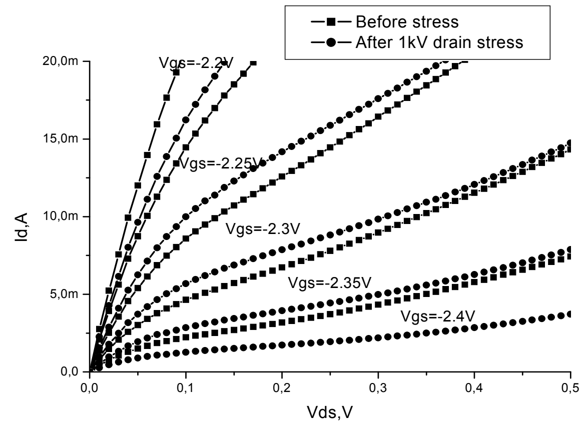
Fig. 2. I-V characteristics of MESFET before and after ESD stress by 0.7kV (a) and 1kV (b) voltage pulse at gate



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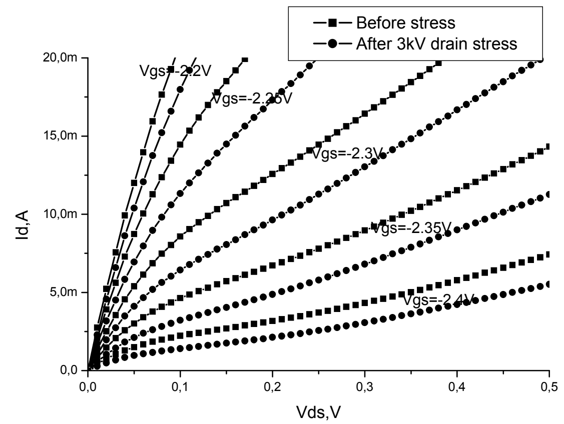


b)

Fig. 3. I-V characteristics of MESFET before and after ESD stress by 1kV (a) and 3kV (b) voltage pulse on drain

The results of the experiments with indirect stress influence on contact (experiment B) – stress applied on drain (gate and substrate floating) are shown in Fig. 3. It could be observed in this Figure that for both low and high voltage stresses, the drain current has decreased after the stress. As we can see in Fig.3, decrease of drain current not have be directly proportional to the voltage peak. This could be explained by statistic of latent defects in the samples. The differences between curves in Fig. 4 for 0.7 kV and 1.0 kV stress on gate can also be understand as the consequence of the latent defects. The mechanisms that influence decrease in drain current are probably different in the experiments A and B. The possible failure mechanism in the case of the experiment A would be atom diffusion at the gate contact, and in the case of the experiment B creation of defects due to inelastic carrier scattering.

3.2 Low frequency noise

One can expect that degradation of the Schottky contact of degraded MESFET to be „visible“ in gate current low frequency noise spectra. In order to obtain information about location of degradation without destruction of test samples the noise measurements were realized with Schottky contacts in the transistor and diode (two options of source-gate diode: floating drain and drain short connected with source) modes. The noise spectra (Figs. 4, 5 and 6) for both modes have approximately the same magnitudes and shapes that means that the Schottky contact region is degraded during the ESD stress.

As we can observe in Fig. 4, the noise spectra before stress have an $1/f^{\gamma}$, $\gamma > 1$, dependence at the left side of the measured frequency region. This dependence with $\gamma > 1$ is a consequence of the fact that together with 1/f noise there is a source of the noise with Lorenzian spectrum whose characteristic frequency is smaller then 10Hz, which will be confirmed latter in sub-section 4b (Table 2).

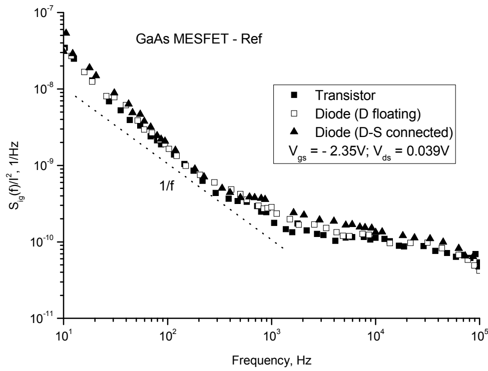
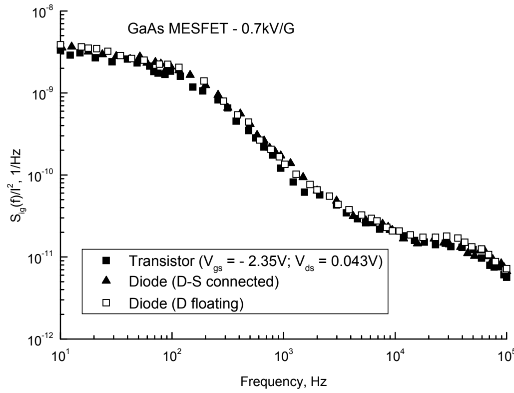


Fig. 4. Relative gate current noise spectral densities of MESFET before stress: transistor (■) and diode (□, ▲) modes

All noise spectra for MESFET's after ESD stress in gate (Fig. 5) have noticeable noise components with Lorentzian spectra with characteristic frequencies in the measurement range. From the fact that noise spectrum shapes and noise levels approximately are the same for transistors in transistor and diode modes, one can conclude that the same noise sources are in question in these cases.



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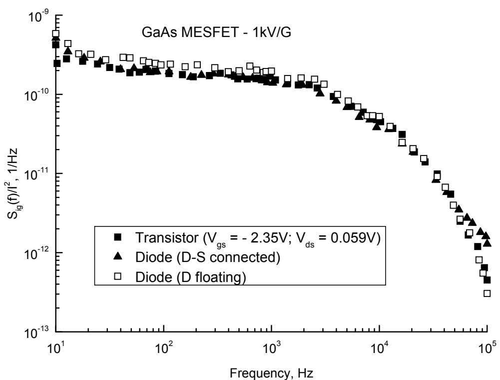
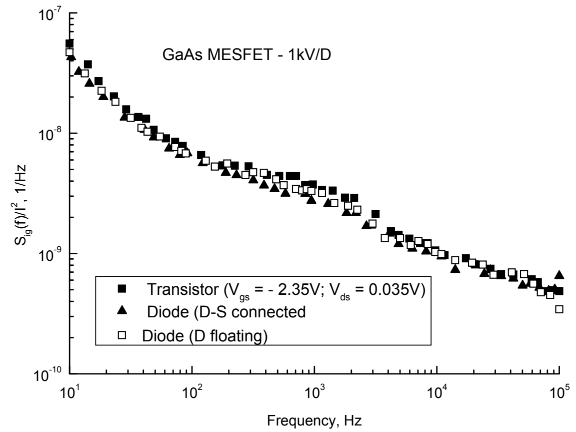


b)

Fig. 5. Relative gate current noise spectral densities of MESFET in transistor and diode mode after stress with a voltage pulse of 0.7 (a) and 1kV (b) on the gate.

The opposite result related to noise components with Lorentzian spectra is obtained in the case of ESD stress on the drain (Fig.6), where there is no obvious presence of them. This is in correlation with the I_d-V_d degradation, which suggests that there are different mechanisms behind the degradations of the gate and drain stresses. In the case of 3kV stress, one can observe a greater slope in the spectra for low frequencies. This slope could be connected with noise components with Lorentzian spectra with characteristic frequencies lower then 10Hz.



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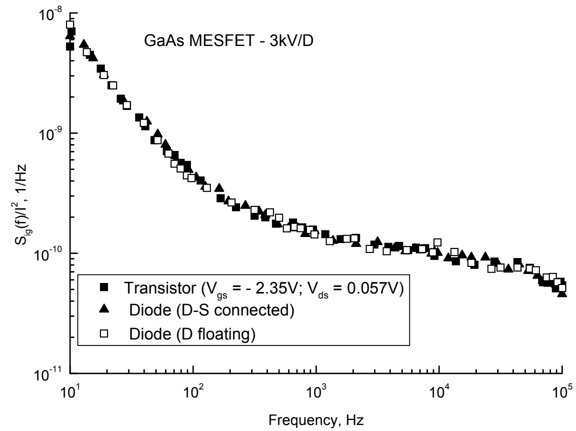

b)

Fig. 6. Relative gate current noise spectral densities of MESFET in transistor and diode mode after stress with a voltage pulse of 1 (a) and 3kV (b) on the drain.

Comparison of all mentioned experimental relative spectra of MESFET's (transistor mode) are presented in the Fig.7 together with full lines which represent the theoretical curves as the results of fitting them with experimental results. This is discussed in the following section.

4. Analysis and discussion

4.1 Drain current of degraded transistor

The experimental results related to the output and transfer characteristics of degraded transistors address to conclusion that different failure mechanisms are present in the MESFETs depending of stress conditions. Generally, two degradation modes which have been observed, drain current increase (Fig.2a) and drain current decrease (Fig.2b and 3) have been observed, could not be caused by the same degradation processes. The degradation of the I-V characteristics can be caused by gate leakage current and/or by change in the current transport conditions through the channel after stress. The leakage currents under conditions of noise measurements, V_{gs} = -2.35 V and V_{ds} in range of 0.035 V to 0.06 V, were of order of magnitudes of 10^{-7} A before stress, 10^{-6} A stressed on gate and $5\cdot10^{-7}$ A stressed on drain. According to the fact that the changes of drain currents are of order of magnitude of mA, the current of transistors with the CI mode of degradation the drain current is not only degraded by the leakage current.

To estimate the possible causes of I-V characteristic degradation, taking into account changes in carriers transport conditions across the channel, we have analyzed the I_d-V_d characteristic of MESFET given implicitly as

$$I_d = 2G_{ch0}\left\{V_d - (r_S + r_D)I_d - \frac{2}{3V_p^{1/2}}\left[(V_d - r_D I_d - V_g + V_{bi})^{3/2} - (r_S I_d - V_g + V_{bi})^{3/2}\right]\right\} \quad (1,2)$$

where $G_{ch0} = qN_D\mu_n dZ/L_g$, q – the absolute electron charge, N_D – the channel dopant concentration, μ_n – the effective electron mobility, d – the thickness of the channel, Z, L_g – the width and the length of the gate, respectively, r_S, r_D – the source and drain series resistances, respectively, $V_p = qN_d d^2/(2\varepsilon_s)$ corresponds to the gate voltage that leads to the charge depletion region over the channel thickness d in approximation to the total depletion, ε_s – the dielectric constant of semiconductor, V_{bi} – the gate built-in potential. The pinch-off condition is defined as $V_p = V_d - r_D I_d - V_g + V_{bi}$. The equation (1) describes the I_d-V_d characteristic for $V_d \le V_{dsat}$, where V_{dsat} is the minimal V_d that satisfies the pinch-off condition. For $V_d > V_{dsat}$ the drain current is constant ($I_d = I_{dsat}$, $r_D = 0$) or limited by r_D ($I_d > I_{dsat}$, $r_D \neq 0$, satisfied pinch-off condition). To estimate how the changes in MESFET parameters influence the changes in drain current we have numerically analyzed equation (1). The qualitative results of this analysis which illustrate trend of changes and an example of numerical results as an illustration of the changes are shown in Table 1.

Table 1. Drain current changes due to MESFET parameters changes (I – increase, D – decrease).

Parameter (P_i)	Parameter P_j change	Current I_d change	P_j [1)] change	I_d [1)] change
Geometric parameters - width of gate (Z) - length of gate (L_g) - thickness of channel (d)	I(D) I(D) I(D)	I(D) D(I) I(D)	I:1.2x I:2x I:1.3x	I:1.2x D:2x I:13.4x
Impurity concentration (N_D)	I(D)	I(D)	I:1.08x	I:2.73x
Effective mobility (μ_n)	I(D)	I(D)	I:1.18x	I:1.15x
Built-in potential (V_{bi})	I(D)	D(I)	I:1.5x	D:1.9x
Series resistance (r_S, r_D)	I(D)	D(I)	I:10x	D:1.24x

[1)]For example, I:1.2x means 1.2 times higher than nominal value; D:2x means 2 times less than nominal value.

As can be seen in Table 1, both an increase and decrease of the drain current are possible depending on the nature of changes of the given transistor parameter during stress. The contact potential V_{bi} includes implicitly the interface properties through the dependence of the barrier height on the interface. The series resistances r_S and r_D include both bulk and surface conductivity of the source-gate and gate-drain regions. Our detailed numerical analysis has shown that the current is the most sensitive factor to the effective impurity concentration and the changes in the contact interface. N_D is included in G_{ch0}, V_p and V_{bi}, and thus the change, for example, of 8% in N_D results in current change of 173% at V_d = 0.06V. It has to be noted also the possible compensation effects. For example, degradation in interface will be included in V_p and V_{bi}, but not in G_{ch0}, that is a parameter of the bulk conductive part of the channel.

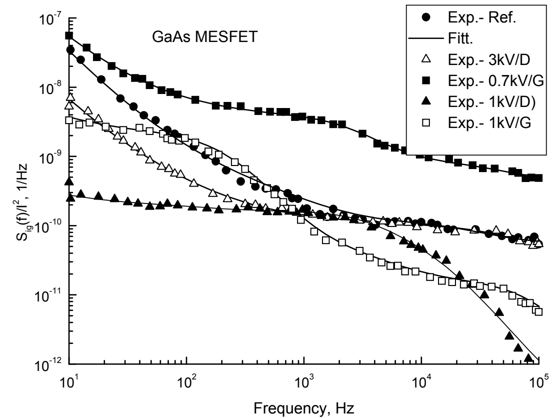

Fig. 7. Gate current noise spectral densities of unstressed and stressed MESFETs (full lines – fitting of experimental and theoretical results)

The change of effective mobility may be a consequence of new scattering mechanisms after degradation or enhanced influence of any scattering mechanism that was also present before degradation. The

effective change of channel thickness, i.e. effective increase of the space charge region could be a consequence of donor positive charge compensation by the acceptor like defects produced by the ESD stress in the contact interface.

Fig. 8. Small signal low frequency equivalent circuit of degraded MESFET including noise sources

In the ESD degradation, the thermal effects have a significant role [17]. Although the ESD stress pulse that we have used in the experiments had an unfavorable shape for thermal analysis, we have estimated the local volume in which the basic material GaAs melting temperature (θ_l = 1237°C) can be achieved. This is significant for estimation of conditions for atom diffusion and defect creation mechanisms in gate contact region during stress. We examined reality of this process in following way. The ESD pulse was realized by discharging a capacitor (C_C = 100pF) over a series circuit, which defines the time constants: [pulse duration t_d = 150ns and rise time t_r = 10ns]. If the capacitor is charged to V_C = 1kV, and modeling the current pulse with a triangular pulse with the same duration t_d and the rise time t_r as the real pulse, and using the data for GaAs [18] (specific heat capacity c_p = 0.325 J g^{-1} °C^{-1}, density ρ = 5.316 g m^{-3}), with approximation that there is no heat conduction during the ESD pulse (all energy is used for local temperature increase), we have obtained the following: If the ESD energy is smoothly executed during the pulse, the melting temperature is achieved in the box with an edge of 60nm, but if one uses a maximum pulse power $I_{max}V_{max}$ during Δt = 10ns (part of handed energy: $I_{max}V_{max}\Delta t = 1.02\cdot10^{-5}$ J), then the melting temperature is achieved in the box with an edge of 16.5μm. These two extreme values confirm that thermal effects may really be present.

4.2 Low frequency noise and degradation

As can be observed in Fig.7, ESD stress produces different effects on low frequency noise. It has already been published [19] that noise sources in MESFET could be (i) in the region of conducting channel (conductivity fluctuations), (ii) in the source and drain neighboring regions (conductivity_fluctuations, fluctuations in surface carrier trapping process and in l-h regions of source and drain junctions), (iii) in the space charge region of Schottky gate contact and isolation p-n junction related to substrate (charge fluctuations) and (iv) in the Schottky contact region (fluctuations in gate leakage currents). In the equivalent circuit [19] noise sources (iii) and (iv) are represented in the gate circuit with parallel connection between the current source and resistor together with serial connection of voltage source, and noise sources (i) and (ii) are represented with a current source on the drain. In reference [14], experimental results for noise are explained with the model where the Schottky diode is shunted with conductance to source and drain, in other words, the gate edge currents dominate in the noise spectra. Series resistance to the source and drain was introduced in [20] too, and generally it should be noted that many different noise sources in FET might be important, including the contribution of the gate leakage current, contact noise, bulk noise, surface noise, and fluctuations of the Schottky barrier space region (SCR) width. According to our results that gate current noise spectra in transistor and diode mode measurements have approximately the same magnitudes and shapes the noise sources are located in the Schottky contact region.

Table 2. Parameters of extracted noise components.

ESD stress	Degrad. mode	A A^2/Hz	B/I_g^2	C_{gr1}/I_g^2	f_1 Hz	C_{gr2}/I_g^2	f_2 kHz	C_{gr3}/I_g^2	f_3 kHz
Ref.		1.34×10^{-25}	1.13×10^{-7}	1.45×10^{-5}	1				
0.7kV/Gate	CI	3.7×10^{-25}	1.6×10^{-8}	2.53×10^{-6}	202	5.44×10^{-7}	5.74	8.17×10^{-6}	86.0
1kV/Gate	CD	3.97×10^{-25}	2.0×10^{-9}			2.7×10^{-6}	3.7	3.73×10^{-6}	34.0
1kV/Drain	CD	4.51×10^{-26}	3.6×10^{-7}	6.22×10^{-6}	1	$4.36\times10^{--5}$	2.42	4.5×10^{-4}	12.0
3kV/Drain	CD	1.82×10^{-25}	2.4×10^{-8}	2.78×10^{-6}	1	$4.6\times10^{--7}$	1.8	5.65×10^{-5}	120.0

In order to model noise of degraded MESFET's we have divided transistors with a plane S' near the gate on the source side and a plane D' near the gate on the drain side, perpendicular to the substrate, in its intrinsic region (transistor S'GD') and neighboring source (SS') and drain (D'D) regions. In that small signal transistor circuit (Fig. 9), conductance $g_{G'} = 1/r_{G'} = g_{GS'} + g_{sh}$ takes in consideration the degradation as leakage current at the gate edge from gate to source ($g_{GS'} = 1/r_{GS'}$) and degradation of contact region ($g_{sh} = 1/r_{sh}$), and with $g_{GD'} = 1/r_{GD'}$ is considered the leakage current at the gate edge from gate to drain. Surface conductances $g_{SS'} = 1/r_{SS'}$ to source and

$g_{DD'} = 1/r_{DD'}$ to the drain are included in conductances $g_{S'} = 1/r_{S'} = g_{SS'} + g_S$ and $g_{D'} = 1/r_{D'} = g_{DD'} + g_D$, together with neighboring conductances of the source ($g_S = 1/r_S$) and drain ($g_D = 1/r_D$) regions. The transistor channel conduction S'GD' is $g_{ch} = 1/r_{ch}$.

Under the condition that noise sources are independent, noise spectra for all noise sources related to the currents $i_{G'}$, $i_{S'}$, $i_{ch'}$, $i_{D'}$ and $i_{GD'}$ in particular branches of equivalent circuit in Fig. 9 could be written as:

- Noise spectrum related to the current $i_{G'}$

$$S_{iG'}(f) = S_{iGS'}(f) + S_{ish}(f) + S_{iG0}(f)\,, \tag{2}$$

where the first and the second term on the right side of the equation represent noise originating from degradation along the gate edge at the source side ($S_{iGS'}$) and the Schottky contact (S_{ish}), respectively, and the third term – noise from non-degenerated Schottky junction region.

- Noise spectrum related to the current $i_{S'}$

$$S_{iS'}(f) = S_{iSS'}(f) + S_{irS}(f)\,, \tag{3}$$

includes noise due to fluctuations of surface ($S_{iSS'}$) and bulk (S_{irS}) conductance of the neighboring source region.

- Noise spectrum related to the current $i_{ch'}$

$$S_{ich'}(f) = S_{ivgs'}(f) + S_{ich}(f)\,, \tag{4}$$

considers noise originating from the gate voltage ($S_{ivgs'}$) and channel (S_{ich}) noise in transistor S'GD'.

- Noise spectrum related to the current $i_{D'}$

$$S_{iD'}(f) = S_{iDD'}(f) + S_{irD}(f)\,, \tag{5}$$

is a consequence of surface conductance fluctuation ($S_{iDD'}$) and volume conduction fluctuation (S_{irD}) of neighboring drain region.

- Noise spectrum related to the current $i_{GD'}$ is $S_{iGD'}(f)$.

From the equivalent circuit in Fig.9 we have found i_g and applying the Fourier transformation we developed the expression for the gate current noise spectral density:

$$S_{ig}(f) = S_{iG'}(f)\cdot F_{gs'}^2 + S_{iGD'}(f)\cdot F_{gd'}^2 + S_{iS'}(f)\cdot F_{SS'}^2 + S_{iD'}(f)\cdot F_{DD'}^2 + S_{ich'}(f)\cdot F_{ds}^2 + S_{iD}(f)\cdot F_D^2 + S_{iG}(f)\cdot F_G^2\,, \tag{6}$$

The last two factors in equation (6) consider noise originating from the circuit with the definition of drain (S_{iD}) and gate (S_{iG}) quiescent point.

Factors F_k are defined with the following expressions:

$$F_{gs'} = \frac{r_{G'}}{\det A}\left[r_{G'}r_{S'} + r_{GD'}(r_{S'} + r_{ch}) + (r_{GD'} + r_{ch})(R_D + r_{D'})\right]\,, \tag{7a}$$

$$F_{gd'} = -\frac{r_{GD'}}{\det A}\left[r_{G'}r_{S'} + r_{ch}(r_{G'} + r_{S'}) + r_{G'}(R_D + r_{D'})\right]\,, \tag{7b}$$

$$F_{SS'} = \frac{r_{S'}}{\det A}\left[r_{GD'}r_{ch} + (r_{G'} + r_{GD'} + r_{ch})(R_D + r_{D'})\right], \tag{7c}$$

$$F_{DD'} = -\frac{r_{D'}}{\det A}\left[r_{G'}r_{ch} + r_{S'}(r_{G'} + r_{ch} + r_{GD'})\right], \tag{7d}$$

$$F_{ds} = \frac{r_{ch}}{\det A}\left[r_{G'}(R_D + r_{D'}) - r_{S'}r_{GD'}\right], \tag{7,8e}$$

$$F_D = -\frac{R_D}{\det A}\left[r_{G'}r_{ch} + r_{S'}(r_{G'} + r_{ch} + r_{GD'})\right], \tag{7f}$$

$$F_G = \frac{R_G}{\det A}\left[(r_{G'} + r_{GD'})(r_{S'} + r_{ch}) + r_{S'}r_{ch} + (r_{G'} + r_{GD'} + r_{ch})(R_D + r_{D'})\right]\,. \tag{7g}$$

where

$$\det A = (r_{S'} + r_{ch} + R_D + r_{D'})\left[R_G r_{G'} + r_{GD'}(R_G + r_{G'})\right] + (R_D + r_{D'})\left[R_G r_{ch} + r_{S'}r_{ch} + r_{S'}(r_{G'} + r_{ch})\right] + r_{S'}r_{ch}(R_G + r_{GD'})\,. \tag{8}$$

Contribution of particular noise sources to the overall noise in the gate circuit depends on the j-th noise source level and the factor F_j, which are a measure of the conversion of the noise in the MESFET's input circuit. The equations (6) and (7) show how generally any inner transistor region may influence the transistor noise properties and illustrate how noises from local noise sources are converted in the gate current noise. The stressed transistors in our experiments are high frequency transistors (1 GHz range) and influence of DD' SS' short regions on total noise may be neglected. The similar spectra in the transistor and diode modes show that the main contribution to the total noise results from the branches $i_{G'}$ and/or $i_{GD'}$ The capacitive effects can be neglected due to low frequency range of the measurements. Therefore, the frequency dependences of the noise spectra may be determined only with the spectra $S_{iG'}(f)$ and/or $S_{iGD'}(f)$, i.e . the first two terms in (6).

With fitting experimental results and theoretical curve defined as the empirical relation under condition of independent noise sources

$$S_i(f) = A + \frac{B}{f} + \sum_j \frac{C_{grj}\tau_j}{1+\omega^2\tau_j^2}, \qquad (9)$$

we have extracted the noise components which are presented in Table 2. The fitting procedure is based on the fitting condition of minimum of sum of squared relative error. A computer software was developed in which the initial conditions are first identified from $fS_i(f)$ data and than the magnitude and shape of fitting curve were corrected by changes in fitting parameters to be satisfied the fitting condition. The fitting of the results are presented in fig.8 with straight line. First factor in equation (9) represents the white noise, i.e. shot noise $A = 2qI_g$ in the case of results in Table 2., second and third factor in (9) represent 1/f noise and noise sources with Lorentzian spectra with typical frequencies $f_j = 1/2\pi\tau_j$, respectively. The relative noise parameters $B_n = B/I_g^2$ and $C_{nj} = C_{grj}/I_g^2$ are shown in the Table 2.

In connection with the I_d-V_d and noise results it has to be pointed out the following. According to our conclusion that the gate leakage does not influence dominantly the drain current changes in degraded transistors and that the gate current noise sources are located in the Schottky contact region we can conclude that the Id-Vd changes contain information about carrier transport along the channel and the gate current noise – transversal to the gate contact.

One can see that there are the differences between the levels of 1/f noise in the cases of ESD stresses in gate and drain. Generally, the 1/f noise parameter B_n decreases after stress, particularly in the case of the stress in gate. Decreasing the 1/f noise component (parameter B_n) implies that 1/f noise is caused by carrier mobility fluctuation due to fluctuations of carrier phonon scattering [20] in the space charge region of Schottky contact [21], [13]. The effect of the fluctuations of carrier phonon scattering will be reduced with scattering on defects created during ESD stress that leads to decrease of B_n. According to the I_d-V_d behavior after stress these defects behave as acceptor like traps, which take part in the gate tunnelling current and at the same time they compensate space charge in the Schottky contact region. Carrier capture fluctuations are sources of noise components with Lorentzian spectra whose parameters C_{grj}/I_g^2 and f_j are presented in Table 2. Therefore, contributions of other regions in expression (6) could be neglected. In the case of gate degradation by defect generation in the Schottky contact region the following relationships for the resistances in the equivalent circuit in Fig.8. can be used: $r_{G'} \approx r_{sh} >> r_D, r_{ch}, r_S, R_D$; $r_{S'} \approx r_S$; $r_{GD'} >> r_{sh}$; $r_{D'} \approx r_D$. At the same time conditions related to (8) could be approximated as $\det A \approx r_{GD'} r_{sh}(r_S + r_{ch} + r_D + R_D)$, which implies using the equation (7a) $F_{gs'} \approx 1$. Also expression (6) can be approximated with $S_{ig}(f) \approx S_{ish}(f)$, e.g., the gate noise of transistors degraded by ESD stress described in this paper is determinate by noise sources in degraded Schottky junction region of MESFET. Noise with Lorentzian spectra with typical frequency less then 10Hz is connected with defects in contact regions presented before stress also (Lorentzian with C_{gr1} and f_1 in reference transistor, Table 2). The new Lorentzian spectra in stressed transistors are connected with defects created during stress.

5. Conclusion

ESD stresses applied on a MESFET gate and drain by single impulses with amplitudes from 0.7 to 1 kV and from 1 to 3 kV, respectively, have shown that two drain current degradation cases are possible; an increase (CI) and decrease (CD) of drain current. We have proposed a general expression for the gate noise of degraded transistor that is obtained using low frequency small signal equivalent circuit and assumed that noise sources are independent. A decrease of 1/f noise and the presence of Lorentzian spectra are connected with acceptor like defects generated in the space charge region near the Schottky contact. The results for gate current 1/f noise are explained by fluctuations in carrier scattering mechanisms in the space charge region of gate Schottky contact.

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