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Memory characteristics of Ni-NiO_x core-shell nanocrystals embedded in SiO_2 gate oxide for nonvolatile flash devices

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The memory characteristics of Ni-NiO_x core-shell nanocrystals (NCs) in the metal-oxide-semiconductor (MOS) capacitor structure were investigated. Scanning electron microscopy (SEM) and high-resolution transmission electron microscopy (HRTEM) confirm the formation of the spherically shaped, well isolated, and uniformly distributed Ni NCs surrounded by NiO_x (1-1.5nm) in MOS capacitor. The Ni-NiO_x NCs in MOS capacitor exhibited a large memory window of 10.6 V as well as efficient programming/erasing speeds and better retention characteristics. A possible band model needed for injection efficiency of carriers was given by considering the electron/hole barrier width and the additional interface states through the NiO_x shell.

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Nonvolatile memory devices based on discrete nanocrystals (NCs) as floating gate have received considerable attention due to smaller operation voltage, high storage ability, prevention of lateral charge movement and so on[1-6].The first NC nonvolatile memory devices were demonstrated utilizing Si NCs embedded in SiO_2 by Tiwari et al[1].Since then, many attempts have been made to develop nonvolatile memory devices using floating NCs such as semiconductor NCs[7],metal NCs[8],compound NCs[9,10], as well as others[11].Among these materials, metal NCs have some advantages over semiconductor counterparts[12], such as a wide range of available work functions, smaller energy perturbation due to quantum confinement and stronger coupling with channel. However, when integrating the metal NCs into the memory device structure, there are still some obstacles. The first is how to fully control the structural characteristics of the nano-scaled NCs. That is to say, to find a way to control the size, density, shape and dispersion of these NCs[13-16].Second, it is required to prevent metal diffusion during high-temperature processes in device integration, which potentially degrade device performance[17].

In this letter, we present the performance of a Ni-NiO_x core-shell NCs as discrete charge traps in metal oxide semiconductor (MOS) capacitor devices embedded in SiO_2 oxide matrix. The memory effects of Ni NCs surrounded by formed NiO_x shell due to ex situ RTA (rapid thermal annealing) in N_2/O_2 mixed ambient are observed. Accordingly, the structural and electrical properties of the Ni-NiO_x core-shell NCs in MOS capacitor are discussed and a possible band model is put forward.

3 inch p-type (4-10 Ω·cm) Si wafers with (100) orientation were cleaned by standard Radio Corporation of America (RCA) recipes and native oxide was removed by diluted hydrofluoric acid. After that, 2.5nm tunneling SiO_2 layer was thermally grown by dry oxidation at 750℃.In order to reduce the interface stated and defects between Si and SiO_2, a subsequent annealing was done in N_2 for 30 min up to 900℃.Then, the sample is introduced in a vacuum chamber with a base pressure of 1.0×10^{-6} mbar, equipped with two electron guns, where deposition is controlled with the use of two piezoelectric crystal thickness monitors. Initially, 20 Å of Ni (nominal thickness) wetting layer are deposited, by e-beam evaporation of metallic Ni, at room temperature, at a rate of 0.3Å/s.Subsequently,the sample was brought out from the chamber and then RTA was performed in N_2/O_2 (N_2:O_2=5:1) mixed ambient at 550℃ for 45s to form Ni-NiO_x core-shell NCs. Finally, SiO_2 film with the thickness of 40 nm was deposited as the control oxide layer by e-beam evaporation. At the same time, the control samples without Ncs with the same process and with Ni NCs were fabricated for comparison. The MOS capacitor embedded with Ni NCs was prepared by in situ e-beam evaporation: After 20 Å of Ni wetting layer was deposited, 40 nm SiO_2 control oxide was deposited on the Ni layer in situ using the same condition as above. Subsequently, RTA

in N_2 ambient at 900℃ for 1min was performed. Finally, removing the native oxide on the backside of the Si wafers of all the samples, the metal electrodes were formed by evaporation of aluminum through the shadow masks and the area of the top electrode is 2×10^{-3} cm^{-2}. The structure of these MOS capacitors was examined by high-resolution transmission electron microscopy (HRTEM) to observe the size, shape, distribution and position of NCs in the gate oxide. Scanning electron microscopy (SEM) was used to investigate the effects of the wetting layer thicknesses and annealing temperatures on the NCs size and density. The high-frequency capacitance- voltage (C-V) relations and the retention characteristic of the MOS capacitors were measured at 1MHz and at room temperature by using HP 4284A. P/E speed measurements by using an Agilent 81104A Pulse generator were performed with LABVIEW code.

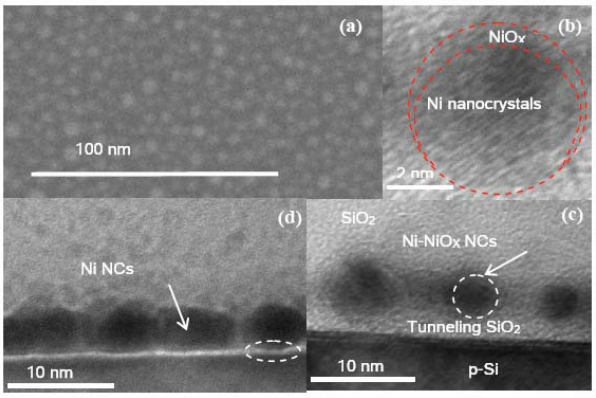

Fig.1. (a)Typical surface SEM images of Ni-NiO_x NCs, Cross-sectional HRTEM images of MOS capacitors embedded with (b) and (c) Ni-NiO_x NCs by ex situ RTA at 550℃ for 45s in N_2/O_2 (N_2:O_2=5:1)mixed ambient, and (d)Ni NCs by in situ e-beam evaporation followed by RTA at 900℃ for 1min in N_2 ambient

Fig. 1(a) shows the typical SEM images of the Ni-NiO_x core-shell NCs formed on the thin SiO_2 tunneling oxide layer before the deposition of the top SiO_2 control oxide layer. In Fig.1 (a), the average diameter and areal density of NCs are estimated as about 5nm and $4\times10^{12}/cm^2$, respectively. The formation of NCs is the process of the nonequilibrium state clusters reshape to obtain a local minimum energy state [18].Thus, the RTA process helps the Ni film get more stable clusters by increasing surface diffusion, and then the more stable clusters self-assemble together to form Ni NCs. Fig. 1 (c) presents the cross-sectional high-resolution transmission electron microscopic (HRTEM) images of the Ni-NiO_x core-shell NCs that were embedded in the gate dielectric after RTA at 550℃ for 45s in N_2/O_2 (N_2:O_2=5:1) mixed ambient. It should be noted that the Ni-NiO_x core-shell NCs are mostly spherical and well isolated in the SiO_2 matrix. As shown from the local HRTEM image in Fig.1.(b), a thin and bright localized shell layer with about 1nm thickness surrounds the Ni NC which reveals distinct lattice fringe patterns. We expect that this shell layer is related to the NiO_x. However, it is still unknown whether the thin shell layer at the interface between the Ni NCs and SiO_2 layer is exactly NiO_x. Therefore, further research techniques about this issue are being pursued due to the difficulties of analyzing this 1nm layer. However, as shown in Fig.1 (b), the bright region of HRTEM images was widely visible, indicating there are partial oxidizations of Ni elements. We consider that the interface shell layer was induced during the fabrication of the NCs because of the *ex situ* RTA in N_2/O_2 (N_2:O_2=5:1) mixed ambient.Fig.1 (d) shows the HRTEM images of Ni NCs embedded in SiO_2 matrix by *in situ* deposition followed by RTA at 900℃ for 1min in N_2. It is obvious to observe that Ni NCs formed by RTA for the whole gate stacks exhibit larger size dispersion and worse aerial uniformity than those shown in Fig.1 (c).Furthermore, some of those aspherical Ni NCs slightly diffuse to the substrate interface by high temperature annealing at 900℃.Nevertheless, any interfacial shell layer was clearly not present in the Ni NCs through RTA in N_2 ambient. Therefore, it is expected that the process of *ex situ* RTA in N_2/O_2 (N_2:O_2=5:1) mixed ambient could help form NiO_x interfacial shell layer to prevent Ni diffusion during high-temperature process, and further come into being spherical, uniformed, and well isolated Ni-NiO_x core-shell NCs. Therefore, such an oxidized NiO_x interface layer could have additional effects on the retention characteristics and programming/erasing (P/E) speeds.

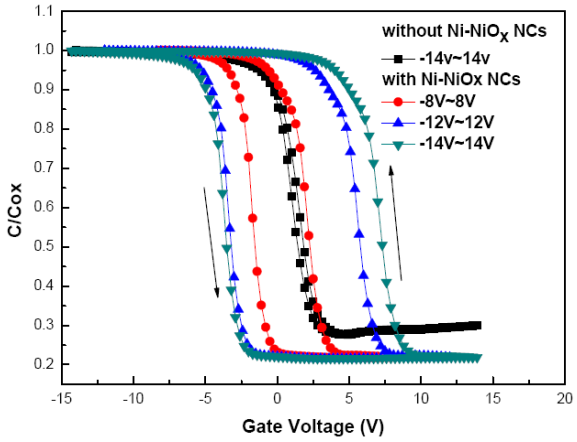

Fig.2 High frequency (1MHz) C-V characteristics of the MOS capacitors with Ni-NiO_x core-shell NCs by changing the sweep range from (-8~+8) to (-14~+14)V. The data of the device with no NCs are also presented in the range of (-14~+14) V.

Fig. 2 shows the high-frequency (1MHz) C-V curves of MOS devices by changing the sweep range form (-8~+8) to (-14~+14)V. Since the hysteresis loop comes from charge trapping within MOS capacitor, both the potential well formed by the embedded NCs and the defects in the gate oxides may act as traps for charges. As observed from

the figure that the reference sample without NCs displays a normal high-frequency C-V characteristic for the MOS capacitor and a negligible hysteresis, the contribution from oxide traps or mobile ions in the dielectrics layer is negligible. In contrast, the MOS structure embedded with Ni-NiO_x core-shell NCs exhibits a broad hysteresis loop in the C-V curves that is accompanied by a large flatband voltage shift (V_{fb}), thereby revealing a significant memory effect in the MOS structure. It should be noted that all samples show counterclockwise C-V hysteresis loops, indicating substrate injection behavior. The memory window increases steadily from 3.4 to 10.5 V with the increasing applied gate voltage from ±8 to ±14 V. The large memory window reveals the high charge trapping efficiency for both electrons and holes.

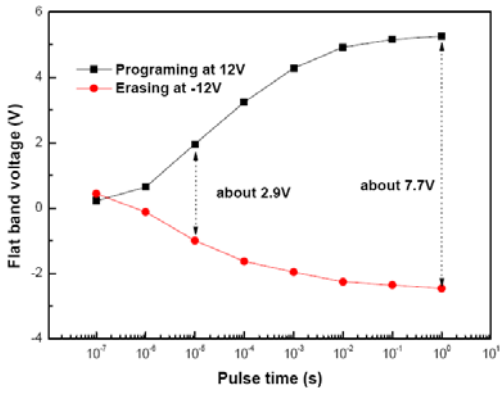

Fig.3 P/E characteristics of the MOS capacitor with Ni-NiO_x core-shell NCs for voltage levels of +12V/−12 V.

The P/E operations were also performed using F-N tunneling method by applying ±12 V pulses on the gate electrode of the devices. Fig. 3 shows the P/E characteristics of the Ni-NiO_x core-shell NCs MOS device. The fully programmed and fully erased states are defined as those that are programmed by a pulse of 12 V, 1 s and erased by a pulse of −12 V, 1 s, respectively. The memory window is +1.9V/-1 V at P/E times 10μs/10μs, respectively, with reference to the standards of nonvolatile memories based on the F-N tunneling regime.

An asymmetric tunnel barrier was formed due to the lower band-gap energy of NiO_x than that of SiO_2. On the basis of these experimental results, the possible energy band diagram of the Ni-NiO_x core-shell NCs embedded in the MOS structure under flatband condition is given in Fig.4 (a).For such an asymmetric tunnel barrier structure, the effective barrier for carrier tunneling can be easily reduced because the NiO_x has a low barrier height that can be fast dragged below the Fermi level of electrons in Si by applying a moderate biasing voltage. Thereby, a relatively high carrier tunneling efficiency can be achieved in both programming and erasing processes, as shown in Fig.4 (b) and (c).Therefore, the P/E speeds were not greatly influenced, although the additional NiO_x interfacial shell oxide layer provides an increased substantial barrier width.

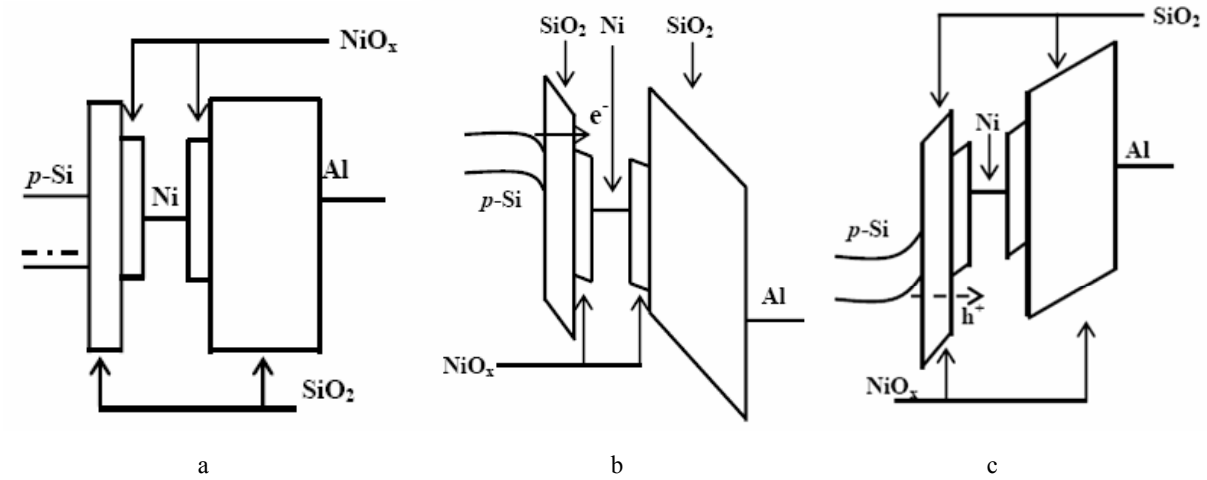

Fig.4 (a) The schematic energy band diagram of the Ni-NiO_x core-shell NCs embedded MOS capacitor with at flatband condition. (b) and (c) shows the band bending profile of this MOS structure under programming , erasing gate voltage, respectively.

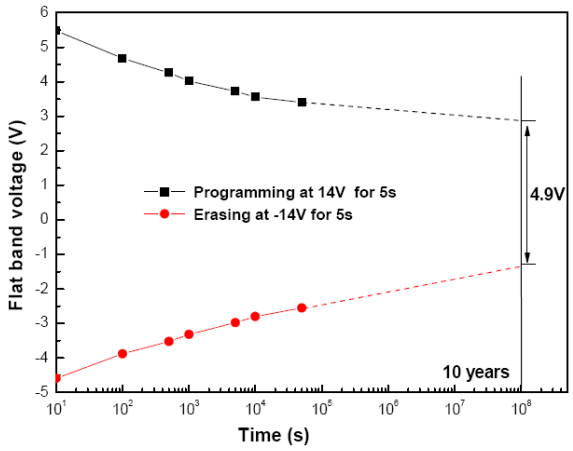

Fig.5 Retention characteristics of the MOS capacitor with Ni-NiO_x core-shell NCs using ±14V gate voltage stresses for 5 s.

The retention characteristics of the MOS capacitor with Ni-NiO_x core-shell NCs was also investigated at room temperature using ±14V gate voltage stresses for 5s.The flatband voltage shift as a function of duration time is shown in Fig.5.Although a charge loss of 30% have occurred after the early duration of 1000 s, the decay rate has slowed down for the rest of the measuring time. Extrapolation of the data up to ten years is also shown in the figure. A large memory window of 4.9 V is estimated to retain even after ten years, which indicates better retention characteristics than that of metal NCs mentioned in prior investigation [19]. Such improved characteristics may be due to the NiO_x shell layer, leading to an increased electron/hole barrier width. We believe that the possible reasons for the improvement in retention may be due to the reduced lateral channel leakage [20] and the Coulomb repulsion in the NCs [21]. Since the NiO_x shell essentially surrounds the spherically shaped metal Ni NCs on the tunneling oxide layer, the lateral leakages through all of the available interfaces might be smaller as long as the NiO_x shell has a sufficiently large additional charge trapping probability due to the enhanced barrier [21].Therefore, the NiO_x shell could improve the retention characteristics at no expense of the program/erase speed. The improvement of retention characteristics indicates the possibilities of using oxidized interface metal shell with NCs in nonvolatile device applications.

In conclusion, the MOS capacitor embedding with Ni-NiO_x core-shell NCs was fabricated. In order to avoid the metal diffusion during high temperature processes, spherically shaped, well isolated, and uniformly distributed Ni-NiO_x core-shell NCs were formed by RTA in N_2/O_2 mixed ambient. Experimental observations of counterclockwise C-V hysteresis curves clearly showed that memory characteristics of the carriers exhibited memory windows of about 10.5 V. The oxidized NiO_x shell layer as providing additional barrier guarantees the charge injection efficiency for program/erase operation due to the lower barrier height of NiO_x. On the other hand, long-term retention characteristics can also be achieved from the comparatively thick asymmetric tunnel oxide composed by NiO_x and SiO_2.Our results reveal that additional barrier, such as a metal oxide shell, is promising for NVM memories

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