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Nano-sized silicon oxide, thermally grown on plasma hydrogenated silicon[♣]

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Oxide layers (~10 nm) grown on rf plasma hydrogenated (100) and (111)Si by thermal oxidation at 850°C are studied using *C-V* and *G-V* measurement techniques, spectroscopic ellipsometry and atomic force microscopy. Analysis of the *G-V* curves revealed the interface traps as single-type defects. In oxides on (111)Si, a triplet P_b centre was found. Higher trap densities were observed for (100)Si. Defects in the Si sub-surface region modified during hydrogenation were detected in the high-frequency range of 200 kHz of the *G-V* curves, and were related to a stressed surface region in the Si substrate. The grown oxide is probably SiO_x, x being dependant on pre-oxidation cleaning. The inter-silicon distance for hydrogenated oxides is about 3.07Å, which suggests a relaxed SiO_2 structure. Hydrogenation of Si at 300°C suppresses the formation of defects. It is suggested that Si hydrogenation has the potential for surface engineering control.

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1. Introduction

As a result of the continuing miniaturization of MOS silicon electronic devices, the oxide thickness lies in the nanometric scale and the properties of the interface to the Si substrate have an increased impact on the device parameters. This intermediate region is formed during silicon oxidation, and its degree of perfection is critical for the device parameters. While, for thicker oxides, the oxygen pressure, substrate orientation and oxidation temperature are the main parameters that determine the oxide and interface quality, for nano-sized oxides the Si wafer cleaning procedures become a key step in obtaining high quality oxides.

Considerable efforts have been devoted to the development of different cleaning procedures [1]. The basic wet cleaning recipes, known as RCA cleaning, have remained almost unchanged since their first introduction in 1965 [2]. RCA cleaning leaves the silicon surface covered with a thin oxide and is usually followed by an HF dip, in order to produce a clean hydrophobic surface. This H-terminated silicon surface offers enhanced stability against oxidation and organic contaminants [3]. However, with continued IC reduction of dimensions, manufacturing control at atomic scales is required, and other non-standard approaches have to be developed [4].

It has been reported that hydrogen plasma removes the native oxide without causing much damage, resulting in a clean silicon surface terminated with hydrogen [5]. Nevertheless, H- plasma treatment causes surface structuring, the roughness depending on the wafer orientation and doping level [6]. The structured surface regions extend into the sub-100 nm scale [7] and contain Si-H bonds, H_2 molecules, and hydrogen induced platelets [8]. Wafer smoothening under plasma hydrogenation [9] has also been reported. The surface retains the structuring, with re-ordering starting at about 800°C, but even at 1000°C the grain boundaries are still observable [7]. These effects depend on the crystallographic orientation of the Si surface.

In our research, we have applied H-plasma treatment as a pre-oxidation step after wet RCA cleaning, with the aim of obtaining a hydrogenated surface region. The proposition is that silicon hydrogenation offers a twofold advantage: firstly the oxidation rate can be increased, and secondly the post-oxidation anneals, both high and low temperature, are unnecessary. H-plasma exposure can affect the interface parameters, and this point needs further clarification. In the present paper, the defects located at the interface oxide/Si (interface traps), those and deeper into the Si substrate (bulk traps) are studied. The relation of the defects to the oxide structure and composition is discussed.

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2. Experimental

Oxides with a thickness below 10 nm were grown on rf plasma hydrogenated (100) and (111) Si, by thermal oxidation at 850°C in dry O_2 ambient. The Si wafers were cleaned using a standard RCA procedure (H_2SO_4/H_2O_2 solution followed by a dip in diluted HF and a rinse in de-ionized H_2O). Some of the substrates were subsequently exposed to a rf hydrogen plasma in a planar plasma unit. The gas pressure was 133 Pa. The rf generator (13.56 MHz, 15 W input power) was capacitively coupled to the reactive chamber. The substrates were kept on the lower electrode for 15 min, without heating or at 300°C.

The oxidation was performed in the same oxidation run for all substrates, RCA cleaned and plasma exposed. The RCA cleaned samples only served for comparison, to reveal the possible advantages of the plasma cleaning technology.

For electrical characterization, 1.96×10^{-3} cm^2 Al dots on the oxide surface and an Al film on the Si back-side were deposited by evaporation, to form a MOS structure. Electrically active defects were examined by analysis of the room temperature capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) characteristics (frequency range 1 - 300 kHz). The measurement unit was a Precision Component Analyzer Wayne-Kerr 6425. The densities of the interface traps D_{it} were inferred from standard HF *C-V* and the bulk traps from *G-V* analysis, respectively [10].

Information about the oxide and interface region to the Si was gained using a Rudolf Research spectroscopic ellipsometer, in the wavelength range 280-820 nm, at an incidence angle of 70º. The accuracies of the thickness and refractive index determinations were ± 0.2 nm and ± 0.002, respectively.

3. Results and discussion

Plasma exposure modifies the Si surface [9], and the structured surface contains defect sites [6, 7]. Previous results showed that the surface morphology of (100) Si surface was maintained upon growth of thin oxide, indicating the conformity of the oxidized surface to the underlying substrate [9]. The defects remained on the surface even after high temperature treatment [7] and thus can represent defects in the interface region between Si and the oxide.

In Fig. 1, *G-V* plots for oxides on Si(111) and Si(100) reveal the presence of multiple peaks in the oxides grown on unheated hydrogenated Si. For (111)Si, the peaks are less intense compared to the oxides on (100)Si, indicating fewer interface traps, which is unusual and contrary to results from the *C-V* analysis. The higher trap concentrations for (100) Si may be due to the contribution of bulk traps [11], i.e. traps that reside in the space charge region in the Si substrate, detectable only by the *G-V* technique. Precursor sites of the bulk traps, such as hydrogen-terminated Si vacancies (VH_X), can be produced by the hydrogenation in the vicinity the Si surface [12]. The concentration of VH_X centres was found to depend strongly on the crystallographic orientation of the Si surface in the order Si(111) < Si(100). The bulk traps manifest their presence as peaks in G/ω versus ω curves, with positions independent of the gate voltage, as shown in Fig. 2. They were observed only in oxides on Si, plasma hydrogenated without heating, and responding at 200 KHz, a frequency substantially higher than for interface traps [11].

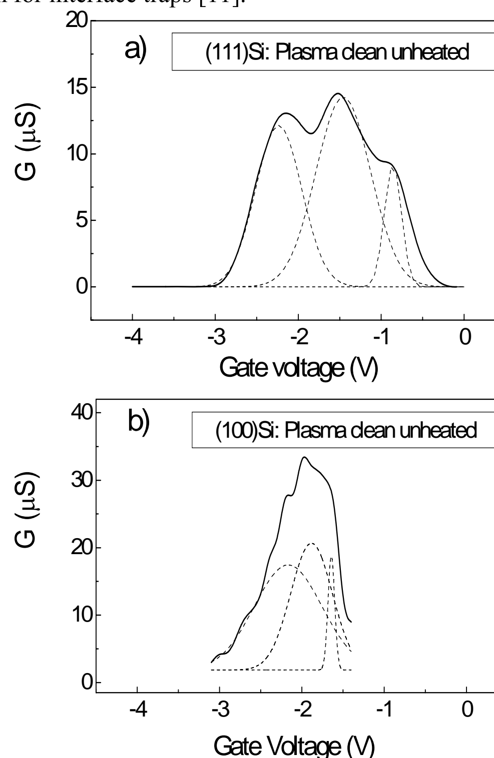

Fig.1. G-V curves for MOS structures on (111)Si (a) and (100)Si (b) cleaned unheated in H-plasma.

Precursors for traps on the plasma induced nano-structured Si surface that survive oxidation were inferred from AFM results [9]. This is also consistent with an ellipsometric study, from which a stressed region in the Si substrate was established, with a stress level of 6.1×10^9 dyn/cm^2 [13]. Strained chemical bonds are known to cause trapping sites. The bulk centres were not observed in oxides grown on Si hydrogenated at 300°C. The implication is that the generation of precursors during plasma exposure is suppressed by the increased temperature. If we regard the plasma influence as a competition process of simultaneous generation and annealing of traps, it seems that in this case the annealing prevails.

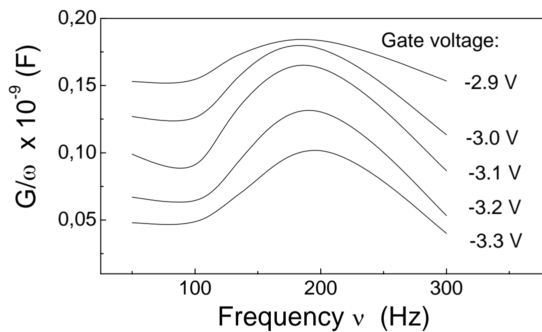

Fig. 2. Frequency dispersion of the conductance of MOS structures on hydrogenated (111)Si.

Interface trap levels at different energetic positions in the Si bandgap were also identified from analysis of the HF *C-V* characteristics (not shown here). The results for oxides on (111)Si are summarized in Fig. 3, together with *G-V* data. The *G-V* results show single levels at same energetic positions, but the time constants are different in oxides on RCA Si and Si hydrogenated without heating. Their densities are lower than those from *C-V* analysis, probably because the *C-V* simultaneously detected all traps with the different time constants.

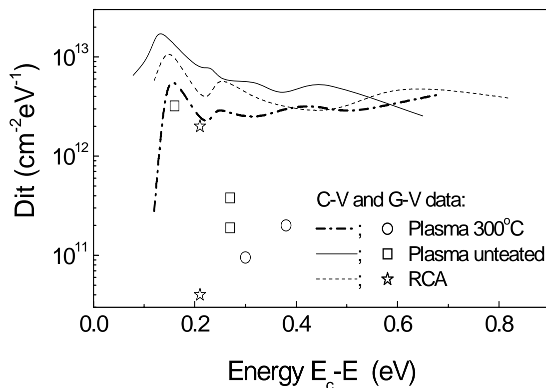

Fig. 3. Interface trap densities for MOS structures on (111)Si, from C-V and G-V measurements.

Usually, the levels corresponding to interface traps in the Si bandgap are ascribed to P_b centers, i.e. dangling Si bonds (• Si ≡ Si_3) at the oxide/Si interface [14-16]. It is well established that on (100)Si, a twofold P_b centre, i.e. P_{b0} and P_{b1}, and a single P_b centre on (111)Si, are present [14]. In our case however, a triplet level is clearly seen. An explanation of a trap on (111)Si due to a double P_b centre with two different time constants was also suggested by other authors [15, 16]; actually, in a magnetic field a triplet structure was observed [16]. Although the oxides were either with thicknesses well above 100 nm [15] or, for native oxides [16], the results could refer to our case. On (100)Si, the P_{b0} is a dangling Si bond with three Si back bonds (• Si ≡ Si_3), while the structure of the P_{b1} center has remained controversial for a long time, and was first ascribed to dangling Si bonds with two Si and one O back bonds [14]. Recent studies [17] have confirmed the suggestion for the P_{b1} to be a Si dangling bond in a strained Si-Si dimer configuration [18]. In any case, the P_b densities for 300°C hydrogenated Si are smaller than those in RCA oxides.

Border traps were also observed in oxides on Si hydrogenated without heating. Although not discussed in detail here, it should be noted that such traps are located within about 3 nm of the interface with the oxide. Therefore, the presence of border and bulk traps indicates a relatively wide transitional region at the oxide/Si interface. Modeling this interface by ellipsometry [19] showed an interface width of about 1 nm. This value amounts to about 10 % of the whole oxide thickness. Even if we consider the rest of the layer as SiO_2, the oxide as a whole will be SiO_x, with x varying along with the pre-oxidation clean.

Further insight into the different oxide structures, depending on the Si surface pre-oxidation state, can be gained from refractive index measurements.

The refractive index was calculated either considering the structure as consisting of Si/oxide (one-layer model) or modeling the structure as Si/interface/oxide (two-layer model [19]). The results are summarized in Table 1, together with data for the oxide roughness.

Whichever model we take, the refractive index of the oxide is higher than that typical for the relaxed SiO_2 layer grown thermally at high oxidation temperatures. This presents further evidence that the oxide can be characterized as SiO_x, with x varying according to pre-oxidation conditions. A higher refractive index is an indication of a stressed oxide. Modeling the distribution of the Si-O-Si bond angles from IR spectra analysis revealed a narrow distribution (145°-147°) of bridging oxygen angles θ in the oxide lattice for hydrogenated Si, while for RCA oxide the distribution was within a wide-angle range (127° - 157°), weighted to the smaller angles [20].

Table 1. Oxide parameters: refractive index and surface roughness.

Si wafer pre-oxidation clean		Refractive index: one-layer model	Refractive index: two-layer model	rms nm
(100) orientation of Si substrate				
RCA		1.66	1.487	0.191
dry	unheated	1.60	1.473	0.261
	300°C	1.69	1.472	0.378
(111) orientation of Si substrate				
RCA		1.58	1.622	0.213
Plasma: unheated		1.46	1.500	0.132
Plasma: 300°C		1.49	1.497	0.407

Since the Si-O bond length r_0 remains nearly constant (1.61 Å), the short-range order of the film structure is characterized by the variation of the inter-silicon distance in the Si-O tetrahedra. The inter-silicon distance can be

obtained from θ and r_0, according to $d_{Si-Si} = 2r_0 \sin(\theta/2)$ [21]. Thus, it distance is about 3.07-3.08 Å for hydrogenated oxides, which tends to the relaxed SiO_2 structure inter-silicon distances of 2.88-3.15 Å. The smaller distance indicates strained bonds that can cause the generation of interface traps.

In Table 1, the roughness of the oxide surface is characterized through the root mean square (rms) value. It is seen that the surface roughness is dependent on the surface hydrogenation, as well as on the substrate orientation. The rms roughness increased with the hydrogenation temperature. However, the rms data are mean values over the investigated area. Actually, the surface is nano-structured with a much smaller roughness, with homogeneously distributed hillocks. We believe that these are the sites that cause the fast oxidation rate in the initial stage of oxide growth, and serve as interface defect precursors.

4. Conclusions

Oxides on hydrogenated Si showed a SiO_x composition and a structure close to relaxed SiO_2. Interface traps due to single defects were detected. The stressed subsurface Si region contained bulk defect sites. The defect density can be controlled through the Si hydrogenation temperature and the Si orientation.

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