Numerical modelling on melt-crystal interface and thermal stress for multi-crystalline silicon grown by directional solidification process

G. ARAVINDAN, M. SRINIVASAN, K. ARAVINTH, P. RAMASAMY*
SSN Research Centre, SSN College of Engineering, Chennai - 603 110, India

Numerical simulation is employed for optimizing the Directional Solidification (DS) process. The temperature distribution, melt-crystal interface, thermal stress are investigated from the numerical simulationduring the cooling process by adjusting the heater temperature of DS furnace. Heat transfer plays an important role in the DS process which controls the thermal stress, dislocation generation and the growth rate of the mc-Si ingot. Here the heat transfer is controlled mainly by the heater temperature adjustment. Our simulation result shows that slightly convex (near to planar) melt-crystal (m-c) interface is achieved up to 0.9 K/h, after that m-c interface changes from convex to concave interface. Thermal stress and dislocation rateof mc-Si ingot are also discussed in this paper.

(Received July 4, 2016; accepted August 9, 2017)

Keywords: Simulation, Directional Solidification Process, Multi-Crystalline Silicon, Melti-Crystal Interface, Thermal stress

1. Introduction

Many researchers work across the world to produce high conversion efficiency solar cells. Electricity is produced by many methods such as crystalline (mono and multi crystalline silicon (mc-Si)) solar cells,thin film solar cells and concentrated PV solar cells [1]. Silicon isthe key material for solar energy production. Now-a-days90 % of PV markets are using silicon solar cells [2]. Silicon crystals are not easily damaged by excess heat. Si material is less expensive due to the greater abundance in nature. The crystalline silicon has advantages such as little maintenance, no supervision, non-polluting, longer life time (20-30 years), it does not require large area installation and it does not require separate area for installation purpose. The single crystalline silicon is more efficient than multi-crystalline silicon, the production cost of single crystalline silicon is very high [3].

Directional Solidification process is a simple and cost effective method for multi-crystalline growth process for PV application and its process is less complex than Cz [2], itreduces the resources cost from the longer production cycle [4]. DS-grown ingots have well-adjusted size with rectangular shape and up scaling of DS is much easier than Cz. The mc-Si grown by DS has defects such as randomly orientated grain boundary, dislocations and impurity. These defects affect the conversion efficiency of solar cells [4, 5].Those defects are controlled by optimization of thermal stress during the DS process. Thermal stress is caused due to higher temperature gradient. The quality of mc-Si ingot is controlled by the DS furnace parameters such as moving the side or bottom insulation along with adjustment of heater temperature, solidification time, gas flow and cooling process. Optimizing of those parameters in a real situation is very difficult and complicated too. Numerical method plays acrucial role for DS process because it helps to understand and optimize the growth process. Here the heat transfer problems are solved by using the finite volume method. The m-c interface has an important role in the mc-Si which affects the quality of grown crystal by the thermal stress and grain growth [4]. Also, it influences the multi nucleation sites on the crucible wall in the DS process [6, 7]. A flat or slightly convex m-c interface is favored for stress reduction [8, 9]. A slightly convex m-c interface pushes the impurities outwards [10]. Also the higher quality of mc-Si ingot enhances the conversion efficiency of the solar cells. Xi Yang et al [11] have numerically investigated the mc-Si by different pulling-down rate of the DS furnace. They found that numerical simulation and experimental results show that a slow pulling-down rate with a small temperature gradient can reduce the thermal stresses in the silicon ingot during the solidification process. The temperature distribution, m-c interface and thermal stress for modified hot zone on DS furnace are investigated in that paper. Temperature gradient is decreased in the modified DS system as m-c interface is convex and thermal stress is low [4].Srinivasan et al [12] have improved mc-Si ingot from bottom grooved DS furnace. Wei. Chen et al have increased mc-Si efficiency by modified DS block thickness and addition of insulation component [13]. Xi Yang et al [14] have improved mc-Si ingot quality from adding conical insulation unit at the bottom of the hot zone. Wencheng Ma et al [15] have increased conversion efficiency by 1.2 % from the addition of side insulation partition block. Carbon, nitrogen and oxygen impurity distribution on the mc-Si ingot was studied by S.G. Nagarajan et al [16] at different

crucible rotation. T.H.T. Nguyen et al have [17] controlled m-c interface by adding the insulation blocks. By spot cooling method T.Y. Wang et al[18] have improved mc-Si ingot. In the present work, we have numerically simulated the effect of cooling rate in the DS furnace for mc-Si growth. The cooling rate was controlled by linear adjustment of heater temperature. From these simulations we have analyzed the thermal stress, m-c interface shape,dislocation rate and temperature distribution in the mc-Si ingot during the directional solidification process. The better cooling rate is found to give good quality mc-Si ingot for PV application.

2. Mathematical model

The thermal stress analysis is analysed using displacement-based thermo-elastic stress model. The governing partial differential equations for momentum balance in an axisymmetric model [5] can be written as,

$$\frac{1}{r}\frac{\partial}{\partial z}(r\sigma_{rr})+\frac{\partial}{\partial z}(\sigma_{rz})-\frac{\sigma_{\phi\phi}}{r}=0 \tag{1}$$

$$\frac{1}{r}\frac{\partial}{\partial r}(r\sigma_{rz})+\frac{\partial}{\partial z}(\sigma_{zz})=0 \tag{2}$$

where σ_{rr}, σ_{zz} and $\sigma_{\phi\phi}$ are normal stresses in the radial, axial and azimuthal directions, respectively, and σ_{rz} is the shear stress. Integrating the above equation in the control volume V of a solid material bounded surface S and substituting the stress-strain equation, we get von Mises stress [8] as

$$\sigma_{von}=(\frac{3}{2}S_{ij}S_{ij})^{\frac{1}{2}} \tag{3}$$

where S_{ij} is the stress deviator

$$S_{ij}=\sigma_{ij}-\frac{1}{3}\sigma_{kk}\delta_{ij}$$

In Alexander-Haasen (AH) model, the creep strain rate and the multiplication rate of the mobile dislocation density can be expressed as follows:

$$N_m=Kk_0(\tau_{eff})^{p+\lambda}\exp(-\frac{Q}{kT})N_m \tag{4}$$

$$\tau_{eff}=\sqrt{J_2}-D\sqrt{N_m} \tag{5}$$

$$J_2=\frac{1}{S_{ij}S_{ij}} \tag{6}$$

$$S_{ij}=\sigma_{ij}-\frac{1}{3}\sigma_{kk}\delta_{ij} \tag{7}$$

where τ_{eff} is Effective stress, k is the Boltzmann constant, T is Absolute temperature in the silicon crystal. N_m is Density of mobile dislocations, S_{ij} is Deviatory stress, J_2 is Second invariant of the deviatoric stress, D-Strain hardening factor, k_0, K, p and λ are material constant [19-20].

3. Model and description

In our simulation investigation is started from the melting stage, by using the Finite Volume Method (FVM). Structured and unstructured grids are used during the simulation. FVM is suitable to solve the structured and unstructured mesh. Schematic diagram of DS furnace is shown in Fig. 1. Left side is shown quadrangular and triangular grids generated to solve the heat conduction, convection and radiation problems. Furnace parts are shown on the right side. DS furnace has silicon melt, silicon crystal, argon, insulation, quartz crucible, heaters, heat exchanger block and steel cover. Inner dimension of the quartz crucible is 87.6 cm× 87.6 cm × 40 cm. Side wall thickness is 1.45 cm and bottom thickness is 1.8 cm. Dimension of the ingot is 87.6 cm × 87.6 cm × 23.3 cm.There are totally 22 blocks. They contain 8528 meshes, quadrangular and triangular. Silicon melt, silicon crystal, heater, heat exchanger block contain structured cells and argon, insulation, crucible and steel cover have unstructured cells. Mesh size of silicon melt, silicon crystal, heater and heat exchange block are corresponding to 0.92929 cm^2, 0.6977 cm^2, 0.4760 cm^2 and 0.89748 cm^2. Grids details are shown in the table 2. Here a transient global numerical simulation has been employed for studying the mc-Si growth process in DS furnace. The simulation was carried out using Crystal Growth Simulator (CGSim) software. Unsteady global simulation was made with time varying temperature profile of heater and side insulation movement. 1685 K temperature was set at the m-c interface. In general the simulation can be done using five simple steps such as designing the geometry of the physical system, defining the material and their physical properties to the system, grid generation for heat transfer problems, defining the boundary conditions and analyzing the output.

A 2-D axisymmetric furnace has been considered for our simulation [21-22]. Triangular and quadrangular grids are generated after designing crucible, heaters, insulators, heat exchanger block and gas tube. Normally a real situation can be simulated based on finite element method, finite difference method, finite volume method and spectral method. Here the heat transfer problems were solved iteratively using finite volume method. The schematic view of DS furnace which is used in our simulation has been shown in Fig. 1. The major assumptions made in our simulation are: (a) The melt was considered as an incompressible Newtonian fluid and the flow was a laminar flow, (b) The effect of gas flow is

negligible [21,23,24]. In the DS process Si_3N_4 coated quartz crucible is used for the growth of mc-Si ingotbecause of high purity and low contamination of silicon [25]. A quartz crucible is supported by graphite susceptor to avoid temperature deformation. The argon gas flows from the top of the crucible. The temperature of silicon at the bottom of the crucible is very low compared to the top of the melt. After the fall of temperature below the melting point of silicon, the crystal starts to grow. To maintain the temperature near to the crucible wall is very important to prevent the seed crystal from melting during the solidification process. Material properties used in our simulation are shown in Table 1. The simulation was carried out in the DS process for different cooling rate by linearly adjusting the heater temperature in steps of 0.1 K/h from 0.1 to 2 K/h. The results presented here are for0.1 K/h (case a), 0.3 K/h (case b), 0.6 K/h (case c), 0.9 K/h (case d), 1.2 K/h (case e) and 1.5 K/h (case f).

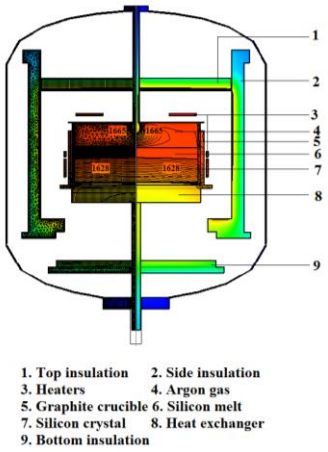

Fig. 1. Schematic view of DS furnace.

Table 1. Material properties.

Material	Properties	Values	Units
Argon	Heat conductivity	0.01	W m^{-1} K^{-1}
	Heat capacity	521	J kg^{-1} K^{-1}
	Dynamic Viscosity	$P(T)=8.466\times10^{-6}+5.365\times10^{-8}$ T-$8.682\times10^{-12}T^2$	Pa S
Graphite	Heat conductivity	$P(T)=146.8885-0.17687T+0.000127T^2-4.6899\times10^{-008}T^3+6.665\times10^{-012}T^4$	W m^{-1} K^{-1}
	Emissivity	0.8	
	Density	1950	kg m^{-3}
	Heat capacity	710	J kg^{-1} K^{-1}
Insulation	Heat conductivity	0.5	W m^{-1} K^{-1}
	Emissivity	0.8	
	Density	500	kg m^{-3}
	Heat capacity	100	J kg^{-1} K^{-1}
Quartz	Heat conductivity	4	W m^{-1} K^{-1}
	Emissivity	0.85	
	Heat capacity	1232	J kg^{-1} K^{-1}
	Density	2650	kg m^{-3}
Steel	Heat conductivity	15	W m^{-1} K^{-1}
	Emissivity	0.45	
	Heat capacity	1000	J kg^{-1} K^{-1}
	Density	7800	kg m^{-3}
Si Melt	Heat conductivity	66.5	W m^{-1} K^{-1}
	Emissivity	0.3	
	Density	P(T)=3194-0.3701T	kg m^{-3}
	Melting Temperature	1685	kg m^{-3}
	Surface tension	0.7835	N m^{-1}
	Dynamic viscosity	0.0008	Pa S
	Heat capacity	915	J kg^{-1} K^{-1}
	Wetting angle	11	Deg

Material	Properties	Values	Units
	Latent Heat	1800000	J kg^{-1}
Si crystal	Heat conductivity	P(T)=110.6122042-0.1507227384T+0.0001093579825T^2-4.009416795×$10^{-008}T^3$+5.66839358×$10^{-012}T^4$	W m^{-1} K^{-1}
	Emissivity	P(T)=0.9016-0.00026208T	
	Density	2530	kg m^{-3}
	Latent Heat	1800000	J kg^{-1}
	Heat capacity	1000	J kg^{-1} K^{-1}

Table 2. Grids details

Block Name	Number of Blocks	Total number of mesh	Type of grid
Silicon melt	1	990	Structured
Silicon crystal	1	225	Structured
Argon	1	1083	Unstructured
Insulation	4	3032	Structured & Unstructured
Steel Cover	4	949	Structured & Unstructured
Heater	3	117	Structured
Heat exchanger block	1	517	Structured
Quartz crucible	1	299	Unstructured
Crucible Stand	3	949	Structured & Unstructured
Top Cover	3	367	Structured & Unstructured

4. Result and discussion

4.1. Temperature distribution

During the mc-Si growth process to control the temperature distribution inside the furnace isimportant, because it affects the quality of mc-Si ingot. The crystal starts to grow at the place of maximum temperature gradient with preferred silicon lattice growth direction [2].If temperature difference in the crystal is high it will induce the stress. During the simulation heat transfer is controlled by heater and side insulation movement. Our ultimate aim is to optimize for the suitable cooling rate by the linear adjustment of heater temperature. Here heater temperature was adjusted in six different cases.Figure 2a showstemperature profile of center of side top heater in the DS furnace at different cases during the solidification process. In all cases side insulation movement is same (0.2 mm/min up to 200 mm, after that kept constant until end of the solidification). Initially simulation starts with silicon at the melt stage. First five hour the furnace is kept at 1700 K for stabilization of silicon melt. Then the furnace is cooled at different cooling rate by adjustingthe heatertemperature.The temperatureof the bottom position at the center of crucible as given by CGSim is shown fig. 2b.

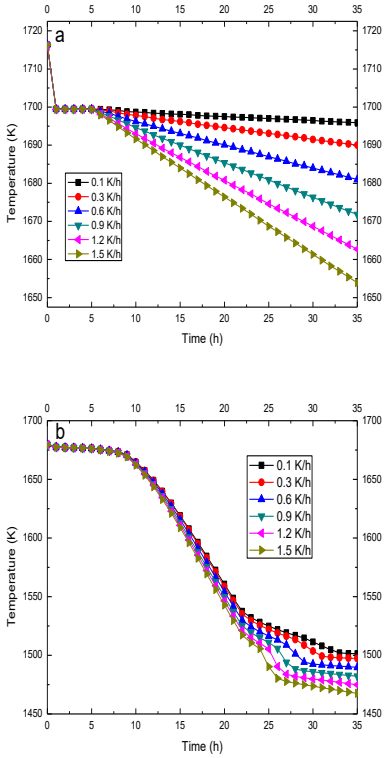

Fig. 2. Temperature profile of DS furnace during the solidification process (a) Top of side heater, (b) Center position in bottom of graphite crucible.

4.2. Melt-crystal interface

In mc-Si growth process m-c interface is important because of its effect on the thermal stress of mc-Si ingot. A convex melt-crystal interface pushes the metal impurities to the corner of mc-Si ingot during the DS process [2]. Fig. 3showsmelt-crystal interface of mc-Si ingot at different solidification fraction (25 %, 50 %, 75 % and 100 %) in sixdifferent cases 2a, b, c, d, e, and f corresponding to the six different cooling rates. It is drawn betweendistancefrom the center toperipheralversus crystal height of the ingot. In this fig. 3 m-c interface of all cases isnearly planar up to 400 mm at25 % of solidification

fraction and it is slightly concave m-c interface nearer to the crucible wall. Similarly for 50 % of solidification fraction the m-c interface is planar up to case d and it changes to concave shape for the case e and f. At 75 % of solidification fraction the convex m-c interface is obtained from case a to case c.Planar m-c interface is obtained for case d.Concave m-c interface is observed for case e and case f. m-c interface at the end of solidification is also shown. From the simulation result investigation the suitable temperature gradient is maintained up to case d (0.9 K/h).Z. Wu et al [23] have studied m-c interface and thermal stress for different side insulation partition movement. They analyzed five different side insulation partition movements. Slow-fast insulation partition movement resulted in flattest m-c interface and lowest thermal stress. Slow-fast insulation partition movement experiment resulted in high conversion efficiency and more vertical grain growth compared to conventional grown mc-Si ingot. In our case m-c interface is controlled by the heater temperature adjustment, flattest m-c interface and lowest thermal stress obtained in the case d. Guoqiang Lv et al [26] have studied experiment and simulation studies of m-c interface and thermal stress of mc-Si ingot. They control the m-c interface by the different pulling down rates, particular pulling down rate has suitable m-c interface and lower thermal stress.

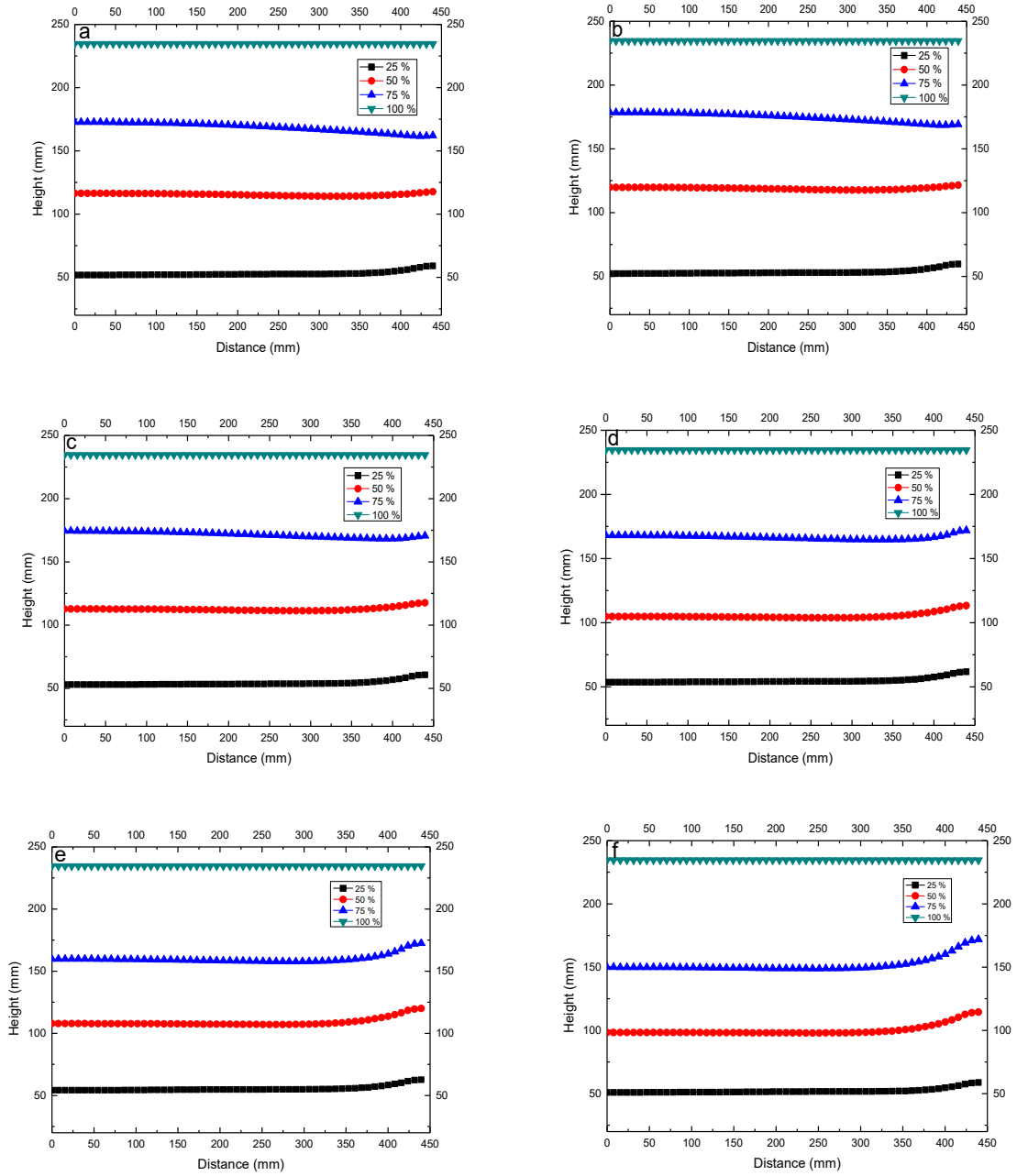

Fig. 3. Melt-Crystal interface of mc-Si ingot.a, b, c, d, e and f correspond to the 0.1 K/h, 0.3 K/h, 0.6 K/h, 0.9 K/h, 1.2 K/h and 1.5 K/h with different solidification fraction (25 %, 50 %, 75 % and 100 %).

4.3. Thermal Stress

Thermal stress of mc-Si ingot mainly depends on the m-c interface of mc-Si ingot during the DS process. The thermal stress will induce the generation of defects in mc-Si ingot. Therefore optimization of thermal stress is crucial in mc-Si growth process. Fig. 4 shows thermal stress (right side) and temperature distribution (left side) of mc-Si ingot at the end of the solidification. Fig. 4a, b, c, d, e and f are corresponding to the case a, b, c, d, e and f. At the end of the solidification time we observed 3.2E5, 4.9E5, 7.5E5, 5.7E5,6.3E5and 9E5 Pa maximum thermal stress corresponding to the case a, b, c, d, e and f. The thermal stress is mainly affected by the m-c interface. To increase the cooling rate the thermal stress also increases. But in the case d the thermal stress is reduced due to change of m-c interface shapes. V. Ganapati et al [27] experimentally analysed stress of mc-Si wafer by using the birefringence imaging, from the analysis they calculated stress in the order of MPa (24 MPa). S. K. Arguirova et al [28] experimentally studied mc-Si sample stress by using the Raman measurement, they calculate stress in the order of MPa (50 MPa). Olga V. Smirnova et al [20] studied different cooling process of DS process and compared experimental results, they obtained von Mises stress in the order of 0.1 MPa to 1 MPa.

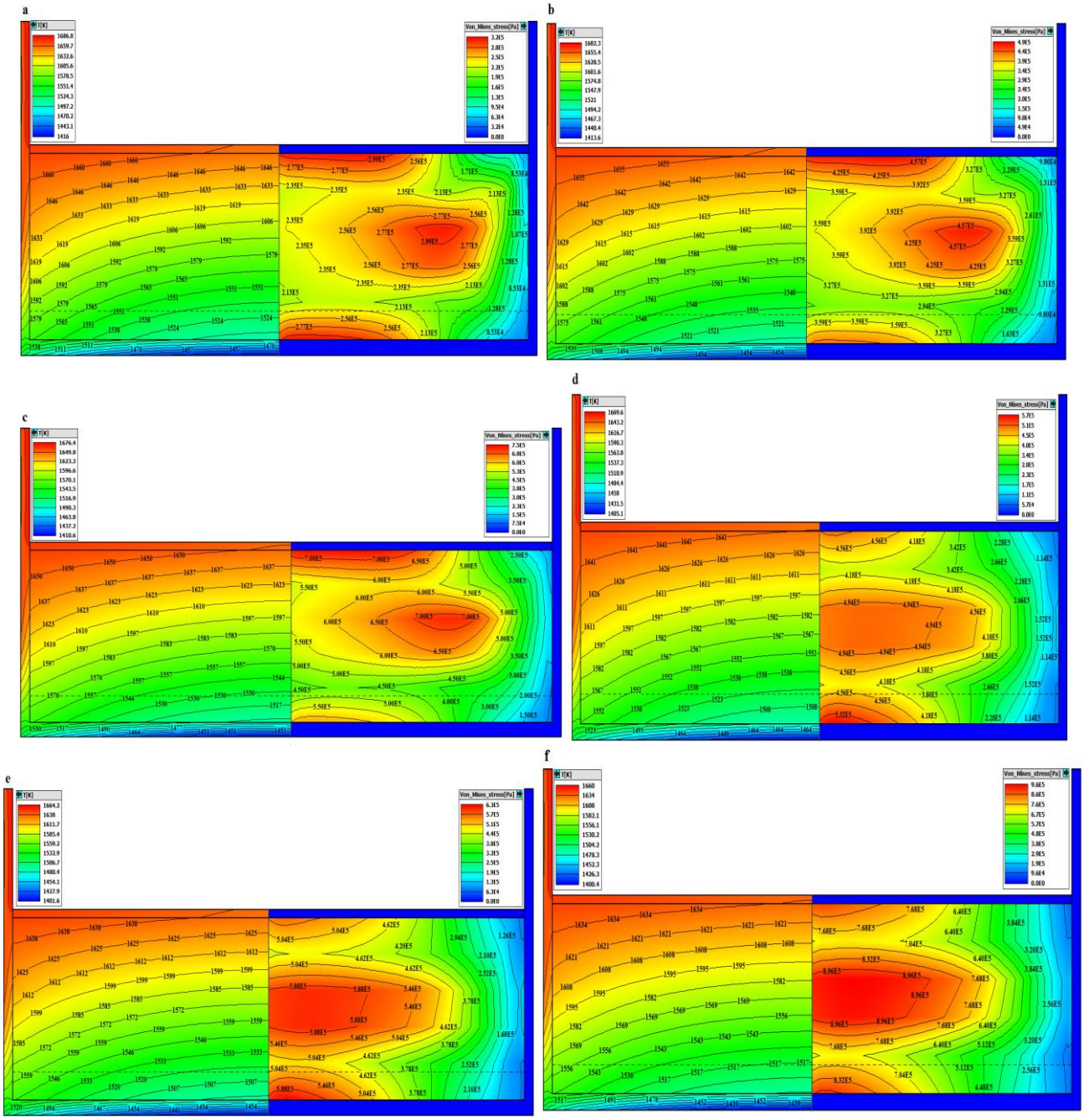

Fig. 4. Thermal stress of mc-Si ingot at the end of the solidification a, b, c, d,e and f are corresponding to the 0.1 K/h, 0.3 K/h, 0.6 K/h, 0.9 K/h, 1.2 K/h and 1.5 K/h.

4.4. Dislocation rate

The conversion efficiency mainly depends on dislocations of mc-Si ingot grown by DS process. Dislocation rate is affected by the thermal stress. Dislocations increase due to mismatching of thermal coefficient of crucible and silicon ingot [2]. Fig. 5 shows dislocation rate of mc-Si ingot at the end of the solidification a, b, c, d, e and f, corresponding to the case a, b, c, d, e and f. At the end of the solidification time we observed maximum dislocation rate of 2.5E3, 6.5E3, 1.6E4, 6.6E3, 9.3E3 and 2.5E4 (1/s/m^2) corresponding to the case a, b, c, d, e and f. The generation of dislocation increases up to case c, decreases for case d, after that increases. The dislocation rate mainly depends on the thermal stress. It means the thermal stress increased after case d. It revealed that the dislocation rate is increased linearly due to increased cooling rate. The dislocation rate decreases due to lower thermal stress in the case d. Graphical diagram of maximum thermal stress and dislocation rate at different cooling rate are shown in fig 6.

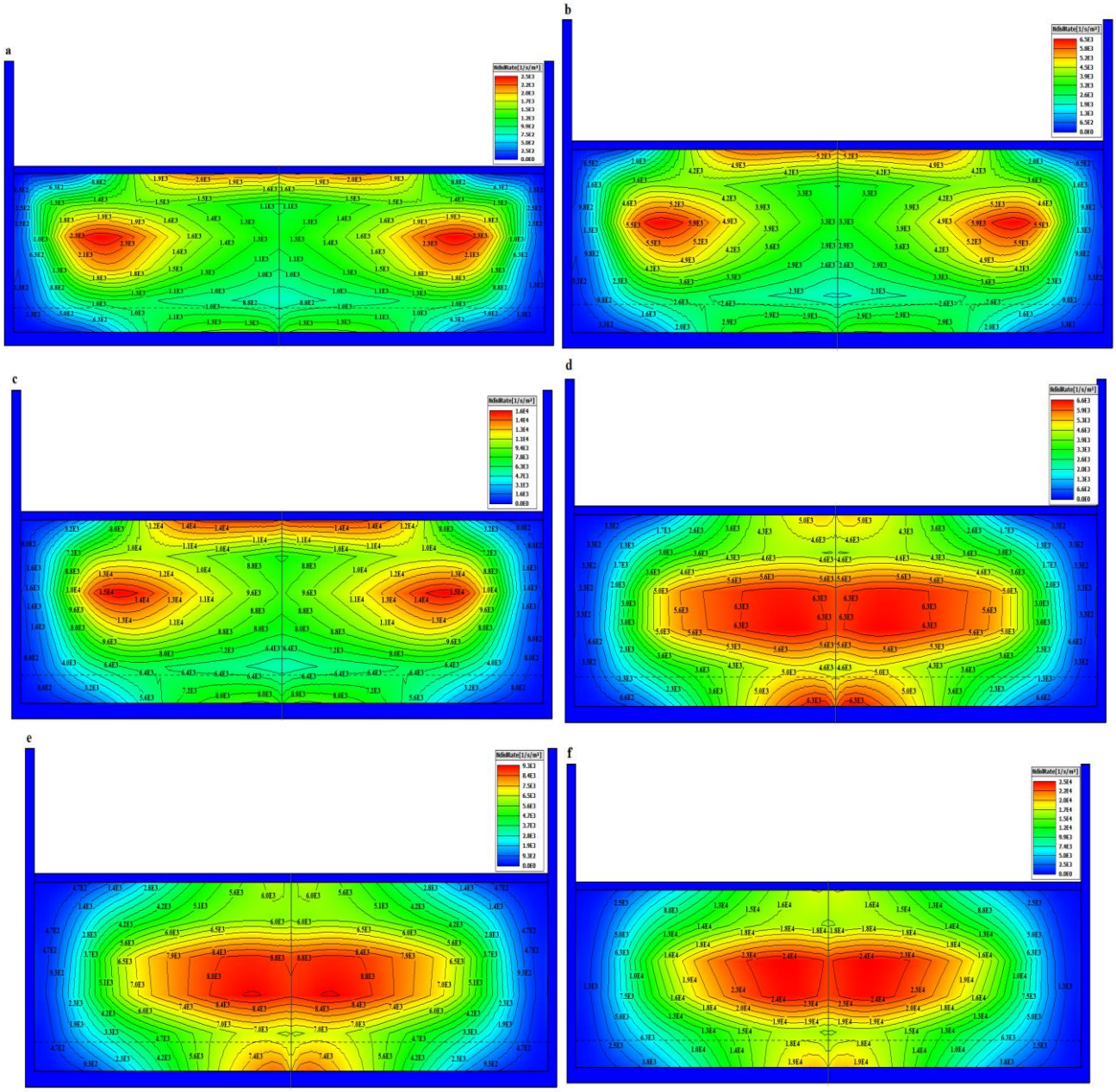

Fig. 5. Dislocation rate of mc-Si ingot at the end of the solidification a, b, c, d, e and f are corresponding to the 0.1 K/h, 0.3 K/h, 0.6 K/h, 0.9 K/h, 1.2 K/h and 1.5 K/h.

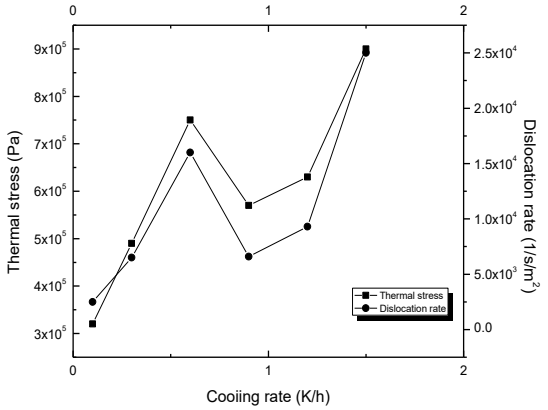

Fig. 6. Maximum thermal stress and dislocation rate of mc-Si ingot at the end of the solidification for different cooling rates (0.1 K/h, 0.3 K/h, 0.6 K/h, 0.9 K/h, 1.2 K/h and 1.5 K/h).

5. Conclusion

mc-Si has an important role in PV application, it is grown in the directional solidification process. In a real situation during the solidification process so many difficulties arise to optimize the furnace parameter. The numerical simulation is the best tool for optimization to get good quality mc-Si ingot and helps to understand the DS process. We have studied different cooling rate by adjusting the temperature from heater. The m-c interface is slightly convex for smaller cooling rate, nearly planar for 0.9 K/h and concave for higher cooling rate. From the simulation results, during the mc-Si growth process cooling rate (temperature adjustment from the heater) 0.9 K/h gives most desirable results. This result may be useful to grow better mc-Si ingot for PV application.

Acknowledgements

This work was supported by the Ministry of New and Renewable Energy (MNRE), the Government of India (Order no: 31/58/2013-2014/PVSE & 15-01-2015).

Reference

[1] A. M. Bagher, M. M. Abadi Vahid, M. Mohsen, American Journal of Optics and Photonics **3**, 94 (2015).
[2] B. Wua, N. Stoddarda, R. Mab, R. Clarka, Journal of Crystal Growth **310**, 2178 (2008).
[3] H. Fang, Q. Zhang, Y. Pan, S. Wang, N. Zhou, L. Zhou, M. Lin, Journal of Thermal Stresses **36**, 947 (2013).
[4] X. Yang, W. Ma, G. Lv, K. Wei, T. Luo, D. Chen, Journal of Crystal Growth **400**, 7 (2014).
[5] H. S. Fang, S. Wanga, L. Zhou, N. G.Zhou, M. H. Lin, Journal of Crystal Growth **346,** 5 (2012).
[6] H. Miyazawa, L. Liu, K. Kakimoto, Journal of Crystal Growth **310**, 1142 (2008).
[7] C. Hauler, G. Stollwerck, W. Koch, W. Krumbe, A. Müller, D. Franke, T. Rettelbach, Advance Materials **13**, 1815 (2001).
[8] X. J. Chen, S. Nakano, L. J. Liu, K. Kakimoto, Journal of Crystal Growth **310**, 4330 (2008).
[9] C. E. Chang, W. R. Wilcox, Journal of Crystal Growth **21**, 135 (1974).
[10] Q. Yu, L. Liu, W. Ma, G. Zhong, X. Huang, Journal of Crystal Growth **358**, 5 (2012).
[11] X. Yang, W. Ma, G. Lv, K. Wei, C. Zhang, S. Li, D. Chen, Metallurgical and Materials transactions e**2E**, 39 (2015).
[12] M. Srinivasan, P. Karuppasamy, P. Ramasamy, A. K. Barua, Electron Materials Letter **12**(4), 431 (2016).
[13] W. Chen, Q. Wang, D. Yang, L.D. Li, X.G. Yu, L. Wang, H. Jin, Journal of Crystal Growth **467**, 65 (2017).
[14] X. Yang, W. Ma, G. Lv, K. Wei, T. Luo, D. Chen, Journal of Crystal Growth **400**, 7 (2014).
[15] W. Ma, G. Zhong, L. Sun, Q. Yu, X. Huang, L. Liu, Solar Energy Materials & Solar Cells **100**, 231 (2012).
[16] S. G. Nagarajan, M. Srinivasan, K. Aravinth, P. Ramasamy, International Journal of Materials Research **107**, 1 (2016).
[17] T. H. T. Nguyen, S. H. Liao, J. C. Chen, C. H. Chen, Y. H. Huang, C. J. Yang, H. W. Lin, H. B. Nguyen, Journal of Crystal Growth **452**, 27(2016).
[18] T. Y. Wang, S. L. Hsu, C. C. Fei, K. M. Yei, W. C. Hsu, C. W. Lan, Journal of Crystal Growth **311**, 263 (2009).
[19] S. Nakano, X. J. Chen, B. Gao, K. Kakimoto, Journal of crystal Growth **318**, 280 (2011).
[20] O. V. Smirnova, V. M. Mamedov, V. V. Kalaev, Crystal Growth & Design **14**, 5532 (2014).
[21] K. Kakimoto, H. Matsuo, S. Hisamatsu, B. Ganesh, G. Bing, X. J. Chen, L. Liu, H. Miyazawa, Y. Kangawa, Solid State Phenomena **156-158**, 193 (2010).
[22] C. Ding, M. Huang, G. Zhong, L. Liu, X. Huang, Crystal Research Technology **49**, 405 (2014).
[23] Z. Wu, G. Zhong, Z. Zhang, X. Zho, Z. Wang, X. Huang, Journal of Crystal Growth **426**, 110 (2015).
[24] C. Ding, M. Huang, G. Zhong, L. Ming, X. Huang, Journal of Crystal Growth **387**, 73 (2014).
[25] C. W. Lan, C. Hsu, K. Nakajima, Multicrystalline Silicon Crystal Growth for Photovoltaic Applications, Ch 10 Hand book of crystal growth.
[26] G. Lv, D. Chen, X. Yang, W. Ma, T. Luo, K. We, Y. Zhou, Vacuum **116,** 96 (2015). .
[27] V. Ganapati, S. Schoenfelder, S. Castellanos, S. Oener, R. Koepge, A. Sampson, M. A. Marcus, B. Lai,H. Morhenn, G. Hahn, J. Bagdahn, T. Buonassisi, Journal of Applied Physics **108**, 063528 (2010).
[28] S. K. Arguirova, W. Seifert, M. Kittler, J. Reif, Materials Science and Engineering **B102**, 37 (2003).

*Corresponding author: ramasamyp@ssn.edu.in