On a numerical simulation of current-voltage features in wide range of temperature in metal/silicon Schottky diodes

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In this work, the current-voltage behavior of metal/silicon Schottky structures is investigated numerically. The forward bias lnI-V plots for different values of series resistance R_s (0, 20, 50, 150 Ω) in various temperatures (40-300 K) are simulated using the iteration method. In this simulation, gold metal and n-type silicon semiconductors have been considered as contact and semiconductor interfacial materials. This type of Schottky structure is called a Schottky barrier diode. Comparison of electrical properties of Au/n-Si Schottky diodes and ideal Schottky diodes (SDs) indicates an abnormal behavior. The results show a crossing/intersection behavior at R_s=0. Considering the intersection points of each curve with other curves, it is clear that the slope of lnI-V plots is autonomous of temperature. The linear relation between voltage and current for R_s=0 show that the current or conductivity increases with the rise in temperature before the intersection region and then begins to decrease. Such a decrease in current despite the rise in temperature after intersection point is in nonconformity with the presented positive temperature coefficient of current. On the other hand, there isn't any intersection behavior in the lnI-V plots for R_s>0 and these plots begin to deviate from linearity for each temperature. The intersection of these curves is hidden and unobservable in homogeneous SDs because of the existence of series resistance. Arrhenius plots for R_s=0 and 150 Ω were also drawn and they show that the slope of these plots which is corresponding activation-energy (E_a) decreases with increasing voltage which indicated the E_a value is dependent on bias voltage as well as temperature. The enlarged view of the confluence region represents that the intersection of a pair of plots occurring at the varied voltage for various temperatures as almost $qV_i=\Phi_B+2KT/q$.

(Received May 13, 2021; accepted November 24, 2021)

Keywords: Schottky diodes (SDs), Numerical Simulation, Series resistance effect on the intersection behavior forward bias I-V plots, Voltage dependent activation energy

1. Introduction

There are several methods for the preparation of metal-semiconductor (MS) and metal-interlayer-semiconductor (MIS) type SDs such as thermal evaporation electron beam and sputtering coating methods using semiconductor wafers as substrate materials. In the ideal case, these SDs have no perfectly ohmic and rectifying behavior depend on fabrication process, temperature, barrier homogeneity, the level of doping donor or acceptor atoms, the chosen work function metal, and applied bias voltage. The electrical characteristics or conduction mechanisms can be evaluated both experimentally and theoretically. In other words, the use of mathematically based on multi-dimensional numerical models for determining the carrier-transport/conduction mechanism (CTMs) in a wide range of temperature and voltage or electric-field, makes it possible to complement, verify, and explain the available experimental data as accuracy and reliability.

The basic electrical parameters of MS or MIS type SDs are usually obtained from the forward-bias current-voltage (I-V) data by usage standard Thermionic-Emission (TE) theory [1-3]. On the other hand, the use of the I-V data just room temperature does not get us intended information on the conduction-mechanisms (CMs). Therefore, the investigation of CMs in a wide range of voltage and temperature is more important to get accurate and reliable results on these diodes. When these diodes have series resistance which causes the voltage-drop across the diode to be lower than the applied bias voltage. Although, the lnI-V plots in the moderate-voltages show good linear behavior in which the effect of R_s can be neglected low, at towards high bias voltage these plots get out of the linearity state because of the effect of R_s rather than interlayer [4-9]. The existence of a native or deposited oxide/insulator layer on the semiconductor surface has also great importance effects on the I-V plots as well as R_s [10,11].

Although the effects of R_s, surface states (N_{ss}), interfacial layer, and barrier inhomogeneity on the forward bias I-V characteristics of diodes are still working intensively both experimentally and theoretically, it has not been adequately enlightened yet [12-14]. In recently, some researchers have also reported both the experimental and theoretical works on the intersection behavior in the I-V plots of diodes for different temperature values and also the impressed of this behavior by the series resistance [9,15-17]. Among them, Osvald [15], has examined the intersection behavior of I-V curves theoretically and

emphasis that the R_s existence for this observation is an inevitable condition. But, according to Chand [9], the intersection behavior in the I-V plots may be occurred due to the decreasing apparent barrier height (BH) with the reduction in the value of temperature, and the presence of non-zero resistance prevents this intersection from observation in homogeneous SDs. Dökme et al. [16] and, Pakma et al. [17] have also investigate the effect of R_s on the intersection of I-V curves in $Al/SiO_2/p$-Si and $Al/TiO_2/p$-Si (MIS) type diodes, respectively.

While R_s and interfacial layer are effective at enough higher forward bias voltages (non-linear region), the N_{ss} is effective only at intermediate bias voltages. When applied bias voltage (V_a) across the Schottky barrier diode, it will be shared by depletion layer of the diode, interfacial layer and N_{ss} as: $V_a=V_i+IR_s+V_d$. In recently, some researchers showed that the values of R_s, interfacial layer, and N_{ss} lead to significant effects both on the electrical characteristics of SDs with and without an interfacial layer [18-22]. Ö. F. Bakkaloğlu et al. [20] showed that both the values of R_s and N_{ss} decrease with increasing temperature, but the value of BH increases. On the other hand, N. Kumar and S. Chand [22] were observed an intersection behavior in the forward bias lnI-V data at almost a certain bias voltage. After this intersection point of the lnI-V plot, the value of R_s was found to increase with increasing temperature because of the lack of free charge carriers at low temperatures.

In this research, the forward bias I-V characteristics of a MS diode have been analyzed as numerically both in the vast domain of temperature and bias voltage by considering the effect of series resistance and barrier inhomogeneity. Because the analysis of the I-V features at the room or above temperatures cannot give us enough more information both on the CTMs and nature of BH at MS interface. The observed intersection behavior in the forward bias I-V curves for zero value of R_s show the decreasing of apparent BH with the reduction in temperature, and this behavior is retained hidden and unobservable in homogeneous SDs due to presence of R_s.

2. Results and discussion

The value of ideality factor and R_s of the SDs have almost to be unity and closer to zero in the ideal case, respectively. But in application, the situation is maybe considerably different from the ideal case because of the non-zero amount of R_s and barrier inhomogeneities at the M/S junctions [1-9]. Firstly, to investigate the effect of R_s on the current flowing through SDs, the forward bias I-V plots were obtained numerically and given in Fig. 1 (a-d) for the various value of R_s (0, 20, 50, and 150 Ω) by using following relation, respectively [1,2,25]:

$$I(V,\Phi_B) = I_0\left[\exp\left(\frac{q(V-IR_s)}{kT}\right)-1\right]. \quad (1)$$

In Eq.1, I_o is the reverse saturation current for zero bias voltage and given as follow:

$$I_0 = AA^{*}T^{2}\exp\left(-\frac{q\Phi_B}{kT}\right), \quad (2)$$

where the quantities of A, A^*, and T are the SD area ($7.85\times10^{-3}cm^2$), the effective Richardson-constant (112 $A.cm^{-2}$ K^{-2} for electrons in n-Si), and the temperature in Kelvin, respectively. This expression was solved numerically by an iteration procedure between 0 and 1 V used the same barrier height (0.80 eV) for four different R_s values (0, 20, 50, and 150 Ω).

According to Fig. 1(a), the lnI vs V plots in the temperature range of 40-300 K have almost a certain intersection/crossing point at about 0.80 V for R_s=0. The intersection demeanor in the forward bias I-V plots has been also observed by some researchers as theoretically [9,16-24]. Such intersection of lnI-V curves may be originated from different sources such as barrier inhomogeneity, the zero or low value of R_s (Ohmic behavior), the somatic or entrusted an interfacial-layer between metal and semiconductor [15-18].

According to Chand and Osvald, the observed crossing behavior of lnI-V curves is the result of zero-value of R_s which has been kept hidden and unobservable in homogeneous SDs due to existence of R_s [6,7]. On the other hand, according to I. Dökme et al. [16], Pakma et al. [17], and Taşçıoğlu et al. [18], this intersection behavior is the result of the absence of free charge at a low temperature which occurs even at SD with a series resistance and for the different values of temperature between 40-300 K where there is no carrier freezing out. This event is inevitable, particularly at low temperatures.

The current flowing through the barrier-height or diode increases despite decreasing the amount of temperature after the intersection point for higher bias voltages. Such behavior is rather unanticipated and in disagreement with the thermionic-emission (TE) theory in the CTMs. As shown in Fig. 1 (a-c), the slope of the lnI vs V plots decreases with increasing temperature. It is clear that if we extrapolate the linear regime of these plots, they will intersect each other. At the voltage range between 0.8-0.85 V, this extrapolation of the linear part of these curves is equivalent to plotting the lnI vs V plots with the R_s=0 like in Fig. 1 (a). Fig. 2. shows the Arrhenius plots for various voltages at R_s=0 Ω and R_s=150 Ω, respectively.

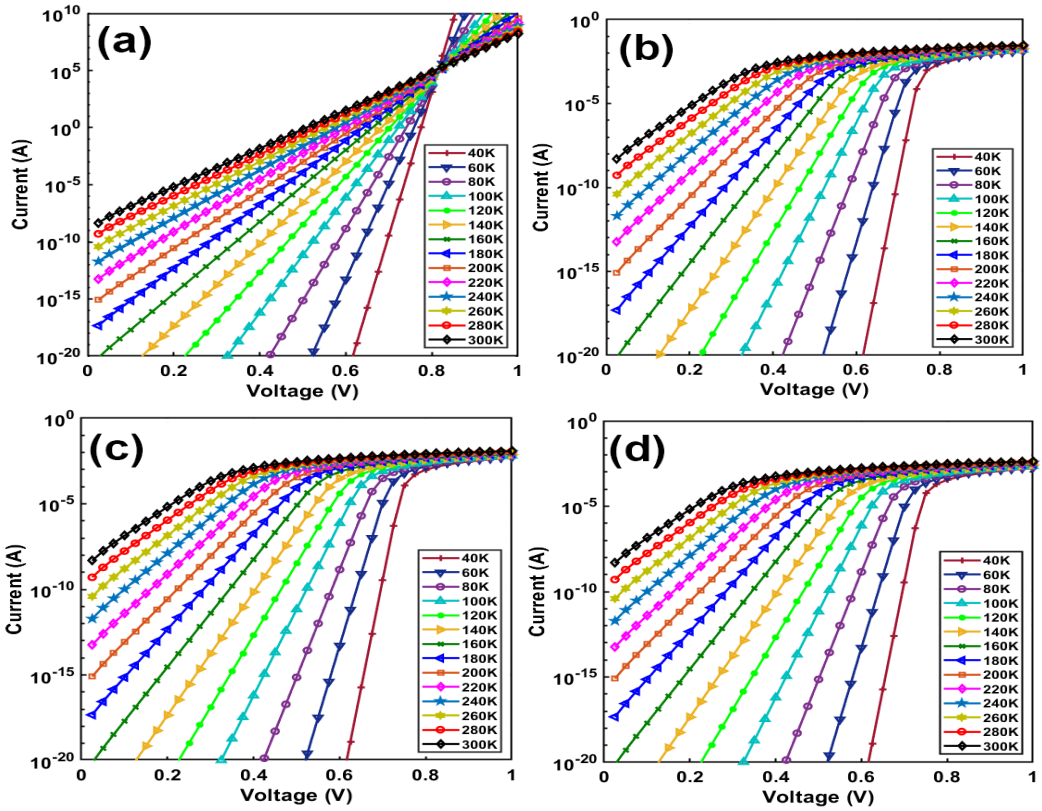

Fig. 1. The forward bias lnI-V characteristics of the SD for R_s =0, 20, 50, and 150 Ω for various values of temperature (40-300 K by 20 K steps) (color online)

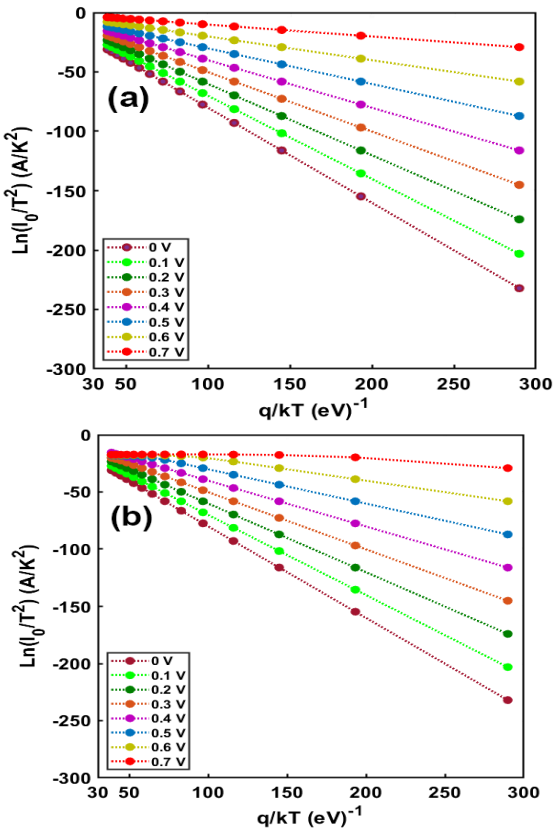

Fig. 2. The Arrhenius plots in the voltage range of 0-0.70 V by 0.1 V steps for various applied bias voltage for; (a) R_s=0 Ω and (b) R_s=150 Ω, respectively (color online)

In order to determine the voltage dependent activation energy (E_a), conventional Richardson or Arrhenius plots for R_s=0 and 150 Ω were also drawn and given in Fig. 2 (a) and (b) by using following relation, respectively [1,2]:

$$\ln(I/T^2) = \ln(AA^*) - \frac{qE_a}{kT}. \quad (3)$$

As shown in these figures, the slope of these plots which is corresponding to E_a decrease with increasing applied bias voltage. This indicated that the value or BH or E_a is also dependent on applied bias voltage as well as temperature is as clearly seen in Fig. 3. The discrepancy in values of E_a becomes increases with an increase in applied bias voltage.

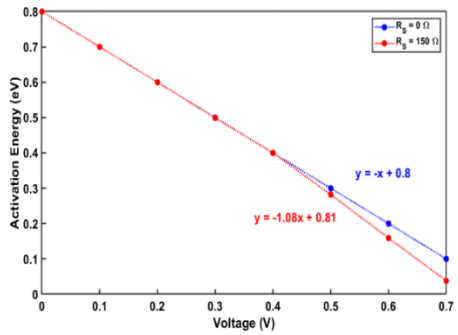

Fig. 3. The Activation energy versus voltage for R_s=0 and 150 Ω in the voltage range of 0-0.70 V by 0.10 V steps, respectively (color online)

When the existence of barrier inhomogeneity between metal and semiconductor, the BH is not homogenous and is represented as a mean BH ($\overline{\Phi_{B_0}}$) depending on the standard deviation (σ_s) [14-17]. In this case, BH is called as an apparent BH (Φ_{ap}) and they are given as follow:

$$\Phi_{ap}(T) = \overline{\Phi_{B_0}} - \frac{q\sigma_s^2}{2kT}. \quad (4)$$

From Fig. 1(a), it can be seen that although the lnI-V plots seem to intersect at the same point, the situation is actually different as depicts in Fig. 4. Fig. 4 shows a magnified view around the intersection point of lnI vs V plots of displayed crossing in Fig. 1(a). It is clear that the values of current and voltage of any pair of lnI-V curves for two different temperatures are the same in the intersection points. Considering this condition on equation (1) implies that the intersection point corresponds to bias as follow:

$$qV_i = \Phi_B + 2kT/q. \quad (5)$$

When the term 2kT/q achieves the eldest value of 0.05 eV for T=300 K or room temperature, the corresponding pair of plots intersect with each other at 0.85 V, which is also apparent from Fig. 4. On the other hand, when BH shows a Gaussian distribution which contains many lower barrier or patches at around mean BH between metal and semiconductor, the crossing point shifts towards to lower bias voltage as follows:

$$qV_i = \Phi_B + \frac{2kT}{q} - \frac{q\sigma^2}{kT}. \quad (6)$$

Here, σ is the standard deviation of BH. Since SD has a Gaussian distribution (GD) of BH based on TE theory, the measured value of Φ_{ap} for any temperature is lower than the mean/average BH (Φ_{av}) V and it decreases with decreasing temperature as $\Phi_{ap}=\Phi_{av}-q\sigma^2/kT$. Therefore, the investigation I-V characteristics of the SD at low ore under room temperature becomes more complicated when compared to room and above temperatures. Because at room and above temperatures, TE theory is usually dominate mechanism, but for low temperatures and high-doped donor or acceptor atoms tunneling mechanisms containing thermionic-field emission (TFE) and field-emission (FE) may be dominated rather than TE theory. Such abnormal behavior and the R_s effect on the forward bias I-V characteristics were also reported by various researchers [26-30].

As a result, in the applications, M/S junction does not a unique or flat barrier, especially at low temperatures. Contrary, there are plenty of big and small barriers in the place of a mean barrier called Pinch-off and this model was proposed by Tung [31]. Werner et al. [32] reached this outcome that the BH was impermanent, and had an average-valued GD with a σ_s autonomous from voltage and temperature. Although the value of BH based on TE is independent of temperature, the essential diode parameters are mighty functions of doping level, temperature, and surface morphology [33-37]. For this reason, the measurement of I-V amounts in an extensive interval of values of temperature and applied voltage and biases is quite considerable.

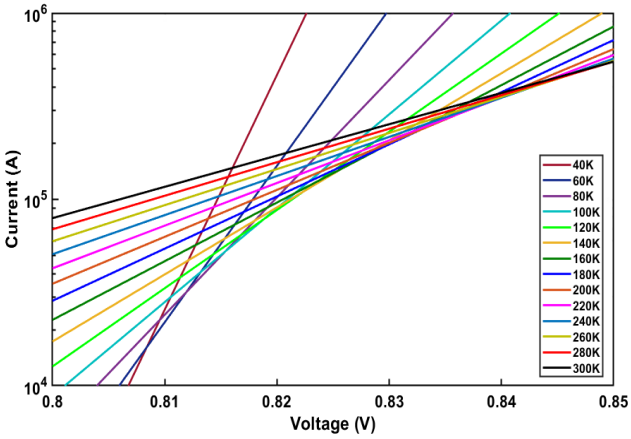

Fig. 4. The enlarged view of Fig. 1(a), around the intersection region of lnI-V curves, indicates that the crossing point of any pair of lnI-V curves for different temperatures occurs at different bias voltages (color online)

The non-ideal behaviour refer to the presence of surface states (N_{ss}), interfacial layer forming native or deposited, the GD of BH (Fig. 5) at M/S interface, and tunneling current via N_{ss} and dislocations in SDs [3,27-31,38]. Therefore, an analytical solution to calculate the BH as function of temperature and voltage recommended by Tung [31,39].

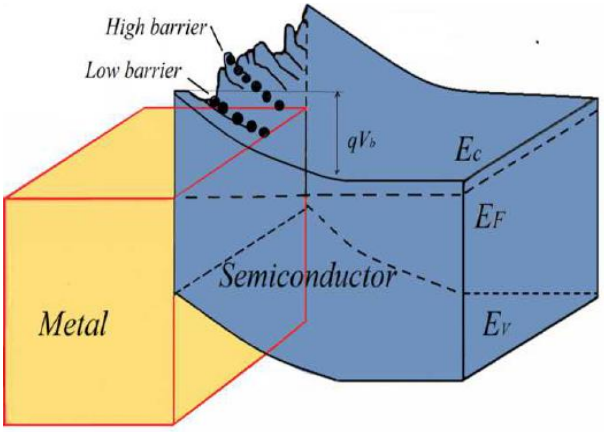

Fig. 5. Gaussian distribution model of BH for SD (color online)

The total current across a Schottky contact including both R_s and barrier inhomogeneities can be expressed as follow [38,39]:

$$I(V) = \int I(V, \Phi_B)\rho(\Phi_B)d\Phi_B, \quad (7)$$

where

$$I(V,\Phi_B) = AA^*T^2 \exp\left(\frac{-q\Phi_B}{kT}\right)\left[\exp\left(\frac{q(V-IR_s)}{kT}\right)-1\right] \quad (8)$$

is the current at any bias voltage for a barrier height (Φ_B), and $\rho(\Phi_B)$ is the normalized distribution function giving the probability of occurrence of barrier height Φ_B. For the case of a GD of BHs with mean value of BH and standard deviation σ, $\rho(\Phi_B)$ is given as follow [38,39]:

$$\rho(\Phi_B) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left(-\frac{(\Phi_B - \overline{\Phi}_B)^2}{2\sigma^2}\right), \quad (9)$$

where $\frac{1}{\sigma\sqrt{2\pi}}$ is the normalization constant.

Thus, the current I(V, Φ_B) for any V for an elementary Φ_B is determined numerically by solving these equations for each temperature for a given R_s using a computer program. It is then multiplied by the probability for that BH, as obtained from Eq. 9 to determine the actual current contribution. Thus, the value of I has been computed for each BH for each voltage and the total current is then estimated by performing the integration Eq. 7 By using Simpson's one-third rule as given Fig. 6 (a-d).

This analytical solution is in good agreement to numerical simulations. Therefore, the lnI-V plots were drawn again by taken into account both the value of R_s and standart deviation (σ) for 100, 200, 300, and 400 K and represented in Fig. 6 (a-d), respectively.

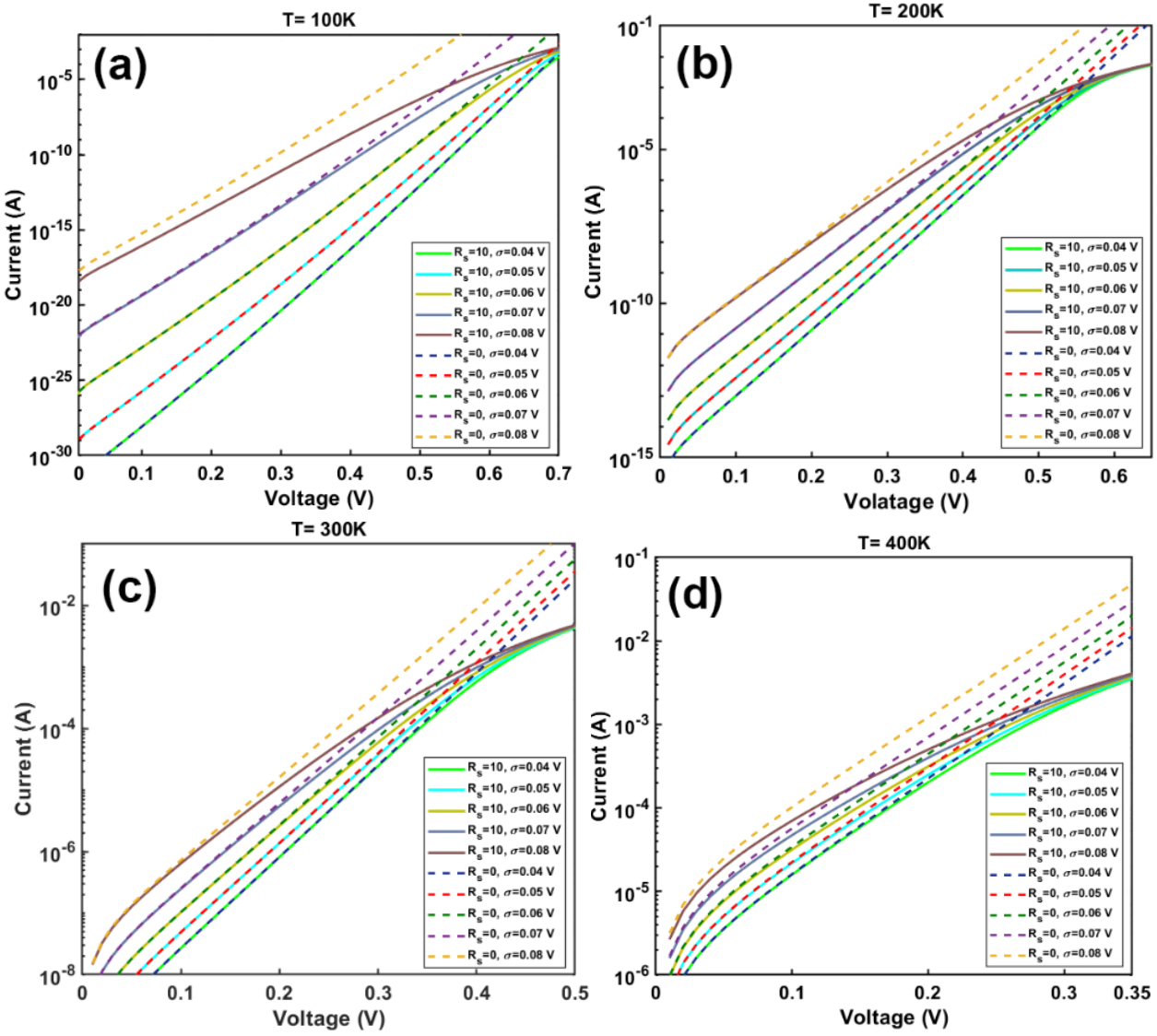

Fig. 6. LnI-V characteristics of the SD by considering R_s and standar deviation for 100, 200, 300, and 400 K, respectively (color online)

Both the BH vs T and E_a vs σ plots were also drawn in Fig. 7 (a) and 7 (b), respectively.

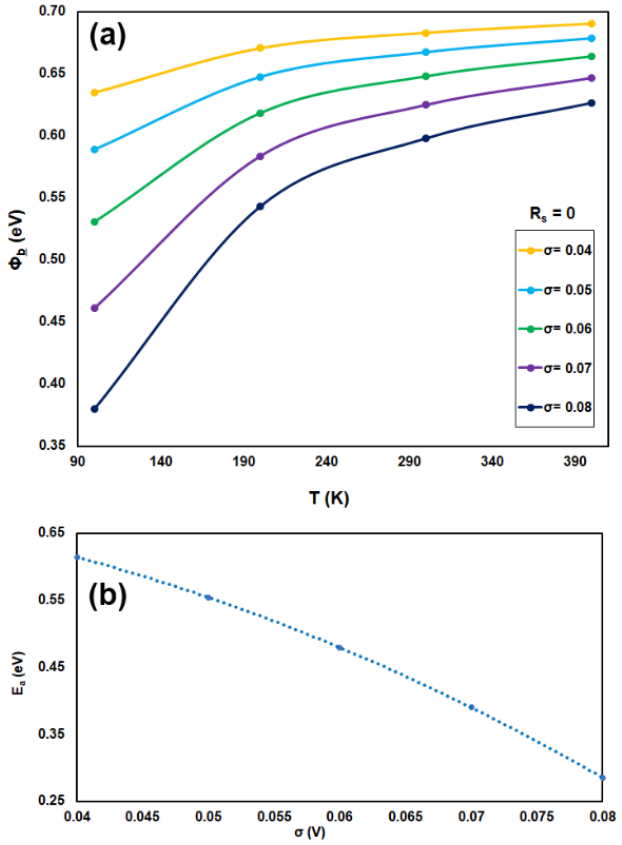

Fig. 7. The BH vs T and E_a vs σ plots for various σ values (0.4, 0.6, 0.7, and 0.8V), respectively (color online)

As can be seen from this figure, while the value of BH for various σ values (0.4, 0.6, 0.7, and 0.8V) increase with increasing temperature, the value of E_a decreases with increasing σ, respectively. It is clear that the changes in value of BH for higher values of σ becomes more evident especially at low temperatures. These results shoew that the value of σ is more effective on the current-conduction mechanisms as well as R_s. Some researchers were also indicated that the barier inhomogeneity is also dependent on used metallic rectifier contact due to its work function and melting point and so the height of the MS contact barrier will be a combination of several local barrier heights [40-43].

3. Conclusion

In this research, the forward bias lnI vs V features in metal/silicon structures have been investigated in detail by using an iteration method in wide range of temperature and voltage for various values R_s. For the zero value of R_s, these plots show an intersection treatment at about 0.8 V and this is unusual behavior in comparison with the expected behavior of ideal SDs. The linear relation between voltage and current for R_s=0 show that the current or conductivity increasing with the rise in temperature until intersection point and then begins to decrease. This reduction in current despite the rising of temperature after intersection point is a contradiction with the presented positive temperature coefficient of current. Interestingly, this intersection behavior becomes disappear for R_s>0 values because this intersection has been kept hidden and unobservable in homogeneous SDs due to the existence of R_s. Contemplating the intersection points of each curve with the other curves, it can be concluded that the slope of lnI-V curves is autonomous of temperature. In order to determine the voltage dependent activation energy, Arrhenius plots for R_s=0 and 150 Ω were also drawn and they show that the slope these plots which is corresponding E_a decrease with increasing applied bias voltage. This indicated that the value or BH or E_a is also dependent on bias voltage as well as temperature. The enlarged view around the intersection region of lnI-V curves indicates that the crossing point of any pair of lnI-V curves for different temperatures occurs at different bias voltages as almost as $qV_i = \Phi_B + 2kT/q$. In addition, the forward bias LnI vs V characteristics have been investigated by considearation both the effects of R_s and σ. While the value of BH for various of σ increase with increasing temperature, the value of E_a decreases with increasing σ, respectively. All these results Show that the investigation of conduction mechanisms in SDs is more complicate and depend on many factors such as temperature, R_s, dislocations, barrier inhomogeneity and its standard deviation especially under room temperatures.

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