On the profile of temperature and voltage dependence of interface states and resistivity in Au/n-Si structure with 79 Å insulator layer thickness

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In this study, the temperature and voltage dependence of interface states (N_{ss}) and resistance profile of Au/n-Si structure with 79 Å insulator layer thickness were obtained from the forward and reverse bias capacitance-voltage (*C-V*) and conductance-voltage (G/ω-*V*) measurements in the temperature range of 80-400 K at 1 MHz. The main electrical parameters, such as doping concentration (N_D), Fermi energy level (E_F), depletion layer width (W_D) and barrier height (Φ_{CV}), of these structures were also determined from the reverse bias C^{-2} vs *V* plots in the same range. The values of Φ_{CV} at the absolute temperature (*T=0 K*) and the temperature coefficient (α) of barrier height were found as 1.152 eV and -2.4×10^{-4} eV/K, respectively. These values are in a close agreement with the bandgap value of Si at 0 K (E_g=1.17 eV) and its temperature coefficient value (-4.73×10^{-4} eV/K). C-V plots for all temperature levels show an anomalous peak in the accumulation region because of the effect of series resistance (*Rs)*. Similarly, G/ω-*V* plots also show a peak in the depletion region between the temperature range of 160-320 K. The effect of R_s on the *C* and *G* is found noticeable especially at high temperatures. Therefore, the measured *C* and *G* values were corrected in order to eliminate the effect of R_s using Nicollian and Brews method. In addition, the temperature dependent ac conductivity (σ_{ac}) data obtained between 200 and 400 K show a linear behavior and was fitted to the Arrhenius plot. The values of activation energy (E_a) obtained from the slope ln□-*q/kT* plots are 21.7, 18.5, 15.0 and 11.5 meV for the values of applied biases 3.5, 4.0, 4.5 and 5.0 V, respectively.

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1. Introduction

In the ideal case, the capacitance of metal-semiconductor (MS) structures with and without an interfacial insulator or organic layer is usually frequency independent, especially at high frequencies (f ≥ 500 kHz) and shows an increase with the increasing forward bias voltage [1-8]. However, the situation is different in practice especially because of interface states (N_{ss}), series resistance (R_s) of structures, interfacial insulator layer and its thickness (d_i) and surface charges [9-18]. Among them, the interface states at semiconductor/insulator interface play an important role in determination of the main characteristic parameters of these structures. Since the bare silicon (without an interfacial insulator layer) surfaces exhibit orders of magnitude higher state density than the silicon-oxide interfaces in these structures, the state density can be expected to decrease with increase in the number of initial oxide mono-layers [8-9]. In addition, the existence of an insulator layer at metal/semiconductor (M/S) interface converts the structures into metal-insulator-semiconductor (MIS) structures/diodes, and it also can have a strong influence on diode characteristics as well as on N_{ss} [1-3,17-20] present at the insulator-semiconductor interface [17-20]. These interface states usually cause a bias shift in the measured capacitance - voltage (C_m-*V*) and conductance - voltage (G_m-*V*) curves [1,2]. This insulator layer does not only prevent inter-diffusion between metal and semiconductor substrates, but also alleviate the electric field reduction issue in MS structures. R_s is also an important parameter which causes the electrical characteristics of these structures to be non-ideal especially at high bias voltages [1-6,19-23]. Therefore, the parameter R_s is only effective in the accumulation region or at sufficiently high bias voltages of the *C-V* and G/ω-*V* characteristics, whereas the other parameters are effective especially in the depletion and weak inversion regions.

When a voltage is applied across the MS structure, the combination of the insulator layer, depletion layer and R_s of the device will share the applied bias voltage. The share-ratio depends on insulator layer thickness and R_s. Although MS structures have been studied extensively, satisfactory understanding in detail has not been achieved yet [10-23]. The best of our knowledge, the temperature and applied bias voltage dependent profiles of N_{ss} and R_s of these structures have not been investigated in the wide temperature and applied bias voltage ranges. Particularly, the anomalous peak and intersection behavior can only be observed at sufficiently high forward bias voltages

[12,14]. In recent years, some investigations [5,7,11,19] have reported an anomalous peak in the forward bias *C-V* characteristics. One of these very interesting studies is presented by Chattopadhyay and Raychaudhuri [19]. They showed that, in the presence of R_s, the *C-V* characteristics should exhibit a peak. The peak value of the *C* and its position depends on a number of various parameters such as density distribution of N_{ss}, doping concentration (N_D *or* N_A), R_s of device, and interfacial insulator layer and its thickness d_i [7,11,19].

The aim of this study is to investigate experimentally the temperature dependence of the forward and reverse bias *C-V* and *G/ω-V* characteristics of MS structures with SiO_2 interfacial insulator layer by considering R_s and N_{ss} effect. Therefore, in order to achieve a better understanding of the effects of N_{ss} and R_s on the *C-V* and *G/ω-V* characteristics, we have measured the forward and reverse bias *C-V* and *G/ω-V* characteristics of this structure in the wide temperature range of 80-400 K at 1 MHz. Experimental results show that both N_{ss} and R_s are important parameters that influence the electrical characteristics of MS structure with an interfacial insulator layer. In addition, the values of activation energy (E_a) were obtained from the slope $\ln\sigma$-q/kT plots for various applied bias voltages.

2. Experimental procedure

The metal-semiconductor Au/n-Si structures with 79 Å insulator layer (SiO_2) thickness were fabricated on n-type (P-doped) single crystals silicon wafer with <100> surface orientation, having thickness of 350 μm, 2" diameter and 1 Ω.cm resistivity. For the fabrication process, the Si wafer was degreased in organic solutions of $CHClCCl_2$, CH_3COCH_3 and CH_3OH, then etched in a sequence of H_2SO_4 and H_2O_2, 20% HF, a solution of $6HNO_3$:1HF:$35H_2O$, 20% HF and finally quenched in de-ionized water with resistivity of 18 MΩ cm for a prolonged time. High purity (99.999 %) gold (Au) layer with a thickness of ~1500 Å was thermally evaporated from the tungsten filament onto the whole backside of Si wafer at a pressure of ~$2x10^{-6}$ Torr in oil vacuum pump system. The ohmic contact was prepared by sintering the evaporated Au back contact at 650 ^oC for 60 minutes in flowing dry nitrogen ambient at rate of 2 lit./min. This process served both to the sinter the Au and to form the required insulator layer (SiO_2) on the upper surface of the Si wafer. Finally, circular dots of 1 mm diameter Au with a thickness of ~1500 Å were deposited in order to form the rectifier contacts on the oxidized surface of the Si wafer through a Cu shadow mask in the same vacuum system. The thickness of metal layers and the deposition rates were monitored with the help of quartz crystal thickness monitor. The interfacial layer thickness was estimated to be about 79 Å from high frequency (1MHz) C-*V* measurement of the oxide capacitance in the strong accumulation region. In order to carry out *C-V* and *G/ω-V* measurements, the electrical contacts are made on to the upper electrode on the oxide with the help of fine phosphor-bronze spring probe.

The temperature dependence of the reverse and forward bias capacitance-voltage (*C-V*) and conductance-voltage (*G/ω-V*) measurements of MS structures with SiO_2 interfacial insulator layer were carried out in the temperature range of 80-400 K at 1 MHz by using a HP 4192A LF impedance analyzer (5 Hz - 13 MHz) and a small sinusoidal signal of 40 mV_{p-p} from the external pulse generator is applied to the sample in order to meet the requirement [1]. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card. Also, the sample temperature was continually monitored by using a copper-constant thermocouple close to the sample and measured with a Keithley model 199 dmm/scanner and a Lake Shore model 321 auto-tuning temperature controller with sensitivity better than ± 0.1 K.

3. Results and discussion

It is well known the MIS or MOS structure consists of two parallel plates with one electrode (a metallic plate) and the other electrode that are called as gate and semiconductor, respectively. These two electrodes or plates are separated by a thin insulating layer such as SiO_2, SnO_2 and TiO2. MIS structure was first proposed as a voltage-dependent capacitor [1]. Soon after, it was used to study properties of the Si-SiO_2 interface by Terman [24] who calculated energy levels and relaxation times (τ) of interface states (N_{ss}) from the analysis of experimental *C-V* measurements over a wide range of frequency values. Also, Goetzberger [25] performed a similar study in detail. Afterwards, Nicollian and Brews [1] wrote a book to give detailed information on the charges in the MOS system measurement methods and theoretical background MOS structures. The analysis of the *C-V* and *G/ω-V* measurements of these devices at only room temperature and one bias voltage cannot give us detailed information about conduction mechanisms and barrier formation at M/S interface. However, *C-V* and *G/ω-V* measurements of these devices in a wide temperature and bias voltage range (both under forward and reverse bias) can allow us to understand different aspects of conduction mechanisms and/or the temperature and bias voltage dependence of main electrical parameters. The measurements were held at 1 MHz because at sufficiently high frequencies ($f \geq 1$ MHz), N_{ss} cannot follow the ac external signal so that the amount of excess capacitance coming from N_{ss} is minimized [1].

In the light of the explanation made above, in this study, the *C-V* and *G/ω-V* measurements of Au/n-Si structure with 79 Å insulator layer thickness were carried out in the temperature range of 80-400 K at 1 MHz and are given in Fig 1(a) and (b) respectively. As shown in Fig. 1(a) and (b), both *C-V* and *G/ω-V* characteristics exhibit accumulation, depletion and inversion regions. The applied voltage range was between -3 V and +7 V. As can be seen in these figures, the *C* and *G/ω* values increase with the increasing temperature in the depletion region.

The *C-V* plots for all temperatures show an anomalous peak in the accumulation region because of the effect of series resistance (*Rs)*. Similarly, *G/ω-V* plots also show a peak in depletion region between 160 and 320 K. Another important feature in the *C-V* plots is the crossing/intersection behavior at about a certain bias voltage. After this crossing point, the values of C happen to decrease with the increasing temperature.

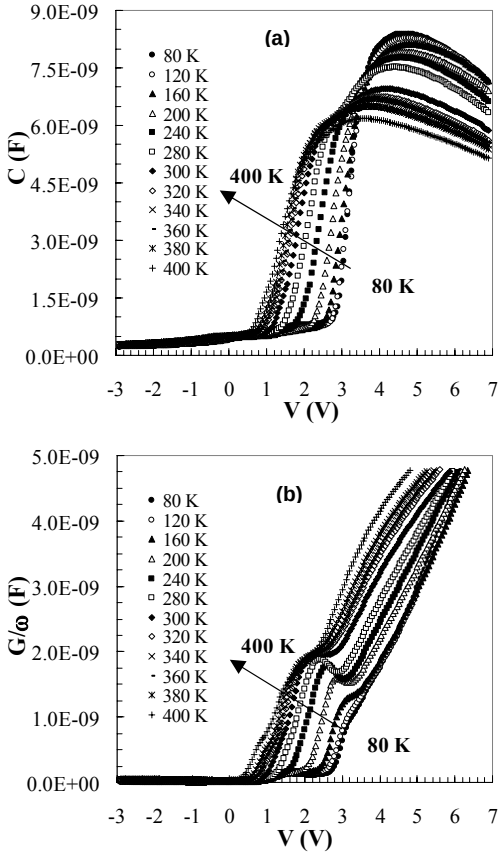

Fig. 1. The temperature dependent plots of (a) C-V and (b) G/ω-V characteristics of the Au/n-Si structure with 79 Å insulator layer thickness at 1 MHz.

In order to explain the effect of bias voltage, the capacitance and conductance values are shown in Figs. 2 (a) and (b), respectively, in the accumulation region (after the crossing point) as a function of temperature with steps of 0.25 V. As shown in these figures, the values of *C* decrease with the increasing temperature while those of *G* increase with the increasing temperature for all bias voltage values. However, the change in *C* and *G/ω* is considerably high at low temperatures. We believe that the trap charges have enough energy to escape from the traps located at M/S interface in the Si band gap under the temperature effect. Also, this can be attributed to the decrease in R_s with the increasing temperature. It is clear that the effect of R_s on *C* and *G* is noticeable especially at high temperatures and in the accumulation region. Therefore, the measured *C* and *G* values were corrected in order to eliminate the effect of R_s.

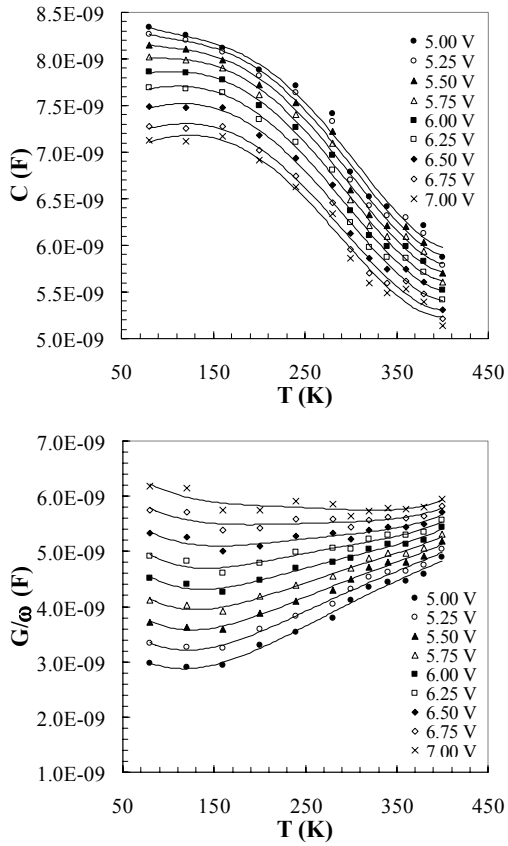

Fig. 3. The temperature dependent plots of (a) C-V and (b) G/ω-V characteristics of the Au/n-Si structure with 79 Å insulator layer thickness at 1 MHz and various bias voltages with the step of 0.25 V.

Many methods have been suggested [1,21-23,26] to extract the value of R_s, but many suffers from a limitation of their applicability to practical devices with an interfacial insulator or oxide layer. Therefore, in our calculations, we have applied the admittance method presented by Nicollian and Goetzberger [1]. According to this method, the real series resistance of a MIS or MOS device can be subtracted from the measured capacitance (C_{ma}) and conductance (G_{ma}) values in the strong accumulation region at a sufficiently high frequency value (f ≥ 1 MHz) [1]. In addition, voltage dependence of the R_s can be obtained from the measurements of frequency dependent *C-V* and *G/ω-V* data using the following equation.

$$R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2} \tag{1}$$

where C_m and G_m represent the measured *C* and *G* for a given bias voltage. Once the R_s values are found, the capacitance of insulator layer C_{ox} can be obtained in strong

accumulation region at 1 MHz by substituting R_s into the relation

$$C_{ma} = \frac{C_{ox}}{(1+\omega^2 R_s^2 C_{ox}^2)} \quad (2a)$$

From this relation, C_{ox} is obtained as

$$C_{ox} = C_{ma}\left[1+(\frac{G_{ma}}{\omega C_{ma}})^2\right] = \frac{\varepsilon_i \varepsilon_0 A}{d_{ox}} \quad (2b)$$

where ε_i=3,8ε_o [1,2] and ε_o (=8,85x10^{-14} F/cm) are the permittivity of the interfacial insulator layer and that of free space, respectively. Finally, by comparing the imaginary and real parts of corrected admittance (Y_c=G_c+$j\omega C_c$) one obtains the corrected capacitance (C_c) and conductance (G_c) as

$$C_c = \frac{\left(G_m^2+(\omega C_m)^2\right)C_m}{a^2+(\omega C_m)^2} \quad (3a)$$

and

$$G_c = \frac{G_m^2+(\omega C_m)^2\, a}{a^2+(\omega C_m)^2} \quad (3b)$$

where

$$a = G_m - \left(G_m^2+\left(\omega C_m\right)^2\right)R_s \quad (3c)$$

The insulator layer (SiO_2) thickness d_i was obtained from high frequency (f = 1 MHz) *C-V* curve using the Eq. 2(b) and was found as 79 Å.

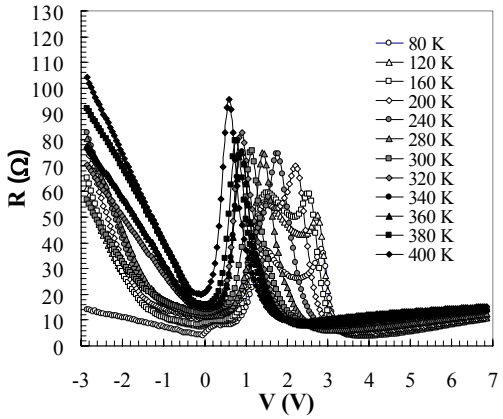

Fig.3. The variation of the series resistance of the Au/n-Si structure with 79 Å insulator layer thickness as a function of bias voltage for various temperatures at 1 MHz.

The voltage dependent R_s values of the structure were calculated using the data of Fig 1 (a) and (b) according to Eq.(1) and shown in Fig. 3 for various temperatures. Also, the values of R_s for the various forward biases are given in Fig. 4. These very significant values demanded that special attention should be given to effects of the R_s in the application of the admittance-based measurement methods (*C–V* and *G/ω–V*).

As seen in Fig. 2, the R_s plots exhibit two peaks in the low temperatures and then the second peak disappears at high temperatures. In addition, the first peak moves to the strong accumulation region with the increasing temperature and the amplitude of these peaks increases with the increasing temperature. The change in R_s becomes rather important in the depletion and accumulation regions, but nearly independent of temperature in the strong accumulation region. The change in *C* and G/ω in the depletion region as well as the change in R_s can be attributed to the particular density distribution of interface states/traps at Si/SiO_2 interface and to the trapped charges' having enough energy to escape from the traps located between metal and semiconductor interface in the Si band gap and. This variation of R_s with temperature can be expected for the semiconductors in the temperature region where there is no freezing behavior of the carriers. As a result, it is clearly seen from Figs. 2 and 3, the value of R_s depend on the changes in both temperature and applied bias voltage from region to region. The other reason of such behavior of R_s may be restructure and reordering of surface atoms under temperature [33-36].

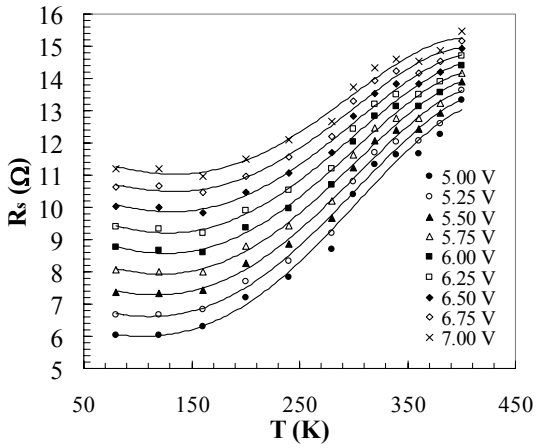

Fig. 4. The temperature dependence of R_s for the Au/n-Si structure with 79 Å insulator layer thickness at various bias voltages and 1 MHz with the step of 0.25 V.

To obtain the real capacitance C_c and conductance G_c/ω of the device, the measured capacitance and conductance at 1 MHz under forward and reverse biases were corrected to rule out the effect of R_s using the equations 3 (a) and (b) for four different temperature values and they are given in Figs. 5 (a) and (b), respectively. When the correction was made on the *C-V* plots, the values of the corrected C_c increased with increasing voltage, especially in the strong accumulation region, as seen in Fig. 5 (a). On the other hand, the plots of the corrected G_c/ω give a peak, proving that the charge transfer can take place through the interface (Fig. 5 (b)). These results indicate that R_s is only effective in the

accumulation region while N_{ss} is only effective in the depletion region.

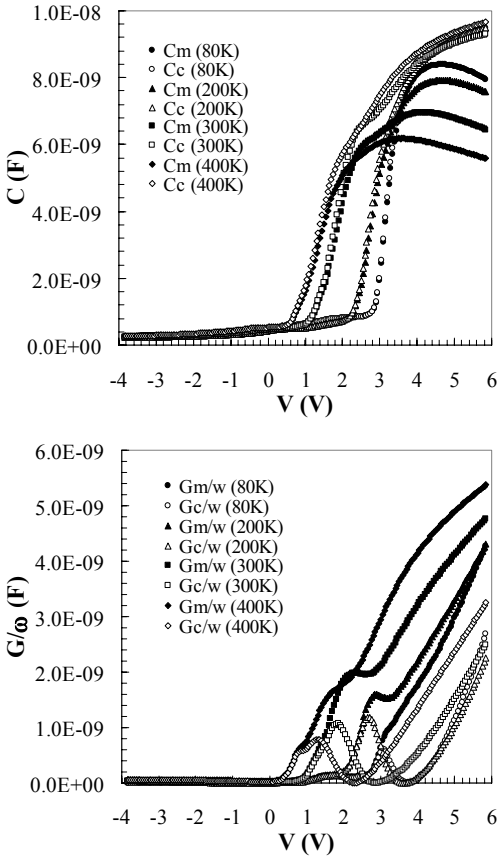

Fig. 5. The voltage dependent plots of the corrected (a) capacitance and (b) conductance at room temperature and 1 MHz.

The temperature dependent C^{-2} vs V characteristics of Au/n-Si structure with 79 Å insulator layer thickness were obtained from the reverse bias C-V and they were presented in Fig. 6. As it can be seen from Fig. 6, the C^{-2} vs V plot gives a straight line in a wide bias voltage range which is an evidence of the admittance measurements were done at sufficiently high frequency. The diffusion potential values are obtained from the extrapolation of these straight lines to the voltage axis for each temperature, and are given in Table 1. The depletion layer capacitance of a diode can be expressed as [1-3].

$$C^{-2} = \frac{2(V_R + V_o)}{q\varepsilon_s N_D A^2} \tag{4}$$

where V_R is the reverse bias voltage, N_D is the doping concentration and V_o is the built-in voltage at zero bias, and can be determined from the extrapolation of the C^{-2} vs V plot for each temperature on bias axis.

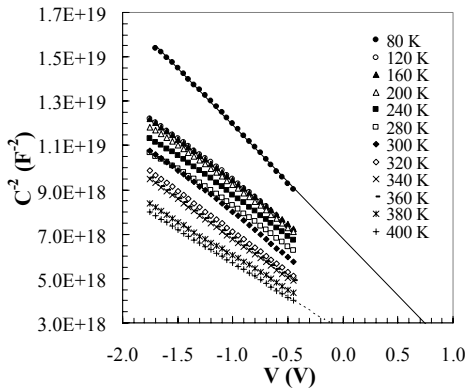

Fig. 6. The reverse bias C^{-2}-V characteristics of Au/n-Si structure with 79 Å insulator layer at 1 MHz for various temperatures.

Thus, the values of Fermi energy level (E_F), depletion layer width (W_D), N_D were determined from C^{-2} vs V plots (Fig. 6) for each temperature using the following equations:

$$V_o = V_D - \frac{kT}{q} \tag{5a}$$

where V_D is the diffusion potential at zero bias and the term of kT/q is thermal energy.

$$E_F = \frac{kT}{q} Ln\left(\frac{N_C}{N_D}\right) \tag{5b}$$

With

$$N_C = 4.82x10^{15} T^{3/2} (m_e^* / m_o)^{3/2} \tag{5c}$$

where N_C is the effective density of states in the semiconductor conductance band and m_o is the rest mass of the electron. Thus, the barrier height Φ_{CV} values were calculated at each temperature using the following relation.

$$\Phi_{CV} = V_o + \frac{kT}{q} + E_F - \Delta\Phi_B \tag{6}$$

where $\Delta\Phi_B$ is the image force barrier lowering and given by [1,2]

$$\Delta\Phi_B = \left(\frac{qE_m}{4\pi\varepsilon_s\varepsilon_o}\right)^{0.5} \tag{7a}$$

where E_m is the maximum electric field and it can be obtained from the following relation:

$$E_m = \left(2qN_D V_d / \varepsilon_s\varepsilon_o\right)^{0.5} \tag{7b}$$

In general, at sufficiently high frequencies ($f \geq 1$ MHz) the interface states (N_{ss}) do not contribute to the capacitance [1-3] since they are in equilibrium with the semiconductor. The relationship of the theoretical carrier doping density $N_D^{'}$=1.73×10^{15} cm^{-3} and the ratio of the experimental and the theoretical carrier doping density N_D is known as $c_2 \cong N_D^{'}/N_D$ [14,17,27,28]. Therefore, the density of interface states N_{ss} were calculated at different temperatures by using

$$c_2 = \frac{1}{1+\beta} \tag{8}$$

where $\beta = q\delta N_{ss}/\varepsilon_i$ [29,30]. The mean density of interface states N_{ss} were calculated at different temperatures from Eq. (8), by taking the d_i value as 79 Å. The obtained experimental values of V_o, N_D, E_F, Φ_{CV}, E_{max}, W_D, c_2, and N_{ss} at different temperatures were presented in Table 1. As shown in Table 1, the obtained V_o, Φ_{CV}, W_D and N_{ss} values decrease, while the values of N_D , E_F and c_2 increase with the increasing temperature. In addition to table 1, the temperature dependence of Φ_{CV} was given in Fig. 7. As can be seen in Fig.7 and Table 1, the values of Φ_{CV} decrease with the increasing temperature and can be described as

$$\Phi_{CV}(T) = \Phi_{CV}(T=0) - \alpha T \tag{9}$$

where Φ_{CV} *(T=0)* is the barrier height extrapolated to zero temperature and α is the temperature coefficient of barrier height. In Fig. 7, the fitting of the Φ_{CV} *(T)* yields Φ_{CV} *(T=0)* as 1.152 eV and α as -2.404x10^{-4} eV/K. Here the negative temperature coefficient of the barrier height is in a close agreement with the temperature coefficient of the Si band gap (-4.73x10^{-4} eV/K) in the temperature range of interest. Such temperature dependence of the barrier height can be explained either in the terms of Fermi level pinning or reduction of diffusion potential. The Fermi level can be pinned either by the metal induced gap states (MIGS) or defect states at the interface [31]. If the Fermi level is pinned by defects, the temperature dependence of barrier height (BH) will be strong because the temperature dependence of the BH is governed by the temperature dependence of the band gap. As a result, the variation of the BH with temperature is similar to forbidden band gap of semiconductor. It is well known the variation of band gap of semiconductor with temperature can be expressed approximately by a universal function [2]

$$E_g(T) = E_g(0K) - \frac{\alpha T^2}{(\beta + T)} \tag{10}$$

where E_g (0 K) is the value of band gap at absolute temperature, α is the negative temperature coefficient (-4.73x10^{-4} eV/K for Si) of band gap (dE$_g$/dT) and β is a constant (636 for Si). The decrease in the BH and E_g of semiconductor with the increasing temperature can be explained by using Eq.(9) and (10), respectively.

Table 1. Temperature dependent values of various parameters determined from C–V characteristics of Au/Si structure with 79 Å insulator layer at 1 MHz.

T (K)	V_0 (V)	N_D (cm^{-3})	E_F (meV)	E_{max} (V.cm^{-1})
80	1.075	5.80x10^{15}	53.7	4.39x10^4
120	1.035	6.70x10^{15}	79.1	4.63x10^4
160	0.995	7.10x10^{15}	104.7	4.68x10^4
200	0.955	7.60x10^{15}	129.7	4.76x10^4
240	0.920	7.80x10^{15}	155.1	4.74x10^4
280	0.880	7.95x10^{15}	180.5	4.69x10^4
300	0.860	8.15x10^{15}	192.7	4.70x10^4
320	0.840	8.25x10^{15}	205.3	4.68x10^4
340	0.825	8.38x10^{15}	217.6	4.68x10^4
360	0.805	8.55x10^{15}	229.7	4.68x10^4
380	0.790	8.90x10^{15}	241.2	4.74x10^4
400	0.770	9.10x10^{15}	253.2	4.74x10^4
T (K)	**Φ_{CV} (eV)**	**W_d (cm)**	**c_2**	**N_{ss} (eV^{-1}.cm^{-2})**
80	1.135	4.93x10^{-5}	0.418	1.15x10^{13}
120	1.124	4.51x10^{-5}	0.482	8.86x10^{12}
160	1.113	4.31x10^{-5}	0.511	7.90x10^{12}
200	1.101	4.09x10^{-5}	0.547	6.84x10^{12}
240	1.095	3.97x10^{-5}	0.562	6.45x10^{12}
280	1.084	3.85x10^{-5}	0.572	6.17x10^{12}
300	1.078	3.77x10^{-5}	0.587	5.82x10^{12}
320	1.072	3.71x10^{-5}	0.594	5.65x10^{12}
340	1.071	3.65x10^{-5}	0.603	5.43x10^{12}
360	1.065	3.57x10^{-5}	0.616	5.16x10^{12}
380	1.063	3.47x10^{-5}	0.641	4.63x10^{12}
400	1.057	3.40x10^{-5}	0.655	4.35x10^{12}

The value of ac electrical conductivity (σ_{ac}) of Au/n-Si structure with 79 Å insulator layer thickness was also calculated using the measured conductance values (Fig. 1(b)) for four different applied bias voltages from the relation

$$\sigma_{ac} = \frac{G_m . d_i}{A} \tag{11}$$

where G_m is the measured conductivity for a given applied bias voltage at 1MHz and d_i is the thickness of interfacial insulator layer(SiO_2).

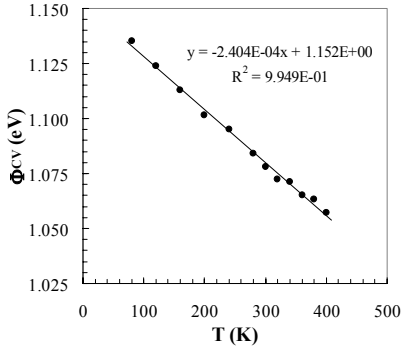

Fig. 7. The temperature dependent of Φ_{CV} vs T characteristics of Au/n-Si structure with 79 Å insulator layer at 1 MHz for various temperatures.

The temperature dependence of the σ_{ac} of the structure is given in Fig. 8. As can be seen in Fig. 8, the values of σ_{ac} for each bias voltage increases with the increasing temperature in the whole temperature range. This behavior of σ_{ac} is parallel to the behavior of G/ω with temperature in accordance with the Eqn. 11. The relationship between the σ_{ac} and inverse absolute temperature is given by the following equation,

$$\sigma_{ac} = \sigma_0 \exp\left(-\frac{E_a}{kT}\right) \quad (12)$$

where σ_o is the pre-exponential factor, k is the Boltzmann constant, T is the absolute temperature in K and E_a is the apparent activation energy. Using the Eqn. 12, one can obtain E_a values from the slope of $ln\sigma_{ac}$-q/kT plot which is also known as Arrhenius plot. The obtained σ_{ac} data for the four different bias voltage values were fitted to the Arrhenius plots which are also given in the Fig. 9 in the temperature range of 160-400 K.

As can been seen in Fig. 9, the $ln\sigma_{ac}$-q/kT plots show almost linear behavior for four different bias voltage values. The E_a values were obtained from the slopes of the $ln\sigma_{ac}$-q/kT plots as 21.7, 18.5, 15.0 and 11.5 meV for the applied bias values of 3.5, 4.0, 4.5 and 5.0 V, respectively. The E_a values decrease with the increasing bias voltage and such low values of E_a is associated recombination which causes even more departures from thermionic-emission behavior at low temperatures [32]. Moreover, such low values of E_a can also be attributed to the existence of the space charges. The conduction electrons may be created in the form the donor state as a possible consequence of ionized oxygen vacancies.

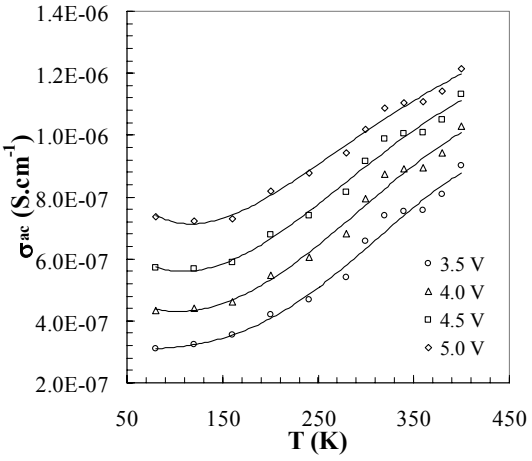

Fig. 8. Temperature dependence of ac electrical conductivity (σ_{ac}) of Au/n-Si structure with 79 Å insulator layer thickness at 1 MHz.

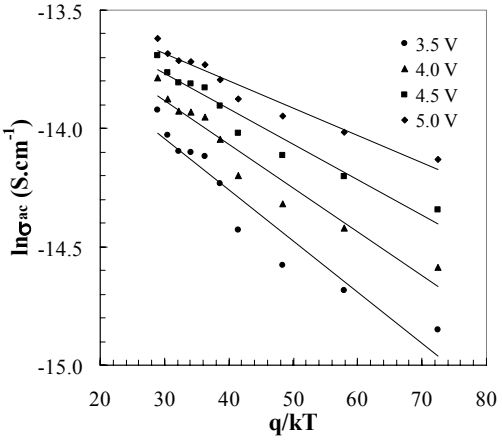

Fig. 9. Arrhenius plot of σ_{ac} of Au/n-Si structure with 79 Å insulator layer thickness at 1 MHz.

4. Conclusions

The measurements of the forward and reverse bias C-V and G/ω-V characteristics of the Au/n-Si structure with 79 Å insulator layer thickness were carried out in the temperature range of 80-400 K at 1 MHz. Experimental results show that C and G/ω values are quite sensitive to temperature, applied bias voltage, R_s and N_{ss}. The values of C increase with the increasing temperature till a peak is observed and after the peak the C values decrease with the increasing temperature and applied bias voltage. Similar to C values, G/ω values also increase with the temperature and applied bias voltage. Another important feature in the C-V plots is the crossing/intersection behavior at about a certain bias voltage. After this crossing point, the values of C happen to decrease with the increasing temperature. The peak behavior in the accumulation region of C-V plots is a result of R_s while that in the depletion region of G/ω-V plots is a result of N_{ss}. However, the peak behavior in the G/ω-V plots, unlike that in the C-V plots, tends to disappear as the temperature is increased since the values of N_{ss} decrease with the increasing temperature. The values of R_s calculated using C-V and G/ω-V measurements give two peaks for low temperature values and the magnitude of the peaks observed in R_s-V plots increase with the increasing temperature. The change in C, G/ω and R_s in the depletion region can also be attributed to the particular density distribution of N_{ss} at Si/SiO_2 interface and to the trapped charges' having enough energy to escape from the traps located between metal and semiconductor interface in the Si band gap. In addition, C and G/ω values were corrected to eliminate the effect of R_s and from the C_c-V and G_c/ω-V plots it was observed that R_s is more effective at high temperatures. The values of V_o, Φ_{CV}, N_D, E_F, c_2 and W_D are also derived from the C^{-2}-V plots. Experimental results show that the obtained V_o, Φ_{CV}, W_D and N_{ss} values decrease, while the values of N_D, E_F and c_2 increase with the increasing temperature. Also, the values of E_a are obtained from the slopes of $ln\sigma_{ac}$-q/kT

plots as 21.7, 18.5, 15.0 and 11.5 meV for the applied bias values of 3.5, 4.0, 4.5 and 5.0 V, respectively.

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