Optical quadruple Peres gate using SLM and Savart plate

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In recent years, energy dissipation is a major issue and this occurs due to information loss. Lossless data processing can be achieved using reversible circuits. Any reversible computation in a system can be performed if the system consists of only reversible logic gates. Reversible logic is very useful to many future computing technologies for faster operation. Optical logic gates are very important for handling large volume of data at high speed in multi valued logic (MVL) with high efficiency. In MVL system, trinary and quadruple valued logic are the most important. In this paper, optical quadruple Peres Gate using spatial light modulator (SLM) and Savart Plate has been proposed and described.

(Received January 24, 2017; accepted February 12, 2018)

Keywords: Di-bit, Peres Gate, Quadruple, Savart Plate, SLM

1. Introduction

In recent years, the advantages of integrated circuit technology made it feasible to implement electronic circuits operating with more than two discrete levels of signal. This gives the concept of multi valued logic (MVL). E.V. Dubrova [1] and others have proposed and developed multi valued logic (MVL) circuit design, revealing both the opportunities they offer and the challenges they face [2-4]. Different arithmetic operations like addition, multiplications in Galois field and also addition, subtraction and multiplication in modulo-4 arithmetic are demonstrated in MVL system by Vasundara Patel and K. S. Gurumurthy [5]. Quaternary to binary and binary to quaternary converters are also designed for this purpose [6].

The advantages of technology during the last two decades have generated a large demand for handling large volume of data at high speed. To meet up the requirements, the concept of multi valued logic (MVL) came forward from the status of the two-valued or binary logic system in the one hand and on the other, these include the idea of optical processor for switches. Parallel operation can be performed using optical processors but it was also felt that it can be possible to represent multivalued logic using the polarization states of light beam along with the presence or absence of light in optical system [7]. Avizienis introduced a signed digit number system for proper utilization of parallelism of optical beam instead of cascaded single- bit operating units [8]. The modified signed digit [9-13] or modified trinary number system [14] suggested the carry free operation. The ternary logic system based on three states was introduced by Lukasiewicz [14] and further it was modified by him to four states logic for better proposition.

Irreversible operation produces information loss which results in energy dissipation. The energy dissipated for every irreversible bit operation is at least KTln2 joules according to Landauer's research, where T is the operating temperature and K=1.3806505*10-23m2kgs-2K-1 (joule/kelvin) is the Boltzmann's constant [15]. The above mentioned energy can be saved if the operation is a reversible operation as described by Bennett in 1973[16]. Reversible operation means inputs can also be derived form output.

Differnt applications for lossless data processing can be performed using reversible operation [17-20]. Design of reversible logic optically is very important for faster operation. With this aim, a optical quadruple Peres Gate using SLM and Savart Plate is presented in this paper. The simulation results verify the he superiority of the proposed scheme.

The proposed paper is organized as follows: Section 2 deals with the description of quadruple valued logic systems. Section 3 describes briefly the truth tables based on di-bit representation. Section 4 presents The operation of the basic building block using SLM and Savart Plate is presented in Section 4. The operating principle and design of Quadruple Peres Gate is represented in Section 5. The logical simulation results and final conclusion with scope of future works are made in Section 6 and Section 7 respectively.

2. Quadruple Valued Logic System

The four states of the quadruple valued logic system are represented as the true, partly true, partly false and the false [21-23]. As the quadruple valued system with states {0, 1, 2, 3} does not satisfy the basic field conditions so, dibit representation of the form 00 ➔0, 01➔ 1, 10➔ 2 and 11 ➔3 is considered which is similar to basic two

valued logic system. As four is not a prime number, this should be included in Galois Field GF(k^r) for cosideration as a field, where r is a positive integer and k is a prime number . For quaternary logic, Galois field may be represented as GF(2^2) i.e k=2 and r=2. The elements and the states {0,1,2,3} of GF(2^2) are represented by dibit as {00, 01, 10, 11} respectively [24]. Table 1 represents the logical states, their representations and corresponding dibit representations and the state of polarization.

Table 1. Quadruple-Valued Logic System

Logical state	Represented by	Dibit representation	State of polarization
False/ Wrong information	0	00	No light
Partial Information	1	01	Vertical polarization
Partial Information (complement of 1)	2	10	Horizontal polarization
True/ Complete Information	3	11	Presence of both the horizontal & vertical polarization

3.Truth tables based on di-bit representation

The different quadruple logic gates e.g., OR, AND, NOT, XOR, NAND, NOR and XNOR are represented bit-wise in this section as shown in Table 2.

Table 2. Truth tables for (a) OR, (b) AND, (c) NOT (d) XOR, (e) NAND, (f) NOR and (g) XNOR Gates.

(a)

B \ A	00	01	10	11
00	00	01	10	11
01	01	01	11	11
10	10	11	10	11
11	11	11	11	11

(b)

B \ A	00	01	10	11
00	00	00	00	00
01	00	01	00	01
10	00	00	10	10
11	00	01	10	11

(c)

A	$\bar{A}$
00	11
01	10
10	01
11	00

(d)

B \ A	00	01	10	11
00	00	01	10	11
01	01	00	11	10
10	10	11	00	01
11	11	10	01	00

(e)

B \ A	00	01	10	11
00	11	11	11	11
01	11	10	11	10
10	11	11	01	01
11	11	10	01	00

(f)

B \ A	00	01	10	11
00	11	10	01	00
01	10	10	00	00
10	01	00	01	00
11	00	00	00	00

(g)

B \ A	00	01	10	11
00	11	10	01	00
01	10	11	00	01
10	01	00	11	10
11	00	01	10	11

4.The basic building block

Different logical operations in quadruple valued logic system are implemented using basic building block. The basic building block is shown in Fig. 1. Light output from laser source L after getting polarized at an angle 45° with respect to the two crystal axes is incident on the Savart Plate S_1 as shown in Figure 1. The savart plate S_1 is used to split the light into two orthogonal components. The light comes out of S_1 with a spatial shift between them. The output of S_1 are controlled by electrically addressable negative SLMs - P_1 and P_2. The SLMs are controlled by electrical signal applied on it. The negative SLM becomes opaque when an electric voltage is applied on it and it becomes tranpaprent when no electric voltage is applied on it. The operation of positive SLM is just opposite of negative SLM. The outputs from SLM are finally combined by the Savart Plate S_2.The flow chart of basic building block is also provided in Fig. 2 to understand the operation easily.

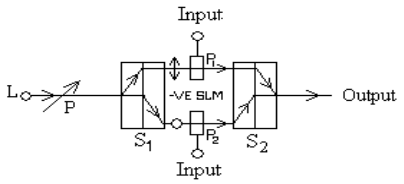

Fig. 1. The Basic Building Block

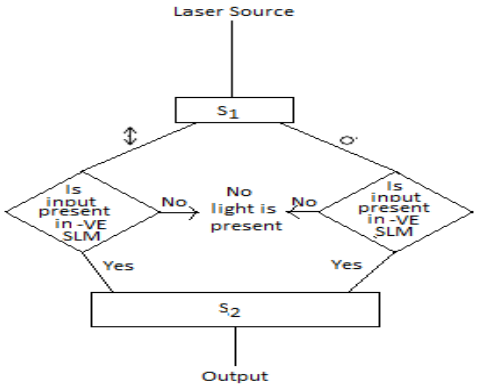

Fig. 2. The flow chart of Basic Building Block

5. Quadruple Peres Gate: Principle and Design

Peres Gate is a (3:3) conservative reversible logic gate. It has three inputs (A, B, C) and three outputs (X, Y, Z) that satisfy the Boolean relations as follows:

$$\left.\begin{aligned} X &= A \\ Y &= A \oplus B \\ Z &= A.B \oplus C \end{aligned}\right\} \quad (1)$$

The binary truth table of Peres Gate is given in Table 3.

Table 3. Binary Truth table of Peres Gate

Inputs			Outputs		
A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

The truth table of quadruple Peres Gate with dibit representation is given in Table 4. In addition, the SLM and Savart Plate based circuit for optical Peres Gate is given in Fig. 3.

Table 4. Truth table of Quadruple Peres Gate

A	A_1	A_2	**B**	B_1	B_2	**C**	C_1	C_2	**X**	X_1	X_2	**Y**	Y_1	Y2	**Z**	Z_1	Z_2
0	0	0	**0**	0	0	**0**	0	0	**0**	0	0	**0**	0	0	**0**	0	0
0	0	0	**0**	0	0	**1**	0	1	**0**	0	0	**0**	0	0	**1**	0	1
0	0	0	**0**	0	0	**2**	1	0	**0**	0	0	**0**	0	0	**2**	1	0
0	0	0	**0**	0	0	**3**	1	1	**0**	0	0	**0**	0	0	**3**	1	1
0	0	0	**1**	0	1	**0**	0	0	**0**	0	0	**1**	0	1	**0**	0	0
0	0	0	**1**	0	1	**1**	0	1	**0**	0	0	**1**	0	1	**1**	0	1
0	0	0	**1**	0	1	**2**	1	0	**0**	0	0	**1**	0	1	**2**	1	0
0	0	0	**1**	0	1	**3**	1	1	**0**	0	0	**1**	0	1	**3**	1	1
0	0	0	**2**	1	0	**0**	0	0	**0**	0	0	**2**	1	0	**0**	0	0
0	0	0	**2**	1	0	**1**	0	1	**0**	0	0	**2**	1	0	**1**	0	1
0	0	0	**2**	1	0	**2**	1	0	**0**	0	0	**2**	1	0	**2**	1	0
0	0	0	**2**	1	0	**3**	1	1	**0**	0	0	**2**	1	0	**3**	1	1
0	0	0	**3**	1	1	**0**	0	0	**0**	0	0	**3**	1	1	**0**	0	0
0	0	0	**3**	1	1	**1**	0	1	**0**	0	0	**3**	1	1	**1**	0	1
0	0	0	**3**	1	1	**2**	1	0	**0**	0	0	**3**	1	1	**2**	1	0
0	0	0	**3**	1	1	**3**	1	1	**0**	0	0	**3**	1	1	**3**	1	1
1	0	1	**0**	0	0	**0**	0	0	**1**	0	1	**1**	0	1	**0**	0	0
1	0	1	**0**	0	0	**1**	0	1	**1**	0	1	**1**	0	1	**1**	0	1
1	0	1	**0**	0	0	**2**	1	0	**1**	0	1	**1**	0	1	**2**	1	0
1	0	1	**0**	0	0	**3**	1	1	**1**	0	1	**1**	0	1	**3**	1	1
1	0	1	**1**	0	1	**0**	0	0	**1**	0	1	**0**	0	0	**1**	0	1
1	0	1	**1**	0	1	**1**	0	1	**1**	0	1	**0**	0	0	**0**	0	0
1	0	1	**1**	0	1	**2**	1	0	**1**	0	1	**0**	0	0	**3**	1	1
1	0	1	**1**	0	1	**3**	1	1	**1**	0	1	**0**	0	0	**2**	1	0
1	0	1	**2**	1	0	**0**	0	0	**1**	0	1	**3**	1	1	**0**	0	0
1	0	1	**2**	1	0	**1**	0	1	**1**	0	1	**3**	1	1	**1**	0	1
1	0	1	**2**	1	0	**2**	1	0	**1**	0	1	**3**	1	1	**2**	1	0
1	0	1	**2**	1	0	**3**	1	1	**1**	0	1	**3**	1	1	**3**	1	1
1	0	1	**3**	1	1	**0**	0	0	**1**	0	1	**2**	1	0	**1**	0	1
1	0	1	**3**	1	1	**1**	0	1	**1**	0	1	**2**	1	0	**0**	0	0
1	0	1	**3**	1	1	**2**	1	0	**1**	0	1	**2**	1	0	**3**	1	1
1	0	1	**3**	1	1	**3**	1	1	**1**	0	1	**2**	1	0	**2**	1	0
2	1	0	**0**	0	0	**0**	0	0	**2**	1	0	**2**	1	0	**0**	0	0
2	1	0	**0**	0	0	**1**	0	1	**2**	1	0	**2**	1	0	**1**	0	1
2	1	0	**0**	0	0	**2**	1	0	**2**	1	0	**2**	1	0	**2**	1	0
2	1	0	**0**	0	0	**3**	1	1	**2**	1	0	**2**	1	0	**3**	1	1
2	1	0	**1**	0	1	**0**	0	0	**2**	1	0	**3**	1	1	**0**	0	0
2	1	0	**1**	0	1	**1**	0	1	**2**	1	0	**3**	1	1	**1**	0	1
2	1	0	**1**	0	1	**2**	1	0	**2**	1	0	**3**	1	1	**2**	1	0
2	1	0	**1**	0	1	**3**	1	1	**2**	1	0	**3**	1	1	**3**	1	1
2	1	0	**2**	1	0	**0**	0	0	**2**	1	0	**0**	0	0	**2**	1	0
2	1	0	**2**	1	0	**1**	0	1	**2**	1	0	**0**	0	0	**3**	1	1
2	1	0	**2**	1	0	**2**	1	0	**2**	1	0	**0**	0	0	**0**	0	0
2	1	0	**2**	1	0	**3**	1	1	**2**	1	0	**0**	0	0	**1**	0	1
2	1	0	**3**	1	1	**0**	0	0	**2**	1	0	**1**	0	1	**2**	1	0
2	1	0	**3**	1	1	**1**	0	1	**2**	1	0	**1**	0	1	**2**	1	0
2	1	0	**3**	1	1	**2**	1	0	**2**	1	0	**1**	0	1	**0**	0	0
2	1	0	**3**	1	1	**3**	1	1	**2**	1	0	**1**	0	1	**1**	0	1
3	1	1	**0**	0	0	**0**	0	0	**3**	1	1	**3**	1	1	**0**	0	0
3	1	1	**0**	0	0	**1**	0	1	**3**	1	1	**3**	1	1	**1**	0	1
3	1	1	**0**	0	0	**2**	1	0	**3**	1	1	**3**	1	1	**2**	1	0
3	1	1	**0**	0	0	**3**	1	1	**3**	1	1	**3**	1	1	**3**	1	1
3	1	1	**1**	0	1	**0**	0	0	**3**	1	1	**2**	1	0	**1**	0	1
3	1	1	**1**	0	1	**1**	0	1	**3**	1	1	**2**	1	0	**1**	0	1
3	1	1	**1**	0	1	**2**	1	0	**3**	1	1	**2**	1	0	**3**	1	1
3	1	1	**1**	0	1	**3**	1	1	**3**	1	1	**2**	1	0	**2**	1	0
3	1	1	**2**	1	0	**0**	0	0	**3**	1	1	**1**	0	1	**3**	1	1
3	1	1	**2**	1	0	**1**	0	1	**3**	1	1	**1**	0	1	**2**	1	0
3	1	1	**2**	1	0	**2**	1	0	**3**	1	1	**1**	0	1	**0**	0	0
3	1	1	**2**	1	0	**3**	1	1	**3**	1	1	**1**	0	1	**1**	0	1
3	1	1	**3**	1	1	**0**	0	0	**3**	1	1	**0**	0	0	**3**	1	1
3	1	1	**3**	1	1	**1**	0	1	**3**	1	1	**0**	0	0	**2**	1	0
3	1	1	**3**	1	1	**2**	1	0	**3**	1	1	**0**	0	0	**1**	0	1
3	1	1	**3**	1	1	**3**	1	1	**3**	1	1	**0**	0	0	**0**	0	0

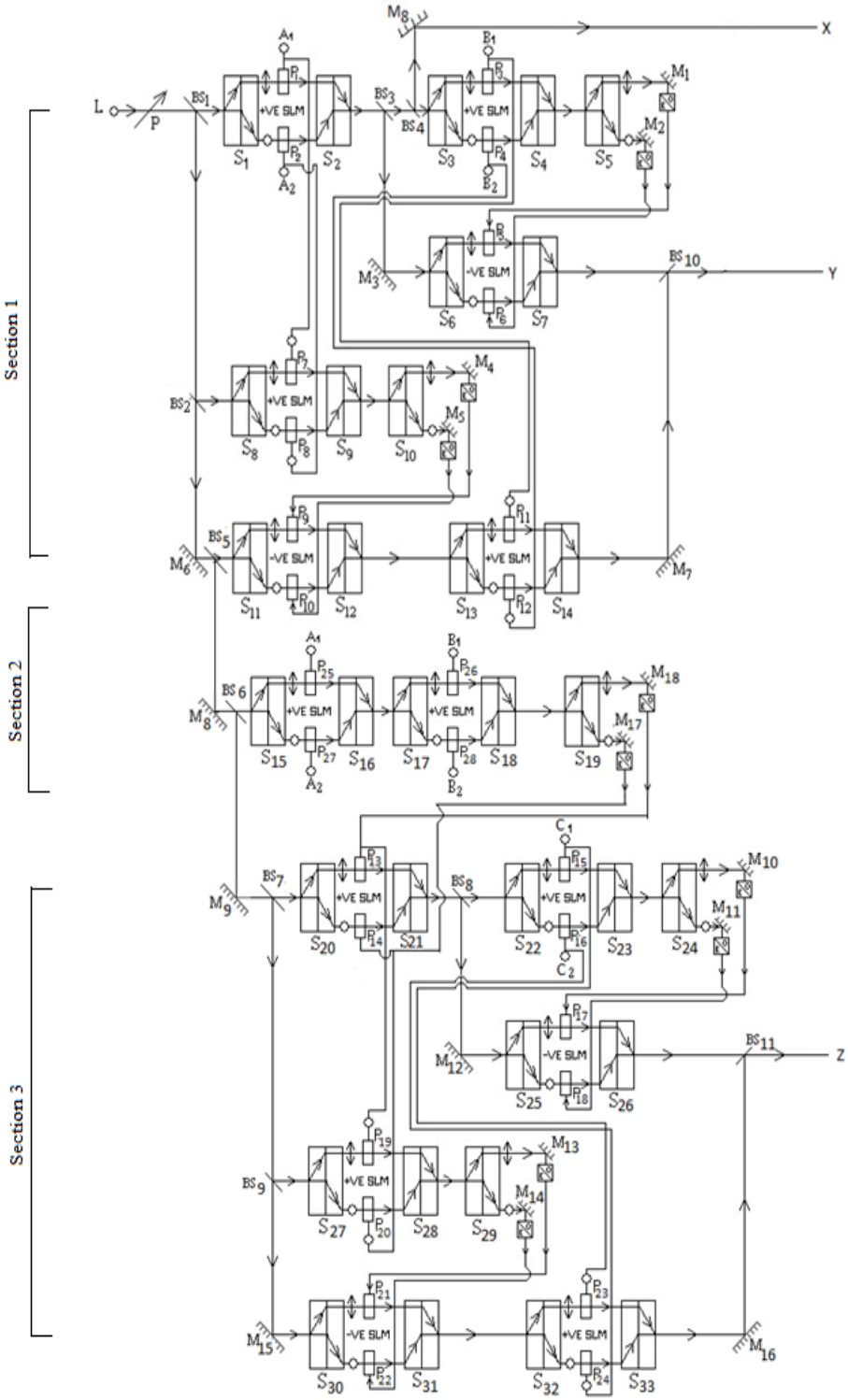

Fig. 3. SLM and Savart Plate based Peres Gate

The above figure consists of three sections. The 1st section performs the XOR operation, 2nd one for AND operation and the last one for again XOR operation. The light output from the Laser source L after getting polarized is incident on the beam splitter BS_1. The beam splitter splits the light into two directions as shown Fig. 3. One part is incident on the Savart Plate S_1 and the other part on the beam splitter BS_2. The output of savart plate S_1 consists of two orthogonal components of light. The components are horizontal polarization of light and the vertical polarization of light. The input A (A_1,A_2) controls the positive SLMs P_1 and P_2. The outputs of P_1 and P_2 are recombined by the Savart Plate S_2. The combined output from S_2 is incident on the beam splitter BS_3. The one part of the output of BS_2 is incident on S_8. The output from S_8 are controlled by positive SLMs P_7 and P_8 and finally they

recombined by S_9. The other part of the output of BS_2 after being reflected by the mirror M_6 is incident on BS_5. It splits the light into two components. One of which is incident on Savart Plate S_{11} and the output of S_{11} are controlled by positive SLMs P_9 and P_{10} depending on the input which is the output of S_{10}. The opto-electrical converters (O/E) are used in the path of the rays for conversion of light signal into electrical signal. The one output of BS_3 is fed to BS_4 which splits the light again in two directions.One is refelected by mirror M_8 and produce the output X=A. Another one is incident on Savart Plate S3 and it is also spacilly modulated by the positive SLMs P_3 and P_4 depending on the control input B_1,B_2 and finally they recombined by S_4. By the same procedure finaly the output of S_{14} and S_7 combined by $BS_{10}$and produce the other output Y=A XOR B.The other part of the output of BS_5 ray reflected by the mirror M_8 is incident on beam spliter BS_6.The one output of BS_6 is also spatially modulated by the positive SLMs P_{25}, P_{27},P_{26} and P_{28}depending on the inputs A (A_1,A_2)and B (B_1,B_2). The output of S_{18} provides A AND B, which acts as the control input for SLM P_{13} and P_{14}. The 3rd section is the same as first section of the circuit diagram. As the inputs for 3rd section are AB (A_1B_1, A_2B_2) and C (C_1,C_2) so the final output can be written as Z = AB XOR C. From truth table 4 it can be seen that total 64 cases are considered. Some cases are discussed as follows:

(1)When A=0 (A_1=0,A_2=0) ,B=0 (B_1=0,B_2=0) and C=0 (C_1=0,C_2=0) then no light at the output of S_2, hence X=0 (X_1=0,X_2=0). No light is present at the output of S_7 and S_{14}, so the output, Y =0(Y_1=0,Y_2=0). As the input C =0 so no light is present at the output of S_{26} and S_{33}, leading to Z =0 (Z_1=0,Z_2=0)

(2)When A=0 (A_1=0,A_2=0) ,B=1 (B_1=0,B_2=1) and C=0 (C_1=0,C_2=0) then no light at the output of S2, hence X=0 (X_1=0,X_2=0). There will be no light at the output of S7. As the P9 and P10 are the negative SLMs, so both polarized light will be present at the output of S_{12}.As P_{11}=0 and P_{12}=1, the output of S_{14}will give vertical polarization. There is no light at the output of S_7.The output is Y=1 (Y_1=0,Y_2=1). As AB =0 (A_1B_1=0,A_2B_2=0) and C=0 so there will be no light at the output of S_{26} and S_{33}i.e. Z =0 (Z_1=0,Z_2=0).

(3) When A=0 (A_1=0,A_2=0),B=2 (B_1=1,B_2=0) and C=0 (C_1=0,C_2=0) then no light at the output of S_2, hence X=0 (X_1=0,X_2=0).As the bit representation of B is reverse with respect to the previous case so P_{11}=1 and P_{12}=0. The output of S_{14}consists of horizontal polarization. There is no light at the output of S_7. The output is Y=2 (Y_1=1,Y_2=0).As AB =0 (A_1B_1=0,A_2B_2=0) and C=0 so there will be no light at the output of S_{26} and S_{33} i.e. Z =0 (Z_1=0, Z_2=0)

(4) As A=0 (A_1=0,A_2=0), B=3 (B_1=1,B_2=1)and C=0 (C_1=0,C_2=0) so light at the output of S_2, hence X=0 (X_1=0,X_2=0). The output of S_{14}consists of vertical and horizontal plarized light. There is no light at the output of S_7. The final output is Y=3 (Y_1=1,Y_2=1).As AB =0 (A_1B_1=0,A_2B_2=0) and C=0 so there will be no light at the output of S_{26} and S_{33} i.e. Z =0 (Z_1=0, Z_2=0)

(5) When A=1 (A_1=0,A_2=1) , B=0 (B_1=0,B_2=0) and C=1 (C_1=0,C_2=1), the output of S_2 is at logic 1 state , hence X=1 (X_1=0,X_2=1).The out put of S_7consists of only vertically polarized light and no light at the output of S_{14}. The output is Y=1 (Y_1=1,Y_2=0). There is no light at the output of S_{26} and the output of S_{33} consists of vertically polarized light i.e. Z =1(Z_1=0, Z_2=1).

(6) When A=1 (A_1=0,A_2=1), B=1 (B_1=0,B_2=1)and C=1 (C_1=0,C_2=1) so the output of S_2 is at logic 1 state, hence X=1 (X_1=0,X_2=1).There is no light at the output of S_7 and S_{14}. The output is Y=0 (Y_1=0,Y_2=0).As AB =1 (A_1B_1=0,A_2B_2=1) and C=1 so there will be no light at the output of S_{26} and S_{33} i.e. Z =0 (Z_1=0, Z_2=0).

(7) When A=1 (A_1=0,A_2=1), B=2 (B_1=1,B_2=0) and C=1 (C_1=0,C_2=1)so the output of S_2 is at logic 1 state, hence X=1 (X_1=0,X_2=1). The out put of S_7 consists of vertically polarized light and the output of S_{14} consists of horizontally polarized light. The output consists of both polarazied light i.e. Y=3 (Y_1=1,Y_2=1).As AB =1 (A_1B_1=0,A_2B_2=1) and C=1 so there is no light at the output of S_{26} and the output of S_{33} consists of vertically polarized light i.e. Z =1(Z_1=0, Z_2=1).

(8) When A=1 (A_1=0,A_2=1), B=3 (B_1=1,B_2=1)and C=1 (C_1=0,C_2=1) so the output of S_2 is at logic 1 state, hence X=1 (X_1=0,X_2=1). There is no light at the output of S_7 and the output of S_{14} consists of horizontally polarized light. The output consists of only horizontally polarized light i.e. Y=2 (Y_1=1,Y_2=0). As AB =1 (A_1B_1=0,A_2B_2=1) and C=1 so there will be no light at the output of S_{26} and S_{33} i.e. Z =0 (Z_1=0, Z_2=0).

(9) When A=2 (A_1=1,A_2=0), B=0 (B_1=0,B_2=0) and C=2 (C_1=1,C_2=0) so the output of S_2 is at logic 2 state, hence X=2 (X_1=1,X_2=0). There is no light at the output of S_{14} and the output of S_7 consists of horizontally polarized light. The output consists of only horizontally polarized light i.e. Y=2 (Y_1=1,Y_2=0). As AB =0 (A_1B_1=0,A_2B_2=0) and C=2 so the output of S_{33} consists of horizonta polarization. There is no light at the output of S_{26}. The output is Z=2 (Z_1=1, Z_2=0).

(10) When A=2 (A_1=1,A_2=0) , B=1 (B_1=0,B_2=1)and C=2 (C_1=1,C_2=0) so the output of S_2 is at logic 2 state, hence X=2 (X_1=1,X_2=0). The out put of S_7 consists of horizontally polarized light and the output of S_{14} consists of vertically polarized light. The output consists of both polarazied light i.e. Y=3 (Y_1=1,Y_2=1).As AB =0 (A_1B_1=0,A_2B_2=0) and C=2 so the output of S_{33} consists of horizonta polarization. There is no light at the output of S_{26}. The output is Z=2 (Z_1=1, Z_2=0).

(11) When A=2 (A_1=1,A_2=0) , B=2 (B_1=1,B_2=0)and C=2 (C_1=1,C_2=0) so the output of S_2 is at logic 2 state, hence X=2 (X_1=1,X_2=0). There is no light at the output of S_7 and S_{14}. The outputis Y=0 (Y_1=0,Y_2=0). As AB=2

(A_1B_1=1,A_2B_2=1) and C=2 so There is no light at the output of S_{26} and S_{33}.The output is Z=0 (Z_1=0, Z_2=0).

(12) When A=2 (A_1=1,A_2=0) , B=3 (B_1=0,B_2=1) and C=2 (C_1=1,C_2=0) so the output of S_2 is at logic 2 state, hence X=2 (X_1=1,X_2=0). There is no light at the output of S_7 and the output of S_{14} consists of vertically polarized light. The output consists of only vertically polarized light i.e. Y=1 (Y_1=0,Y_2=1). As AB=2 (A_1B_1=1,A_2B_2=0) and C=2 so There is no light at the output of S_{26} and S_{33}.The output is Z=0 (Z_1=0, Z_2=0)..

(13) When A=3 (A_1=1,A_2=1), B=0 (B_1=0,B_2=0)and C=3 (C_1=1,C_2=1) so the output of S_2 is at logic 3 state, hence X=3 (X_1=1,X_2=1). There is no light at the output of S_{14} and the output of S_{14} consists of both horizontally as well as vertically polarized light. The output consists of both polarazied light i.e. Y=3 (Y_1=1,Y_2=1). As AB =0 (A_1B_1=0,A_2B_2=0) and C=3 the output of S_{33} consists of vertical and horizontal plarized light. There is no light at the output of S_{26}. The final output is Z=3 (Z_1=1, Z_2=1).

(14) When A=3 (A_1=1,A_2=1), B=1 (B_1=0,B_2=1) and C=3 (C_1=1,C_2=1) so the output of S_2 is at logic 3 state, hence X=3 (X_1=1,X_2=1). There is no light at the output of S_{14} and the output of S_7 consists of horizontally polarized light. The output consists of only horizontally polarized light i.e. Y=2 (Y_1=1,Y_2=0). As AB =1 (A_1B_1=0,A_2B_2=1) and C=3 so there is no light at the output of S_{26} and the output of S_{33} consists of horizontally polarized light. The output consists of only horizontally polarized light i.e. Z=2 (Z_1=1, Z_2=0)

(15) When A=3 (A_1=1,A_2=1),B=2 (B_1=1,B_2=0) and C=3 (C_1=1,C_2=1) so the output of S_2 is at logic 3 state, hence X=3 (X_1=1,X_2=1). There is no light at the output of S_{14} and the output of S_7 consists of vertically polarized light. The output consists of only vertically polarized light i.e. Y=1 (Y_1=0,Y_2=1). As AB =2 (A_1B_1=1,A_2B_2=0) and C=3 so there is no light at the output of S_{26} and the output of S_{33} consists of vertically polarized light. The output consists of only vertically polarized light i.e. Z=1 (Z_1=0, Z_2=1).

(16) When A=3 (A_1=1,A_2=1),B=3 (B_1=1,B_2=1) and C=3 (C_1=1,C_2=1) so the output of S_2 is at logic 3 state, hence X=3 (X_1=1,X_2=1). There is no light at the output of S_{14} and S_7. The output is given as Y=0 (Y_1=0,Y_2=0). As AB =3 (A_1B_1=1,A_2B_2=1) and C=3 so there is no light at the output of S_{26} and S_{33}. No light is present at the output of Z i.e. Z=0 (Z_1=0, Z_2=0).

Similarly the other cases can be described .

6. Performance evaluation through simulation

Simulation is done in Mathcad-7. Here we use 50:50 beam splitters. The vertical axis in Fig. 4 indicates power in dBm, while horizontal axis represents time scale in ps.

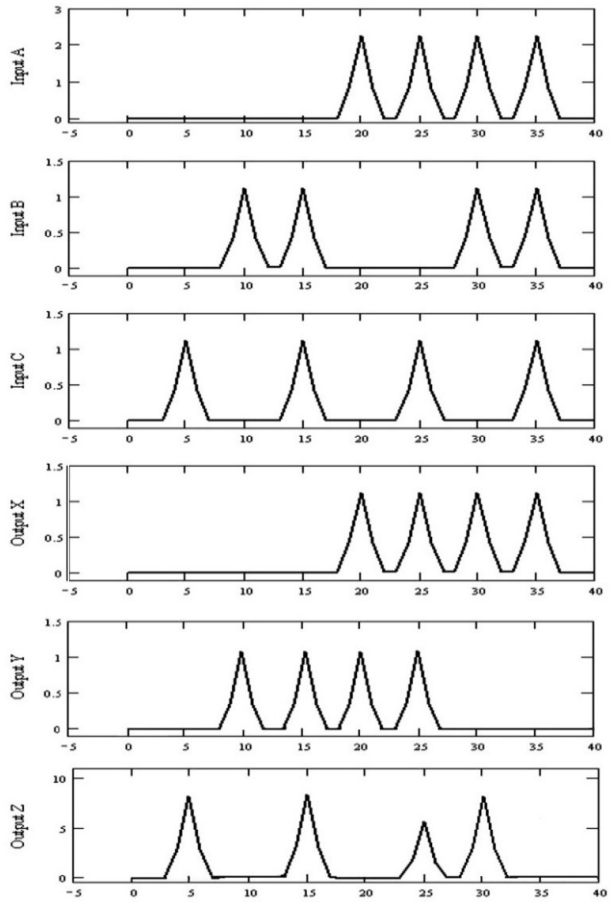

Fig. 4. Logical simulation result [x- axis: time (ps) and y-axis: power (dBm)].

The timing instant for the occurrence of bit pattern are at 0,5,10,15,20,25,30,35 ps. Upper three set waveforms indicate the input bit sequences, 00001111, 00110011, 01010101 for the input variables A, B, C, respectively. Similarly, the lower three waveforms indicate bit sequences 00001111, 00111100, 01010110, bit pattern change of output variables X, Y, Z, respectively.

A circuit is called reversible if input can also be determined from the output combinations. Let us test the reversible operation from the simulation results with chosen arbitrary time at 10 ps. The output signals at time instant 10 ps are X=0, Y=1 and Z=0. Putting these values in Equation (1) we can write as follows:

X = A, indicates A=0

Y=A $\oplus$ B, indicates B=1 and

Z= A.B $\oplus$ C, indicates C=0.

The generated inputs A=0, B=1 and C=0 are satisfying the Table 3. Similarly, the different output bit patterns at different time instant give the different input bit combinations, which satisfy the reversibility condition.

7. Conclusions and scope of future works

This paper deals with the design of optical quadruple Peres Gate circuit based on SLM and Savart Plate. The developed theoretical models are very much useful for

optical reversible logic computing system. This gate can be used to perform different logical and arithmetic operations in reversible domain. The purpose of this study is to explore the quadruple logic system in four-state implementation which is possible to handle more information at a time. In future the peres gate can be used for realization of various boolean expressions in the form of system implementations and arithmetic operations.

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