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Origin of anomalous peak and negative capacitance in the forward bias C-V characteristics of Au/n-InP Schottky Barier Diodes (SBDs)

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The temperature dependence of forward and reverse bias capacitance-voltage (C-V) and conductance-voltage (G/w-V) characteristics of Au/n-InP SBDs have been investigated in the temperature range of 80-400 K at 1 MHz. Experimental results show that the values of capacitance (*C*) and conductance (*G/w)* were found a strongly function of temperature and bias voltage. The forward bias *C-V* plots exhibit anomalous peaks due to the existence of a series resistance (R_s) and the magnitude of these peaks decrease with increasing temperature. In addition, a negative capacitance has been observed in the forward bias *C-V* plots. Physical principle of the negative capacitance has been ascribed to the interface states, the contact injection and minority carrier injection effects. It is thought that the capacitance value decreases with increasing polarization and more carriers are introduced in the structure. Also, the measured capacitance (C_m) and conductance (G_m/w) values have been corrected to obtain the real diode capacitance (C_c) and conductance (G_c/w).

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1. Introduction

Metal-Semiconductor (MS) and metal-insulator-semiconductor (MIS) Schottky barrier diodes (SBDs) are of the most simple of semiconductor devices [1–9]. InP and its alloys are attractive semiconductor in recent years due to their applications in MS, MIS, metal-insulator-semiconductor field effect transistor (MISFET) devices, light emitting diodes (LEDs) and solar cells [10-17]. Although Si has been used fabrication of these devices, compound semiconductor devices using such as InP and GaAs, have recently been developed because of their optimum band gap for photovoltaic energy conversion and a large mobility required for high speed devices [1,2].

Although Schottky interfaces have been well studied for over five decades, its temperature dependent conduction mechanisms have not been sufficiently clarified yet. In the ideal case, the capacitance of these devices is generally frequency independent, especially at high frequency ($f \geq 1$ MHz) and exhibits an decrease with decreasing forward bias voltage [5-9,18-20]. But, this situation is different at low and intermediate frequency and temperature especially in the depletion and accumulation region [6,19-26]. The performance and stability of these devices are dependent on some characteristic SBD parameters such as the formation barrier height at M/S interface, R_s of diodes, doping concentration, interface states and the substrate temperature [7,22,27,28].

Some research have been reported a negative capacitance [29-34] and an anomalous peak [4,5,24,35,36] in the forward bias capacitance-voltage (*C-V*) characteristics in the SBDs in the literature. An anomalous peak in the forward bias *C-V* characteristics can be attributed to interface states (N_{ss}) and series resistance (R_s) [6-8,23]. Physical mechanism of the negative capacitance in different devices has been ascribed to the interface states, the contact injection and minority carrier injection effects [23,29,38]. Observed negative capacitance can be interpreted by considering the loss of interface charge at occupied states below Fermi level due to impact ionization [36]. This negative capacitance occurs when the interface states depart from equilibrium with the metal Fermi level due to an increasing a rate of hopping to the bulk states.

Only at room temperature, the *C-V* and *G/w-V* measurements can not give us detail information about the conduction mechanisms and barrier formation at M/S interface. However, these measurements at wide temperature range allow us to understand different aspects of current-conductions mechanism. Because the change in the substrate temperature has important effects on the determination of main SBD parameters such as barrier height (Φ_B), series resistance (R_s) and doping concentration (N_d).

Therefore, in this paper, we have been carried out the forward bias *C-V* and *G/w-V* characteristics in the wide temperature range of 80-400 K to investigate the effects of anomalous peak and negative capacitance. Many systems consist of a semiconductor between two contacts but with N_{ss} or bulk traps where charges can be accumulated and released when the forward applied bias and the external an a.c. voltage are applied and a large effect can be produced on devices [29-34,37]. However, physical mechanisms of the anomalous and negative *C* are not well understood yet.

For this aim, the origins of anomalous peak and negative capacitance in the forward bias capacitance-voltage (*C-V*) plots of Au/n-InP SBDs have been investigated in the wide range of temperature. Also, in order to evaluate the effect of R_s on the *C-V* and *G/w-V* characteristics in the studied temperature range with bias voltage ranged from -7 to 3V at 1 MHz, the measured capacitance (C_m) and conductance (G_m/w) values have been corrected to obtain the real diode capacitance (C_c) and conductance (G_c/w).

2. Experimental procedure

In this study, Si doped n-type InP having thickness of 7000 A^0 was grown on n-InP(100) substrate using the VG80H solid source molecular beam epitaxy (MBE) system. Before contact process, the n-InP wafer was dipped in 5 H_2SO_4+H_20_2+ H_20 (1:1:300) solution for 1.0 min to remove surface damage layer and undesirable impurities and then in H_20+HCl solution and then followed by a rinse in de-ionized water with a resistivity of 18 MΩcm. The wafer has been dried with high purity nitrogen (N_2) and inserted into the vacuum chamber immediately after the etching process then high purity gold (Au) metal (99.999%) with a thickness of 1020 A^0 was thermally evaporated from the tungsten filament onto the whole back surface of the wafer in the pressure of ~ 10^{-6} Torr. The ohmic contact was formed by sintering the evaporated Au contact at 400 °C for 90 min in flowing dry nitrogen ambient at a rate of ~2 l/min. After finishing this process, temperature was reduced to 300 ^{0}C and sample was annealed during 10 minutes. Then the sample was cooled to room temperature. To make Schottky contact on epilayer section, circular dot shaped Au Schottky contacts with a thickness of 1000 Å were formed by evaporating Au in the pressure of ~10^{-6} Torr. So Au/n-InP SBDs have been fabricated. Then the sample was removed from system and was soldered with silver pleat and then Schottky contacts were connected with conductor fiber by assistance of silver pleat. After fabricated process of the Au/*n*-InP SBDs, temperature dependence *C-V* and *G/w-V* characteristics were measured in the temperature range of 80-400 K. The *C–V* and *G/w-V* measurements have been performed at 1 MHz by using HP 4192A LF impedance. Experimental measurements have been carried out in the temperature range of 80-400 K using a temperature controlled Janes vpf-475 cryostat. The sample temperature has been monitored by using a copper-constantan thermocouple close to the sample and measuring with a dmm/scanner Keithley model 199 and a Lake Shore model 321 auto-tuning temperature controllers.

3. Results and discussion

Fig. 1 (a) and (b) show that the experimental forward and reverse bias capacitance-voltage-temperature (*C-V-T*) and conductance-voltage-temperature (*G/w-V-T*) characteristics of Au/n-InP SBD in the temperature range of 80-400 K at 1 MHz, respectively. The investigation of *C-V* and *G/w-V* measurements at wide temperature and bias regions is more important to clarify the conduction mechanism. The applied voltage range was between -7 and 3 V.

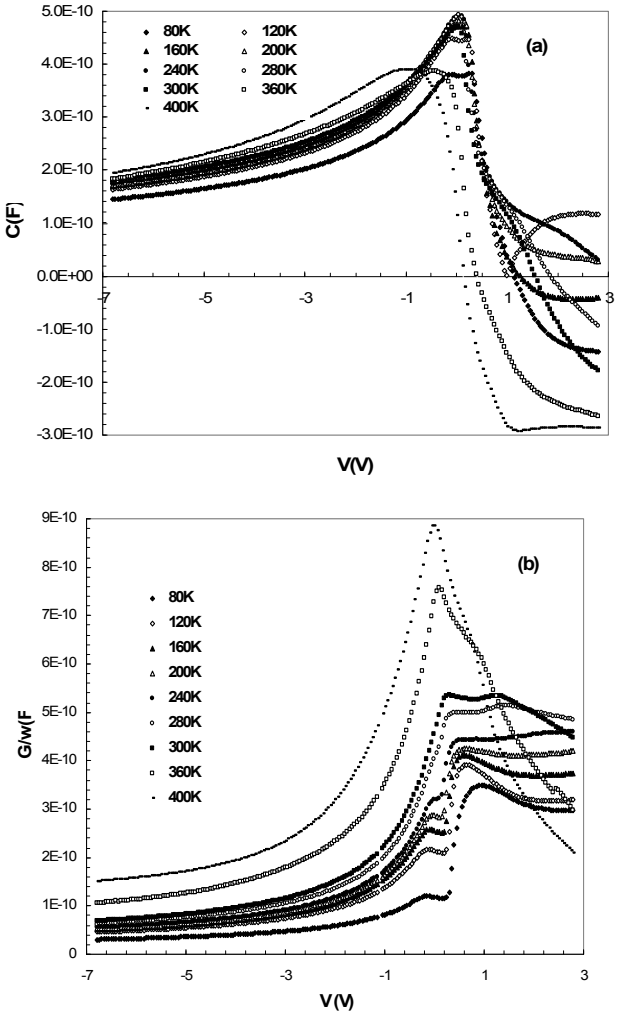

Fig. 1. (a) The capacitance-voltage (C-V) and (b) conductance-voltage (G/w-V) characteristics of Au/n-InP SBD at 1 MHz at wide temperature range.

It is shown that there is the significantly temperature dispersion both in the *C-V* and *G/w* plots, indicating the existence of the interface states and an insulator layer between metal and semiconductor that is in thermal equilibrium with the semiconductor and can not communicate with the metal.

As shown in Fig. 1(a) and (b), both the values of *C* and *G/w* systematically with increasing temperature and give a peak in each temperature and shifting to negative bias region with increasing temperature. These existence peaks in the *C-V* and *G/w-V* plots of Au/n-InP SBD have been reported by the other researchers [7,26,27] and explained by the molecular restriction and reordering of the N_{ss} and R_s. As shown in Fig.1(b), the values of conductance increase with increasing temperature

agreement with the literature. In addition, an existent of negative capacitance in *C-V* plots suggests an increment of bias voltage produces a decrease in the charge on the electrodes [30]. The term of negative capacitance means that the material displays an inductive behavior. Such temperature dependent behaviors of forward bias anomalous *C-V* peak and negative capacitance are an obvious disagreement with the reported in literature for these devices.

Fig. 2 (a) and (b) show the voltage dependent of the capacitance *C* and conductance *G/W* measurement in studied temperature range. As shown in Fig. 2 (a), *C* values usually decrease with increasing temperatures for each bias voltage. It is clearly seen in Fig. 2 (a), that the capacitance is independent of bias voltage at high temperature. On the other hand, *G/w* values (Fig.2 (b)) usually increase with increasing temperatures then become decrease around at room temperature. We considered that the trap charges have enough energy to escape from the traps located between metal and semiconductor interface in the InP band gap.

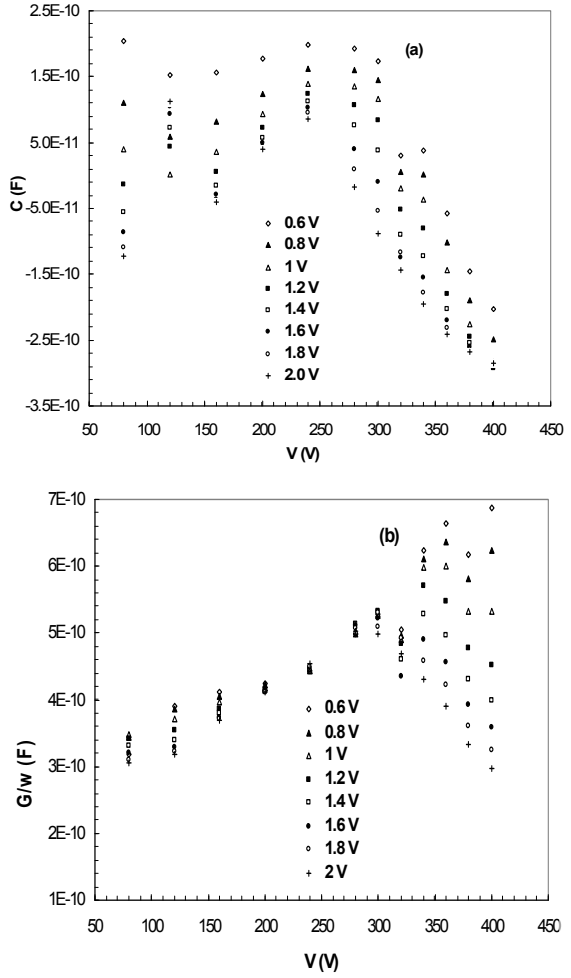

Fig. 2.The temperature dependent of the experimental (a) C-V and (b) G/W-V characteristics of the Au/n-InP SBD for various voltage value ranged from 0.6 V to 2V.

At sufficiently high frequencies (f≥500 kHz), the interface states can not follow the a.c. signal, because at high frequencies the carrier life time (τ) is larger than the measured period [19]. Therefore, the real R_s of the SBDs can be determined from the measured C_m and G_m/w at a high frequency (1MHz). In addition, both the temperature dependence and bias voltage dependence of the values of R_s were obtained from the data of *C-V-T* and *G/w-V-T* plots by using the Nicollian and Goetzberger method [19] and are shown in Fig 3. (a) and (b), respectively.

$$R_s = \frac{G_m}{G_m^2 + \left(\omega C_m\right)^2} \tag{1}$$

where C_m and G_m represent the measured capacitance and conductance in strong accumulation region.

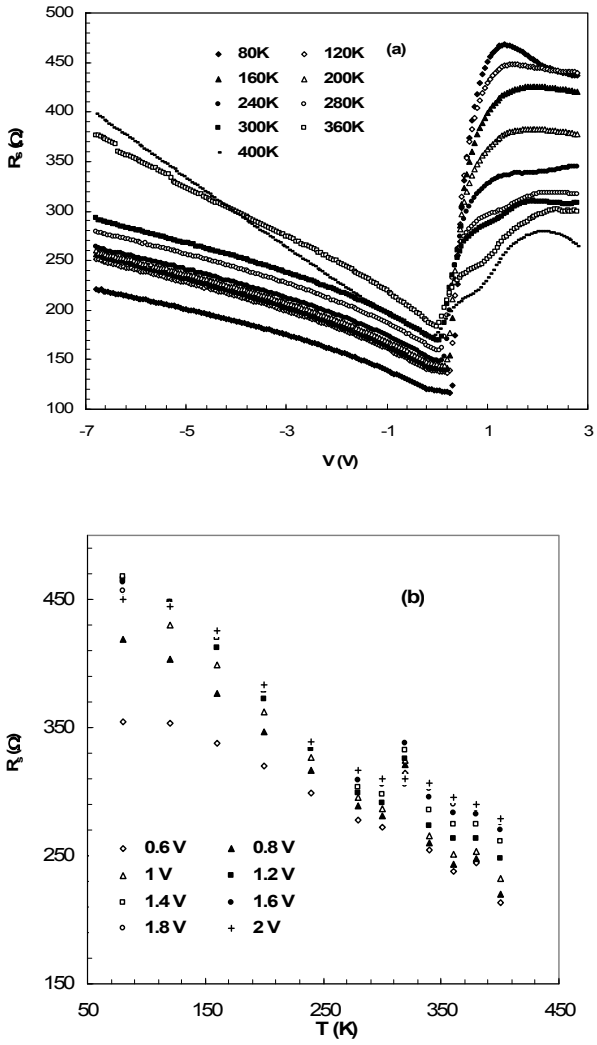

Fig. 3.(a) and (b). The variation of the series resistance of Au/n-InP SBD as a function of voltage in the wide temperature range at 1 MHz and the temperature dependent of R_s for the Au/n-InP SBD at the various voltage, respectively.

Fig. 3 (a) and (b) show that the temperature and bias voltage dependent of the series resistance in the studied

temperature range. These very significant values demanded that special attention be given to effects of the R_s in the application of the admittance-based measured methods (*C-V* and *G/w-V*). As shown in Fig. 3 (a), R_s values give a peak in the voltage range of 1.35 - 2.1 V depending on temperature and this peak position shifts towards high bias voltage increasing with temperature. Also, the temperature dependence of the R_s at various forward bias voltages was calculated and is given in Fig.3 (b). It shows that the values of series resistance are voltage dependent and decrease almost linearly with increasing temperature. This behavior of R_s is agreement with literature. Also, such behavior of R_s can be attributed to the trap charges which have enough energy to escape from the traps located at Au/n-InP interface in the InP band gap. In our previous study, we have also reported DLTS spectrum on the same sample to investigate deep traps effects [31].

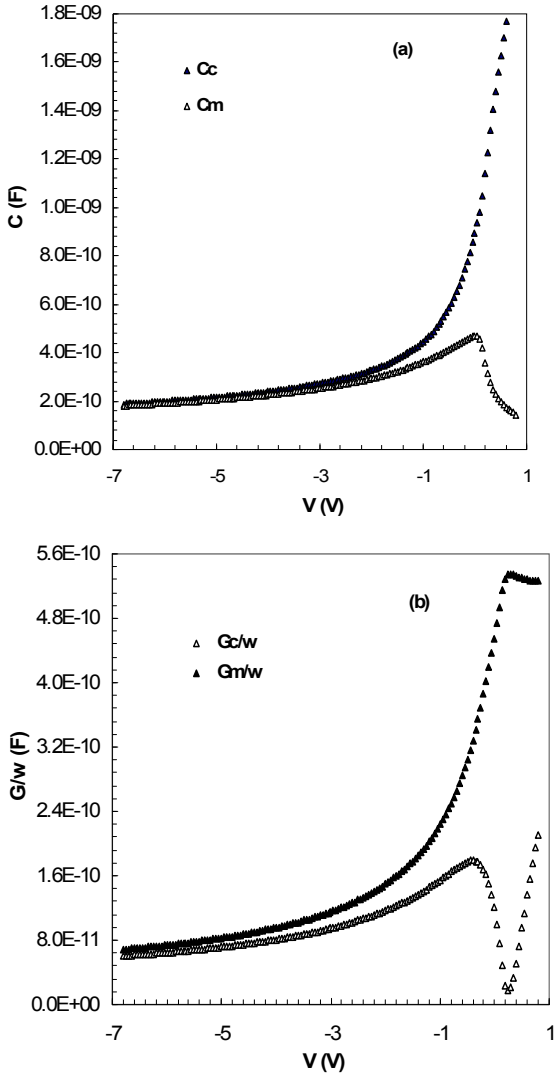

Fig. 4. The voltage dependent plot of the corrected (a) capacitance and (b) conductance curves for 1MHz at wide temperature range.

To obtain the real diode capacitance and conductance, the high frequency (1 MHz) measured under forward and reverse biases at room temperature were corrected for the effects of R_s using Eqs. (2) and (3), respectively, and are given in Fig.4 (a) and (b), respectively, and 1MHz according to

$$C_c = \frac{\left[G_m^2 + (\omega C_m)^2\right] C_m}{a^2 + (\omega C_m)^2} \tag{2}$$

and

$$G_c = \frac{G_m^2 + (\omega C_m)^2 a}{a^2 + (\omega C_m)^2}\ , \tag{3}$$

relations, where a is given in the following form.

$$a = C_m - \left[G_m^2 + (\omega C_m)^2\right] R_s \tag{4}$$

Before corrected, the value of measured capacitance (C_m) gives an anomalous peak in the forward bias region due to the existence of R_s. However, after correction the values of the C_c (Fig.4 (a)), increase with increasing bias voltage, especially in the depletion and accumulation regions. On the other hand, the plot of the corrected conductance (Fig.4 (b)) gives a peak, proving that the charge transfer can take place through the interface.

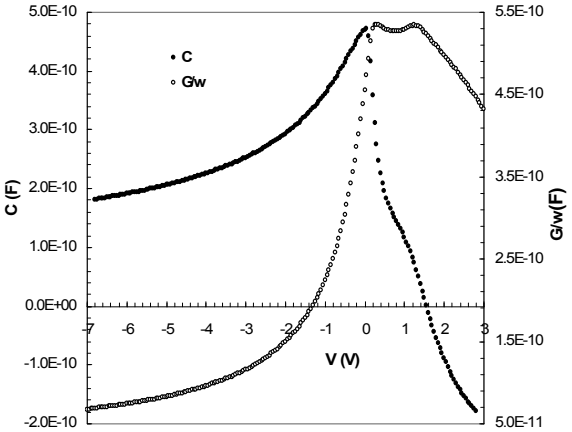

Fig.5. The variation of the C-V and G/w-V for the Au/n-InP SBD as function of bias voltage at room temperature.

Fig. 5 shows variation of measured *C-V* and *G/w-V* of the Au/n-InP SBD at room temperature. As shown in Fig. 5 (a), usually the value of *C* increases with increasing bias voltage in the inversion and depletion regions and gives a peak at accumulation region around about zero-bias voltage. It is clear that the values of *C* shift to negative bias region with increasing bias voltage (V≥1.5 V). At the same time, the values of *G/w* increase with increasing bias voltage in the same regions, but in the accumulation region gives two peaks around about 0.35 and 1.35 V, respectively. In concluded that that the capacitance value

decreases with increasing polarization and more carriers are introduced in the structure.

4. Conclusion

Both the temperature dependence of forward and reverse bias *C-V* and *G/w-V* characteristics of the Au/n-InP SBD were measured in the temperature range of 80-400 K. Experimental results show that both the values of *C* and *G/w* were sensitive to temperature, especially at high temperatures, in which the value of R_s decreases with increasing temperature. Such behavior of *C*, *G/w* and R_s were attributed to the thermal restructuring and reordering of the interfaces states at Au/n-InP interface. In addition, the value of *C* at forward bias gives a peak and then gives negative value. These negative values of *C* correspond to the maximum of the device conductance. It is thought that the capacitance value decreases with increasing polarization and more carriers are introduced in the structure. In addition, the measured capacitance (C_m) and conductance (G_m/w) values were corrected for the effect of series resistance to obtain the real structure capacitance (C_c) and conductance (G_c/w) under both reverse and forward bias.

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