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Practical considerations and electronic properties for CdTe/Si heterojunction solar cell

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The In-doped CdTe/Si (p) Heterostructure was fabricated and its electrical and photoelectrical properties were studied and interpreted. During the fabrication processes of CdTe/Si heterojunction, some practical troubles were encountered. However, the important one was the formation of the SiO_2 thin oxide layer on the soft surface of the Si during the formation of the back contact. The silicon wafer was subjected to different chemical treatments in order to remove the thin oxide layer from the silicon wafer surfaces. It was found that the heterojunction with Si (p+) substrate gave relatively high open circuit voltage comparing with that of Si (p) substrate. Also an electroforming phenomenon had been observed in this structure for the first time which may be considered as a memory effect. It was observed that there are two states of conduction, non-conducting state and conducting state. The normal case is the non-conducting state. As the forward applied voltage increased beyond threshold value, it switches into the conducting state and remains in this state even after the voltage drops to zero

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1. Introduction

In recent years much attention had been paid to the heterojunction devices research [1]. The success of heterojunctions is fully established in electronic devices including solar cells high quality lasers, and optical detectors [2]. Heterojunctions which consist of CdTe as one of the junction sides had been under investigation for many years. Shehathah [3] studied the electrical and photoelectrical characteristics of In-doped CdTe/Si heterojunction. Mohamed et al [4] also studied the electrical properties of post-deposition annealed and as-deposited In-doped CdTe thin films, it was observed that the CdTe film was of modified Poole-Frenkel conduction mechanism and the resistivity of the film could be lowered by more than one order of magnitude due to indium doping. Also, considerable amount of work had been paid to develop the CdS/CdTe solar cells over the last ten years [5]. Levi [6] also studied the electrical, photoelectrical, and structural properties of CdS/CdTe heterostruture. High efficiency solar cells of efficiencies up to 12.5% were developed with a CdTe low temperature (< 450^{o}C) process [7]. Efficient solar cell performance requires minimizing the forward recombination current and maximizing the light generated current. Collection losses can be minimized in thin film of high absorption and short diffusion length. Voltage dependent photocurrent collection losses in CdTe films were observed [8]. The voltage dependence of photocurrent of CdTe/CdS solar cells was characterized by separating the forward current from the photocurrent.

2. CdTe/Si heterojunction properties

Mohamed et al [9] have studied the photovoltaic properties of In-doped CdTe (p) homojunction structure. A new factor denoted as "*S*" was devised to measure how the series resistance affects the short circuit current versus light intensity characteristics of the new structure and generalized conclusions were put forward to cover all types of the conventional solar cells. The In-doped CdTe (p) thin film is of high bulk resistivity which largely affects its photovoltaic properties particularly the short circuit current. It was noted that, the deteriorative effect of the high bulk resistivity increases by increasing the light intensity, which in turn limits the benefit of using light concentrators that improve the short circuit current. Birnkmanm and Alamri [10] found that the use of post deposition heat treatment would probably reduce the bulk resistance and possibly improves contact performance. It was proved previously [4] that the polarity of the applied voltage had almost no effect on the I-V characteristics of Al-In doped-CdTe- Al structure annealed at 100 ^{o}C, which means that the contacts are ohmic. Variation of bulk resistivity with the diffusion temperature is shown in Fig.1. It can be observed that the bulk conductivity of the doped (diffused) films is about one order higher than that of the undoped CdTe films. This is due to the incorporation of Indium atoms that acts as donor sites, which in turn increases the carrier concentration. This will decrease the barrier height at the grain boundaries, resulting in less impedance to the carrier transport [11]. Also it was found that the maximum bulk conductivity is occurred at 100 ^{o}C diffusion temperature.

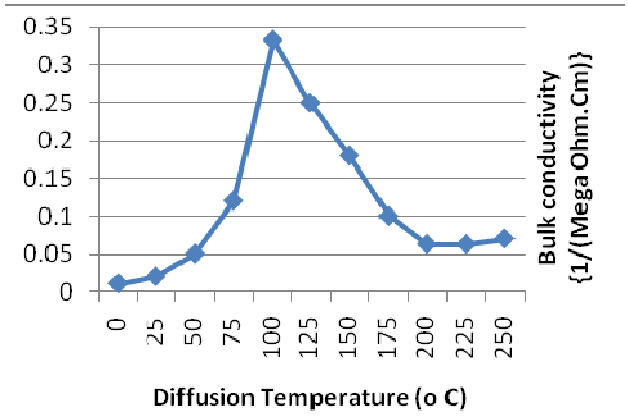

Fig.1: Bulk conductivity vs. diffusion temperatures of In-doped- CdTe thin films.

There is intensive interest to develop high efficiency multi-junction solar cells including the exploration of using silicon (Si) substrate. Heterojunction devices have been realized by depositing phosphorus-doped silicon (Si) (n-type) on a p-type crystalline silicon substrate. The open circuit voltage increases proportionally to the band gap, whereas the number of absorbed photons, i.e., the current decreases with broadening the band gap. The resulting power, as the product of voltage and current, has a maximum value at 1.3 eV. Silicon with the band gap of 1.1 eV and CdTe with 1.5 eV are close to this optimal value. Consistent growth of laterally uniform CdTe (CT) on Si substrate by molecular beam epitaxy has been reported, which indicates that II–VI semiconductor alloys based on CdTe and grown on Si substrates may give good cell performance [12]. Recent nanostructures materials (nanocrystal incorporated in isolators) are used for windows. Electrons can migrate in these structures from one nanocrystal (nc) to adjacent nc and to electrode by tunnel effect, therefore such materials are conductive. Usually nc of the same material as in solar is used for window. Thus, CdTe nc can be used for CdTe solar cell window. Then n-type Si nc on p-type bases is a possible perspective [13].

3. Laboratory preparation

The samples that will be discussed in this paper are of common evaporation conditions. Few samples of CdTe thin films were prepared by thermal evaporation and deposited on Si substrate. The deposition parameters and the sequence of fabricating In-doped CdTe/ Si (p) structure are as follow (see Fig. 2):

a- Deposition of Al back contact 2000 ^{o}A on the back surface of the silicon wafer.

b- Deposition of CdTe layer of 4000 ^{o}A thickness (since the photosensitivity of the evaporated CdTe shows a relatively high value at this thickness [14]) with 8 ^{o}A/s rate of deposition and at 25 ^{o}C substrate temperature. The next step is annealing process at 200 ^{o}C (under vacuum) for an hour in order to anneal the CdTe layer and to support back contact formation.

c- Deposition of indium layer with 100 ^{o}A thickness, on top of the CdTe layer followed by Indium diffusion in CdTe by heating process at 100 ^{o}C under vacuum for an hour.

d- And (e) deposition of aluminum or indium top contact.

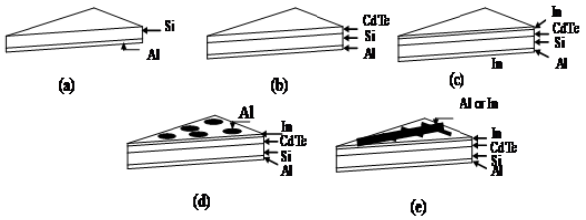

Fig. 2: The sequence of preparing In (Al) – In-doped CdTe/Si – Al structure.

In this paper different structures will be studied. So, for the sake of simplicity, some symbols will be used so that one can easily recognize the different structures. These symbols will be used as superscript incorporated on the letters that describe different structure layers. For instance, the structure In^{*} - $In^{\tilde{}*}$ CdTe/Si (p) indicates and from right to left that: a silicon wafer (p-type) on which a CdTe layer is deposited, $In^{\tilde{}*}$ denotes an indium layer diffused in the CdTe layer in dot- shaped form, so the superscript ($\tilde{}$) represents a diffused layer followed by the superscript (*) denotes the shape of the diffused layer in dot- shaped form. In^{*} denotes indium top contact in dot-shaped form. In this paper the following superscripts will be used:

(*): denotes a dot shape.

($\tilde{}$): denotes a diffused layer.

($^{\#}$): denotes a grid shape, usually used for top contacts.

During the fabrication processes of CdTe/Si heterojunction, some practical troubles were encountered. However, the important one is the formation of the SiO_2 thin oxide layer on the soft surface of the Si during the formation of the back contact. The silicon wafer is subjected to different chemical treatments in order to remove the thin oxide layer from the silicon wafer surfaces. Then the sequence of fabrication the on Al – CdTe/Si (p) –Al structure is as follow:

1. Deposition of Al back contact.
2. Formation of the back contact by annealing process at 200 ^{o}C for an hour (under vacuum).
3. Deposition of CdTe layer.
4. Deposition of Al top contact.

During the formation of the back contact, a thin oxide layer (SiO_2) is grown undeliberately. The existence of this layer is investigated practically by fabrication of Al–Si–Al structure with back contact formation as in steps 1 and 2 above, after which a top contact Al is deposited. Fig. 3 illustrates the (I-V) characteristics of the device, which exhibits a diode effect that consequently indicates the formation of a MOS diode (Al - SiO_2-Si –Al). The existence of the oxide layer badly affects the (I-V)

characteristics of the structure Al – CdTe/Si (p) – Al. Fig. 4 depicts the (I-V) characteristics of the CdTe/Si with the interfacial oxide layer with different CdTe thicknesses. It can be deduced that the characteristics are not of a PN junction (no rectification effect) due to the interfacial oxide layer which prevents the establishment of heterojunction between CdTe and Si. Evidently the introduction of oxide layer increases the total absorption depth. This in turn utilizes the wasted portion of the solar spectrum, consequently increases the short circuit current [15, 16].

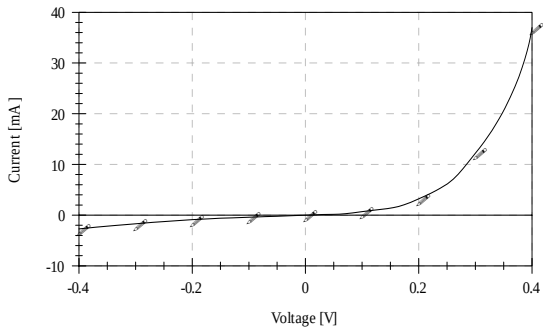

Fig. 3: I-V characteristics of Al-Si (p)-Al.

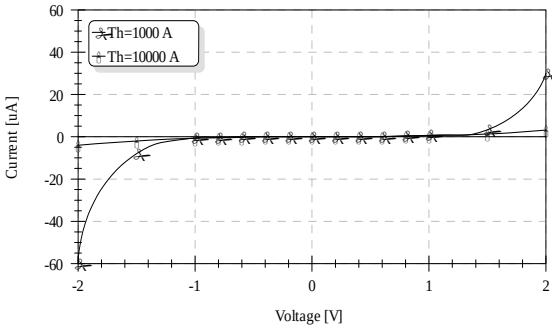

Fig. 4: I-V characteristics of CdTe/S I (p) with interfacial oxide layer for different CdTe thicknesses.

4. The effect of top contact material

Two metals are used as top contacts they are, indium and aluminum. Fig. 5 illustrates the dark (I-V) characteristics of the structure In˜-CdTe/Si (p) with two top contact materials: indium and aluminum in dot-shaped form. The two devices are fabricated under the same evaporation conditions and for the same time. It is observed that the device with indium top contact has a good rectification characteristic comparing with that of the aluminum top contact. Since the bending of the forward dark (I-V) characteristic towards the voltage axis is indicative of high series resistance [17], the conclusion that aluminum metal shows a high ohmic contact resistance to the In˜-CdTe (In-doped CdTe) is valid. The two devices had equal open circuit voltage of about 20 mV at 75 mW/cm^2 light intensity with very low short circuit current.

Fig. 6 depicts the dark (I-V) characteristics of the same structure but with indium and aluminum top contacts in grid form. It is noted that the device with indium top contact has also a good rectification characteristic supporting the conclusion that indium metal shows better ohmic contact comparing to aluminum metal.

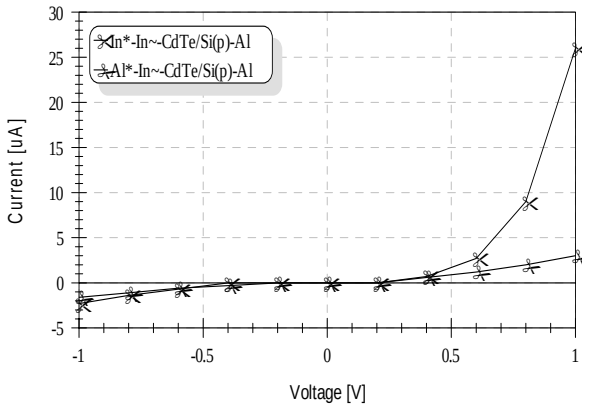

Fig. 5: I-V characteristics of In-doped CdTe/Si (p) for In and Al top contacts in dot-shaped form.

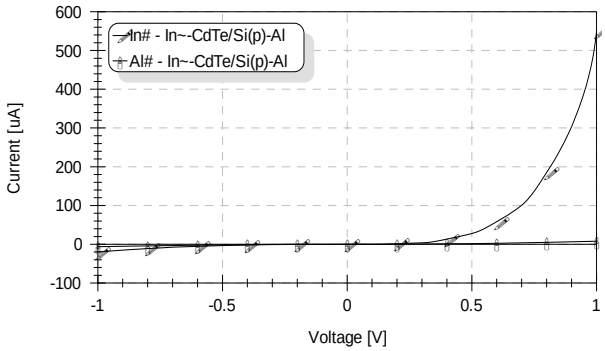

Fig. 6: I-V characteristics of In-doped CdTe/Si (p) for In and Al top contacts in grid form.

5. The effect of the device area

Fig. 7 illustrates a comparison between the dark (I-V) characteristics of device areas, 1 cm^2 and 3 mm^2. Indium is used as a top contact in grid form in the large area device, and in dot-shaped form in small area one. It is clear that the increase in the top contact area will increase the current flowing in the device due to the relatively low bulk resistance. It is found that the large area device shows an open circuit voltage greater than that of the small one, those are 36 mV and 20 mV respectively, at 75mW/cm^2 light intensity. The slight increase in the open circuit voltage by increasing the area of the device may be attributed to the increase in the photo generated current by

increasing the device area, which in turn increases the open circuit voltage.

6. The effect of silicon concentration

The dark (I-V) characteristics of the two structures In˜-CdTe/Si (p+) and In˜-CdTe/Si (p) are discussed. Fig. 8 shows that the leakage current in the former structure is more than in the latter. This effect can be explained in terms of silicon concentration as follows: in the case of Si (p+), the depletion region is narrow due to the high holes concentration in the silicon, while in the case of Si (p) the lowest holes concentration results in a wider depletion region and consequently the lowest leakage current. The device with Si(p+) has shown an open circuit voltage of 100 mV at 75mW/cm^2 light intensity due to the increase in the holes concentration in the silicon which in turn increases the junction abruptness that increase the open circuit voltage.

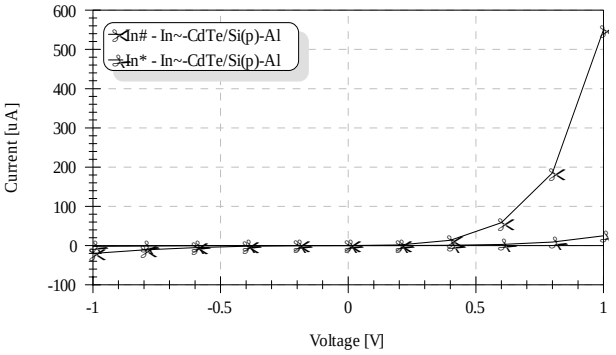

Fig. 7: I-V characteristics of In-doped CdTe/Si (p) for In top contacts in dot-shaped and grid forms.

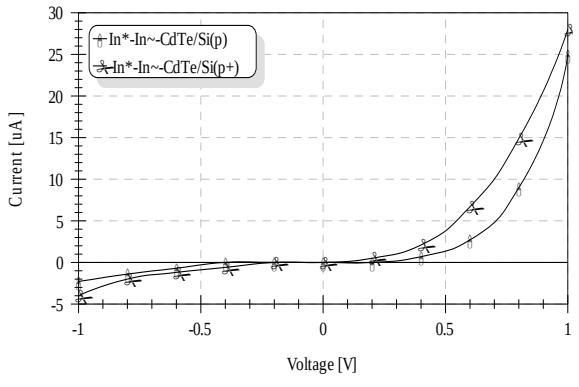

Fig. 8: I-V characteristics of In-doped CdTe/Si(p) and In-doped CdTe/Si(p+) structures.

7. Electro forming phenomenon

It is found that at high electric field the (I-V) characteristics behave strangely. Fig. 9 shows such behavior. It is observed that there are two states of conduction, non-conducting state represented by the curve AB and conducting state represented by the curve CD. The normal case is the non-conducting state. As the forward applied voltage increases beyond threshold value (7 V), it switches into the conducting state and remains in this state even after the voltage drops to zero. This behavior is similar to the electroforming phenomenon observed in metal-insulator-metal structure that is explained in terms of filamentary conduction model [18]. In this model, the conduction takes place through highly conductive filaments that are creating during the Forming process, that bridge the insulating layer between the electrodes. Here the insulating layer consists of two sub-layers, the oxide layer and the semi-insulating CdTe layer. It is observed that when the samples remain under conducting state for several minutes, during which high current flows through the sample, the samples drops to its non-conducting state suddenly. This may be attributed to the rupturing of the conductive filaments due to the relatively high local temperature arises from high current flow. This phenomenon is observed for several samples prepared with different CdTe thicknesses.

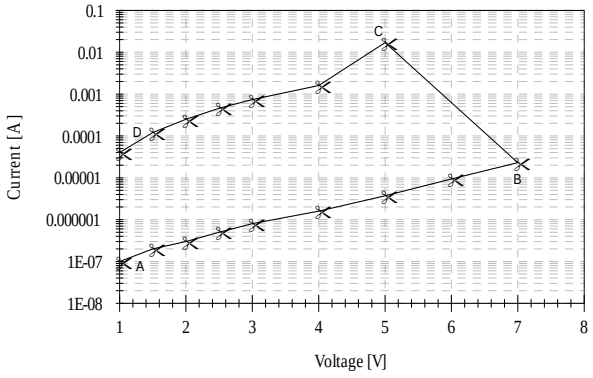

Fig. 9: Forming effect in CdTe/Si (p) with interfacial oxide layer with CdTe thickness of 5740 ^{o}A.

8. Conclusions

The heterojunction structure In-doped CdTe /Si (p) has poor photovoltaic properties due to the high resistivity CdTe film and to the large mismatch between CdTe and Si. It is observed that the Indium metal makes a good ohmic contact to the In-doped CdTe thin film comparing with the Aluminum metal. The heterojunction In-doped CdTe/Si(p+) has shown a relatively high open circuit voltage comparing with that of the Si(p) substrate due to higher junction abruptness that improve the photovoltaic action in the structure. Finally, an electroforming phenomenon has been observed in the CdTe/Si(p) heterojunction which may be considered as a memory effect.

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