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Programming speed, cycle-life and failure mechanisms in binary and multistate ovonic (phase-change) chalcogenide memory devices

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Sensitivity of resistance-current characteristic and programming speed to material and geometry of electrical contacts is demonstrated for same chalcogenide memory alloys. It was established that set speed is more sensitive to changes in top (positive) contact properties. Reset speed was found mostly dependent on bottom (negative) contact lateral properties: electro- and thermo-conductivity. Single fundamental failure mechanism: deterioration of programming speed is suggested. Failure modes and mechanisms specific only for multistate memory together with several practical ways of either using failure phenomena of avoiding failure are described.

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1. Introduction

Modern nanoelectronics demands significant increasing of functionality of a volume unit of device. The traditional paradigm of using relatively simple phenomena in complex interconnection of elements has approached its fundamental limits, and the time is coming for a new paradigm of using complex intrinsic phenomena in a simple interconnection of elements. One of these phenomena is bulk S-type negative differential conductivity (S-NDC) accompanied by electrical instability and appearance of high-current density filaments, which causes switching in vitreous chalcogenide materials [1,2]. Since it has been proven experimentally that electrical switching in threshold and memory devices [1] was a bulk phenomena [3] chalcogenide alloys became one of the prospective materials for future micro- and nanoelectronics [4].The bulk nature of S-NDC means that any separate nanovolume of material, if it exceeds characteristic size, possesses the ability for S-NDC [2-5].

As programming speed and cycle-life are among the most competitive parameters of chalcogenide-based phase change memory (PCM) devices, much effort was devoted to finding fundamental mechanisms, specific to chalcogenide alloys, governing these features. Detailed study of programming speed of PCM [6] established the crucial role of contacts and interfaces in defining limiting factors on set and reset pulse width and on the kinetics of phase transformation specific for electrical PCM. Experimental study of failure behavior common for both types of PCM devices demonstrated that, besides failure modes associated with lost contact or read disturb which are typical for all electrical devices [7], there are two failure modes of fundamental nature specific for all chalcogenide phase-change devices: failure to set and inability to reset [7-12]. Previous investigations of PCM devices demonstrated the multiplicity of failure modes but limited understanding of the failure fundamentals even for chalcogenide binary memories. The features and the nature of failure mechanisms specific to multistate memory devices [11] are yet to be revealed. This paper reports new data critical for understanding of programming speed, cycle-life and failures of PCM devices, role of contacts and isolation properties.

2. Experimental results and discussion

PCM devices after being subjected to high temperature during deposition and contact application have all bulk of memory alloy in a hexagonal crystalline phase with conductivity 2-3 decades higher than fcc cubic modification, whose conductivity is in turn 3-4 decades higher than the one for disordered state of the same alloy when it becomes either amorphous or vitreous depending on composition and the quench rate. Out of these three structural modifications, only the disordered one posesses the ability for electrical switching, while in two others, only thermal breakdown is possible. In thus produced device only the active region of electrical current propagation is experiencing the phase change. The rest of the alloy's volume keeps passively the state of very high conductivity and should be considered as a virtual contact. If the vitreous region adjacent to the bottom electrical contact (BEC) does not protrude through all interelectrode distance, top electrical contact (TEC) should be the same for different TEC materials. Indeed vitreous-hexagonal chalcogenide interface could be very strong [13] and its existence has been indirectly proven by experiments on dumbbell line devices in which other types of interfaces were impossible yet large ~ 1V offset voltage was routenely observed in experiments with the line-length dependence of threshold voltage [14].

2.1 Resistance-Current (RI) and Current-Voltage (IV) Characteristics. Contact Material and Geometry

Data presented below are for devices with $Ge_2Sb_2Te_5$ (225) alloy and Carbon contacts (Fig.1a), and for 225 devices with either continuous bottom metal contact: lateral contact devices (LCD) (Fig.1b), or pore-sidewall Ring-Contact Devices (RCD) (Fig.1c). In BDL BEC and TEC material was Carbon. In BDL devices pore area was defined by breakdown current value and the consecutive interface forming process [15, 19]. In lateral devices [6, 15, 20] pore area was defined by e-beam lithography. In ring contact devices the bottom contact area is a product of bottom electrode thickness and the pore perimeter and it could be changed two ways: the ring diameter by e-beam lithography and the ring thickness by metal deposition [17]. Top electrical contacts (TEC) for all three devices were either Carbon or metal. All devices have been produced at ECD. Resistance – current (RI) and current – voltage (IV) characteristics of devices (Fig.1) taken with square pulses from high resistance (reset) state are shown on Fig.2.

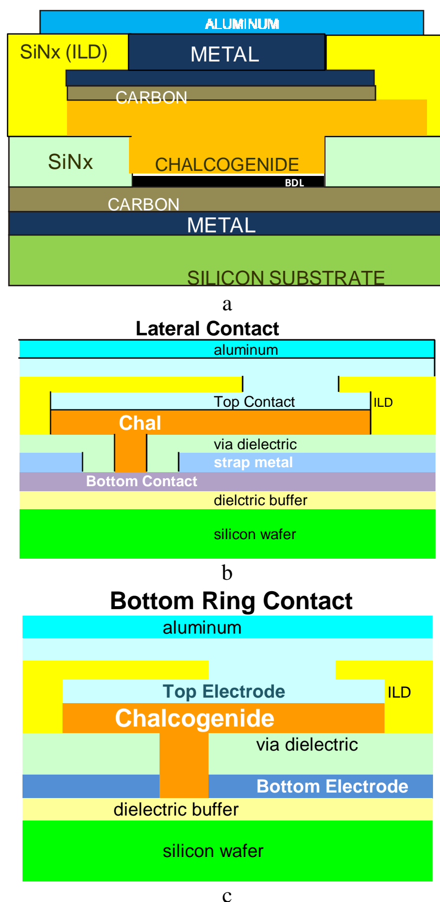


Fig.1. PCM devices produced by ECD. a) Break-Down-Layer (BDL) device C-C-contacts. b) Lateral metal contact device; c) Bottom ring metal contact device. Bottom electrical contact (BEC) thickness and ring perimeter are two dimensions of BEC area.

RI shape and IV parameters noticeably depend on contact material and its positioning (Fig.2). For BDL device, which has Carbon TEC and BEC and usually is being formed after making breakdown pore, RI looks symmetrical with similar moderate slopes of left-hand and right-hand parts and with low contact resistance dV/dI. For LCD one can see "soft" left-hand side of RI but very steep right-hand side of RI and higher dV/dI corresponding to a lateral resistance of BEC. Removal of metal from the pore bottom to manufacture a ring device brings significant changes to the right-hand side of RI: it becomes "soft" with single exponential dependence of R over I. This type of device was used to get 16-states RI published everywhere.

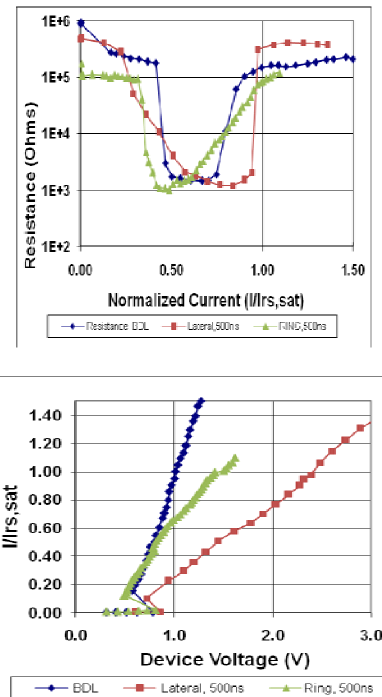


Fig.2. Typical resistance-current (RI) and current-voltage (IV) characteristics of devices from Fig.1. Thickness of chalcogenide was the same (50 nm) but areas were different.

2.2 Reset speed

The difference between these three contact materials and configurations was especially dramatic when speed of programming was being studied. Reset speed was measured by applying double pulses: optimized set pulse with fixed amplitude and width followed by reset pulse. The reset pulse width used was 10ns - 500ns with its amplitude as a parameter. The low field device resistance is measured with a small DC bias after each pulse. Fig.3. shows reset resistance vs. corresponding pulse width and amplitude for types of devices Fig. 1 made with the same chalcogenide alloy but with different geometries and different contact materials [6]. Comparing these figures, one can see a qualitative difference in the RESET programming between device types.

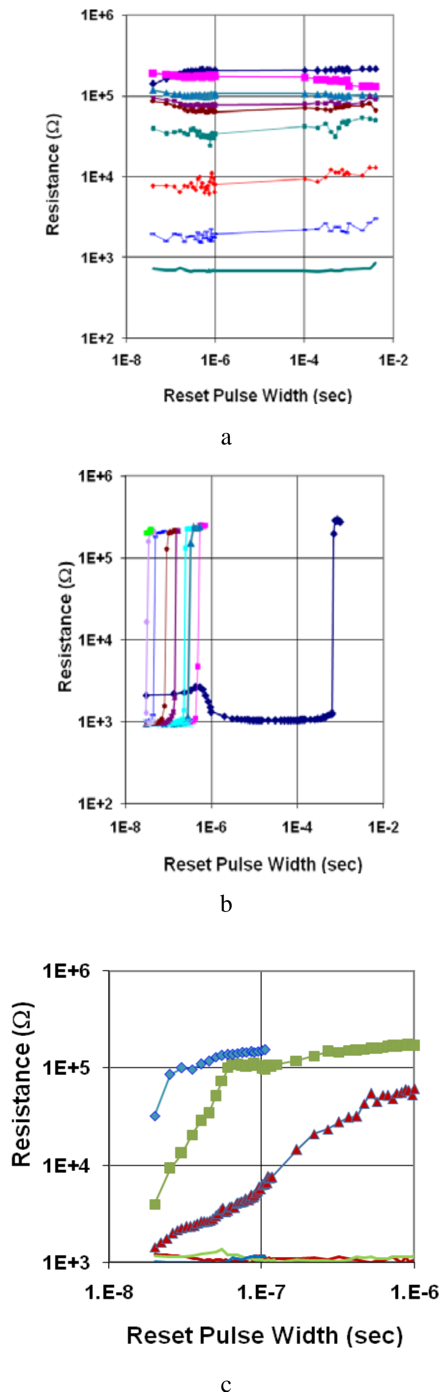


Fig. 3. Reset resistance vs. Pulse width with different reset current. Programming was always done with preceding set pulse. a) For a break-down-layer device with C-C contacts; b) for a lateral device with metal bottom and top contacts; c) for a ring-contact device with metal bottom and top contacts [4].

In the BDL devices, Rrs shows no dependence on reset pulse width and varies ONLY with the reset pulse amplitude. In other words, BDL device demonstrates that in the range of pulse width 30ns – 10ms, only the pulse current programs the device into a reset state and defines the Rrs value. In the lateral device, the RESET data are completely different. In this device, Rrs depended only on the pulse width and was independent on current amplitude. It means that RI of LCD may be misleading: it simply shows that at fixed reset pulse width, one needs to find the current corresponding to this pulse width. RCD demonstrates an intermediate behavior with Rrs dependent on both programming current value and square pulse width. With high enough programming current, RESET speed on all types of devices has approximately the same value. Fig. 4 presents reset speed (pulse width) with different reset current normalized by fixed set current (I_{set}) for each device.

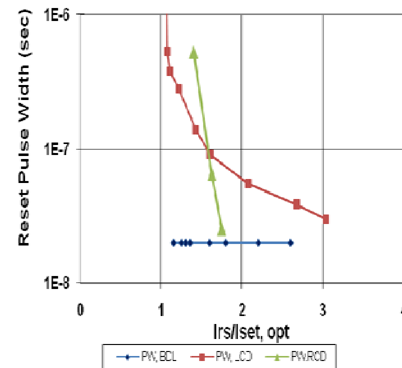


Fig.4. Reset speed dependence on programming current normalized by optimized set current for breakdown layer with Carbon contacts (BDL), lateral metal (LCD) and ring metal contact (RCD) devices.

As can be seen BDL device speed is maximal with any value of I_{rs}/I_{set} ratio, for LCD this ratio should exceed 3 and for RCD – 1.8. The question is: what influences reset speed. Common point of view is that in order to reset PCM device one has to melt and quench chalcogenide alloy. So heat loss through contacts and interfaces becomes especially significant. Let's assume that major heat dissipation occurs in the region adjacent to the smallest area contact, the bottom one and compare heat-loss properties of our devices. Obviously the heat-loss through a contact would be proportional to its resistance or the slope of IV of PCM device and to the interface barrier or holding voltage of device minus holding voltage of a bulk of a chalcogenide [16]. As alloy was the same in all types of devices, we may neglect $V_{h,GST}$ and assume that all the difference in V_h comes from the interface. IV's parameters for three device types are presented in Table 1.

Table1. Parameters of IVs Fig.2 of devices Fig.1.

Device	dV/dI (Ω)	V_h (V)
BDL	300	0.6
LCD	550	0.5
RCD	650	0.35

The highest reset speed corresponds to device with the lowest dV/dI but with the highest V_h. To explain the

difference in V_h one has to assume that vitreous zone touches both BEC and TEC. Thus interface vitreous-hexagonal chalcogenide may be excluded. There could be several other explanations to that, but only the following was backed up with the experiment: Carbon contacts, which are deposited amorphous, do form and after that they have low resistance along the current path but keep higher electrical and thermal resistance across it [6]. This statement is based on the experiment with C-SiNx-C device deposited in a BDL device configuration [6]. As current passes through the device, it becomes more and more conductive. Starting with resistance 1M, after breakdown, the resistance drops to 10K. Further increase in current causes the resistance to drop to 1K and finally to 100 Ohms. Annealing these devices at 350C for 72hrs brought no further resistance changes. In LCD and RCD, side heat loss is defined by metal BEC which did not form and have constant resistance in all directions. Indeed Carbon contacts are quite unique as electrode materials. The uniqueness is based on the change of C from a relatively resistive material to a highly conducting one, but only in the vicinity of the contact region. Thus lateral heat losses through contact are minimized and this is what makes the difference between C-C BDL devices and TiAlN bottom contact lateral devices. Another difference of LCD vs. RCD and BDL devices is an additional side heat loss due to the presence of the strap metal layer on top of BEC just outside the pore.

In [6] it was reported that reset speed is little affected by top contact modifications but depends on the conductivity of the bottom contact and the memory alloy. For higher conductivity alloys reset speed was faster even with C-C contacts. Reset speed is defined mostly by lateral heat losses through the bottom contact and adjacent GST as shown by experiments with lateral conductive contact device and with lower resistivity material. Note that reset speed improves (becomes faster) if bottom contact uses TiAlN with higher resistivity without strap metal [6].

Thus for reset speed side-heat loss at the bottom part of device is the most influential characteristic and as we'll see later on it is also responsible for failures of devices to reset when cycling at very high repetition rate.

2.3 Set speed

To estimate set speed, correct set current must be found. Usually, it corresponds to the RI minima. Procedures of optimizing set pulse parameters when programming from reset state are presented on Fig.5 for BDL (a,b) and LC (c,d) devices. As one can see, there is some difference when set pulse amplitude was chosen on the left-hand side of RI with I_{set} equal or below $I_{set,m}$, corresponding to RI minima. With BDL device, set resistance depends not only on the set pulse width but also on its amplitude (set current goes up from right to left for Fig.5a, c and d; and goes up from bottom to top on Fig. 5 b).

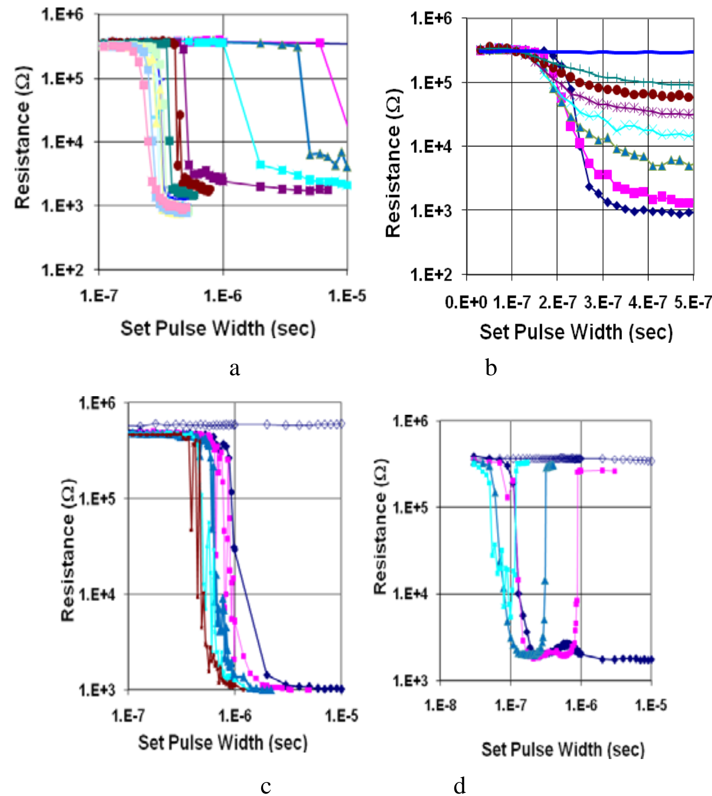


Fig.5. Crystallization from Reset State on Left- and on Right-hand Side of RI. BDL- Carbon (a,b) vs. Lateral –TiAlN (c,d). Set current goes up from right to left for Fig.5a, c and d; and goes up from bottom to top on Fig. 5 b.

For LCD again, as in case of reset speed situation, Rset does not depend on set pulse amplitude and only on set pulse width which decreases (Fig.5 b) with increasing Iset up to value corresponding to RI minima. The

difference between BDL-Carbon and LC-metal becomes dramatic if programming is done on right-hand side of RI when set current rises from the one corresponding to RI minima up to full reset value. For BDL-Carbon with increasing set pulse amplitude one gets well distinguished resistance levels as in case of reset programming from set state although with increased necessary minimum pulse width.

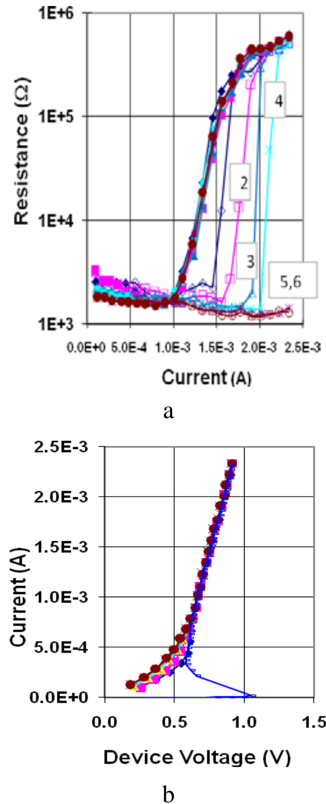


Fig. 6. Resistance-current (RI) and current-voltage (IV) characteristic of BDL device with C-C contacts programmed with double pulses: reset pulse of fixed width (200ns) and variable amplitude followed by set pulse with fixed amplitude (0.8 mA) and variable width (10, 2-20, 3- 40, 4- 80, 5- 160, 6-200ns).

This behavior tells us that for the direct overwrite with short reset pulses of variable amplitude one should use preliminary set. With LCD the situation is quite unique: with set pulse amplitude well above RI minima programming both set and reset states pulses may have the same amplitude but set pulse should be shorter than the reset one. In other words with the same amplitude one needs short pulse to bring resistance down from reset state but longer pulse with the same pulse amplitude will reset the device. Does device melt? Does it need to melt to amorphize? *This is the first time in PCM history that device has been programmed with reset pulse shorter than set pulse and both having the same amplitude thus questioning melt-quench mechanism of amorphization.* Fig.5c demonstrates that as set pulse amplitude increases set speed improves (device reacts to shorter pulses) but set-reset pulse width window narrows and finally shrinks. One thing is common though for both type of devices: at set current corresponding to RI minima Rset is the lowest with reasonably short set pulse width and this approach will be used in the following experiments which are described here only for BDL-Carbon devices.

Several set speed measurements methods were used. In the semi quantitative method (Fig.6) RIs and IVs were measured for BDL device which was programmed with two consecutive pulses: the set one with fixed current (~ 1 mA) and variable width (10 – 200 ns) and the reset pulse with fixed width (200ns) and variable amplitude. The aim of this experiment was to find the min. width of set pulses setting the reset device with variable reset resistance. Data are presented on Fig.6. Pass 1 on IV was performed with only reset pulse without the set one. As one can see increasing reset resistance causes set pulse width to rise in order to reduce resistance to the set level at all Rrs values.

In another, more quantitative method, the same operation has been performed automatically. To be able to compare different passes and different devices a target set resistance ($R_{set,target}$) must be defined. After that a program increases set pulse width till $R_{set,target}$ is reached. At this point the program goes to another step of increasing current of a fixed width (20ns) reset pulse. The SET-PW required to set below the $R_{set-target}$ is plotted vs. Irs together with the RI curve and is shown in Figure 7a.Saturated values of Rrst are determined from the device RIs, and thus $I_{rst,sat}$ and $I_{rs,sat}$ + 20% "over-reset" are estimated [6].

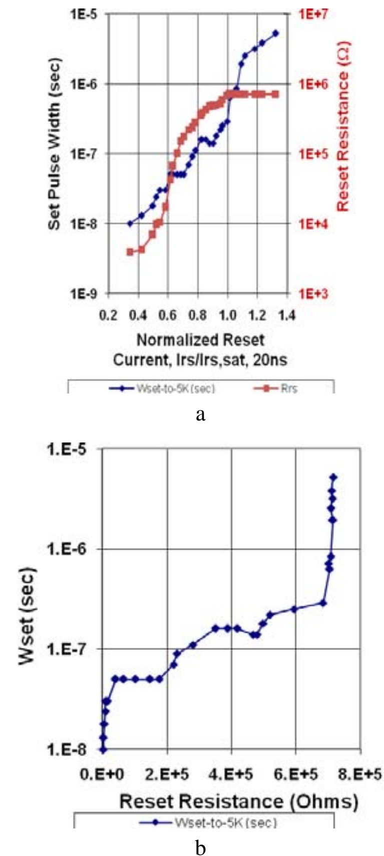


Fig. 7. Set pulse width (W_{set}) dependence on programming reset current (a) and on reset resistance (b). Square pulses, BDL device with C-C contacts [4].

In [6] has also been shown that R_{rs} scales with GST thickness but R_{set} doesn't. It is natural to assume that in this case Rset-dV/dI is mostly an interface resistance at low field. As was mentioned above, crystallized regions acted as a virtual contact to the top electrode interface. Thus W_{set} is not just a crystallization time but also a time for the crystalline region to reach a certain volume and make wider virtual contact to the electrode interface to meet $R_{set,target}$ criteria. This interface is seems to be located at the top contact of the device and when we make it weaker with less resistive top contact or more conductive memory alloy material we increase the set speed. Polarity experiments on devices with different BEC and TEC areas also point at this location of interface resistance. Thus OUM devices could be programmed with higher set speed if the interface resistance is reduced (less resistive) either by choosing more "Ohmic" top contact or using lower resistivity memory alloy or both.

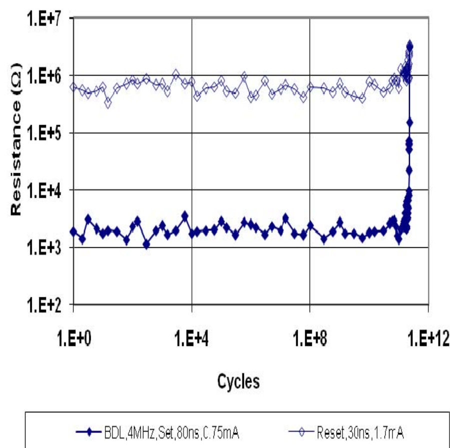


Fig.8 Possible mechanisms of "failure to set" mode. Reduction of set speed with increasing reset resistance. 225 BDL devices with Carbon contacts.

From the above data and results of previous experiments [6] the following conclusions can be made:

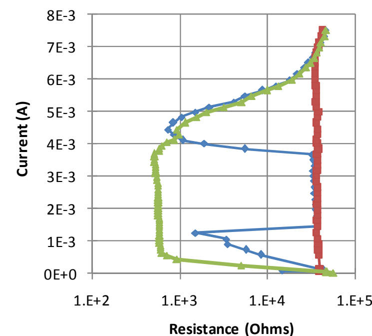
- Reset speed is little affected by top contact material and its resistivity.
- Reset speed depends on the conductivity of the bottom contact. Reset speed becomes faster (shorter pulses) even in LCD configuration if bottom contact uses TiAlN with higher resistivity without strap metal
- Reset speed is probably defined by lateral heat losses through the bottom contact and adjacent GST as shown by experiments with lateral conductive contact device even with lower resistivity memory alloy.
- The bottom contact material and its resistivity have little influence on set-speed.
- For 225 alloy Carbon TEC reduces set speed (increases set pulse width) especially with overreset (Irs ~ 1.2Irs,sat). Changing to a lower resistance alloy improves set speed at 1.2Irs,sat.
- Addition of a Ti layer to the top contact reduces V_h and greatly improves set speed but has no influence on reset speed.

2.4 Cycling failure mechanisms

Cycling is usually performed with square pulses at high repetition rate (~10MHz) to reduce the test time. Devices are first reset with pulses ~ 20 ns and then set with pulses ~ 50 ns. The best BDL devices with Carbon contacts sustained more than 10^{13} write-erase cycles. The most common deterioration modes are: failure to set, failure to reset, and failure to do both. At the initial stage of study it was established that the most influence on the failure to reset mode has reset process. Cycle-life with or without set pulses is the same.

2.4.1 Failure to set

Devices failed to maintain stable low-resistance or set state. Some researchers attribute these phenomena to failure to crystallize as they are often associated with increasing the reset resistance. To make this statement correct it should be added: "at a given width of square set pulse". Indeed dependence of pulse width to set device to desired resistance (W_{set}), with different reset resistance presented on Fig.7 demonstrates a sharp rise of set pulse width at already saturated reset resistance value. This type of set speed deterioration may occur due to increase of the interface strength and/or reducing density of crystallization nuclei [5,19]. If the time of cycle-life experiments was sacrificed and longer "set-sweep" pulses [18] were used, this type of the failure mode might not be observed.



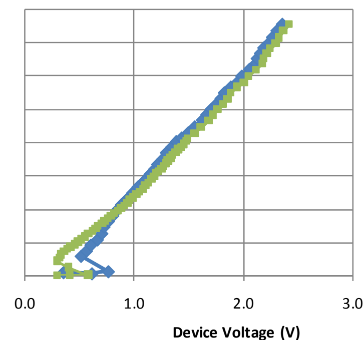


Fig. 9. Failure to crystallize: Dead-space in programming of devices with contact dimensions close to subcritical for electronic filament formation. One RI with single variable current set pulse without fixed reset pulse (green) and several consecutive RIs with double set-reset pulses on Side - Pore - Ring devices, c) IV shows only one switching.

Another possible type of set failure (Fig.9) is specific only for devices with at least one very small dimension of a cross-section. It is a so-called “dead zone” and it is due to suppression of initial high-current density filament when the device “exits” the current range of S-NDC but average current density has not reached the programming level [19,20].

2.4.2 Failure to reset

Devices failed to amorphize or to be programmed into high resistance or reset state. The data for BDL device with carbon BEC and TEC with set pulse width 50 ns and reset pulse width 25 ns and repetition rate 6.6 MHz are presented on Fig. 9. One can see that programming conditions were quite good for the device to cycle comfortably up to 1.5 10^{13} set-reset times. After that additional ~ 10^{8} cycles have brought reset resistance down to set level.

There are several possible fundamental reasons for the cycling device to lose the ability to change the phase from conductive or crystalline to resistive or vitreous:

- Increasing the time of amorphization.
- Decreasing of quenching speed.

Increasing the amorphization time

BDL device is a “mushroom” type device i.e. chalcogenide film is contacted with small effective diameter (~ 200nm) BEC and very large diameter TEC (1000nm). In a virgin device all chalcogenide is in hexagonal modification with very high conductivity and at the first programming event the mushroom of amorphous material is created covering BEC and adjacent regions. In this context increasing of the amorphization time means growth of the time of melting of crystalline material over the whole bottom contact and adjacent areas where crystalline shunts may be present or recreated.

Even if set state was caused by a single crystalline chain and was being molten by electronic filament formed around it melting temperatures in the filament center would be accompanied by crystallization on the filament periphery due to lower current density and temperature there and new crystalline chains would be created till the filament edges would be pushed far outside the BEC.

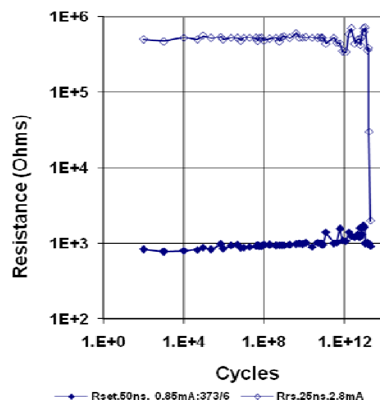


Fig.10. BDL device with Carbon contacts fails to amorphize at initial reset conditions.

Usually the distance should be above chalcogenide film thickness. To slow this process one should either increase the effective area to be covered by amorphous material or increase the heat loss from BEC. In the next experiment BDL device was cycled initially with reset pulse width of 15ns and with amplitude of 1.02 of $I_{rs,sat}$ (Fig.10). After 1 10^{10} cycles Rrs started to go down. Gradual increasing of reset current up to 1.2 $I_{rs,sat}$ brought up temporary restoration of Rrs for almost a decade of the cycle-life followed by Rrs gradual decrease. After Rrs was reduced to 3K I reduced I_{rs} to $I_{rs,sat}$ but increased pulse width to 40 ns. This action immediately restored initial value of Rrs and device continued to cycle for another 2 10^{10} cycles when experiment was stopped. These data rule out the hypothesis of increasing the time of quenching as the failure mechanism for losing the ability to vitrify because when pulse width is increasing with decreasing of Irs the quench rate did not seem to be affected.

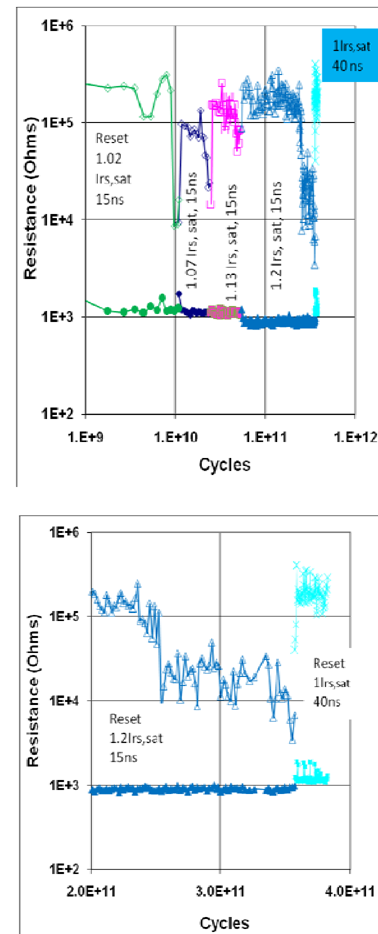


Fig.11. Restoring the value of reset resistance by increasing separately the reset pulse amplitude and width of reset pulse from 15ns to 40ns with constant or lower reset current. BDL device C-C-contacts.

Above it was established that reset current value strongly affects the reset speed for devices with different contact material and geometry and in next experiment the attempt was made to find out if it was possible to keep

reset speed at initial level by changing reset current with constant reset pulse width (20ns). The data is presented on Fig. 12 and show that 4 times increasing of reset current is needed to keep reset resistance around 100K above 3 10^{13} cycles. Such a huge rise of reset current is unrealistic but this experiment has shown two significant features of BDL chalcogenide PCM:

- The reason for devices to fail to amorphize at given width and amplitude of reset pulse could be a reduction of the reset speed.
- A fundamental degradation for BDL device happened NOT because changes in the chalcogenide alloy but was due to increasing of the insulator conductivity in the vicinity of the hottest spot surrounding the bottom contact.

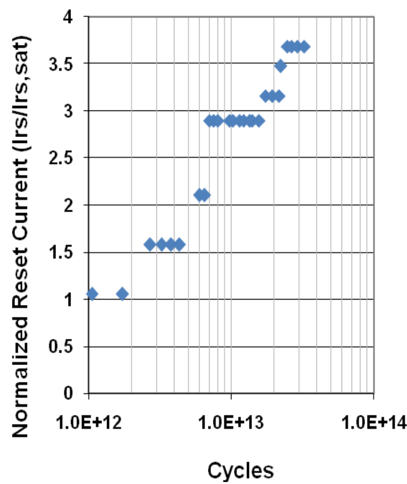


Fig.12. Reset current increase to restore value of Rrs and to keep it at certain level. BDL wired device. Wreset = 20ns Programming Current to Maintain Constant Value of Reset Resistance vs. Cycle Life for OUM with Rrs Drop.

Data presented in Table 2 suggest that change in effective pore size and of lateral heat flow might be responsible for the effect [25].

Table 2

Virgin Resistance of Carbon-SiNx-Carbon Devices. DC read 0.2V.	Resistance of virgin C-SiNx-C after annealing at 350C for 72 hours. DC read 0.2V.
1.7e6	1.3e5
1.2e6	9.1e4
1.4e6	9.4e4
9,6e5	8.5e4

Indeed as can be seen from table 2 annealing virgin devices at low temperatures of 350C causes their conductivity to increase more than 10 times. During reset pulse the chalcogenide and SiNx in the vicinity of the break-down region reaches temperatures 650-700C and when device cycles with repetition rate of 7 – 10 MHz rise in SiNx conductivity will increase the effective pore size and to restore Rrs value gross change of programming pulse parameters might be needed as it is demonstrated in Fig. 12.

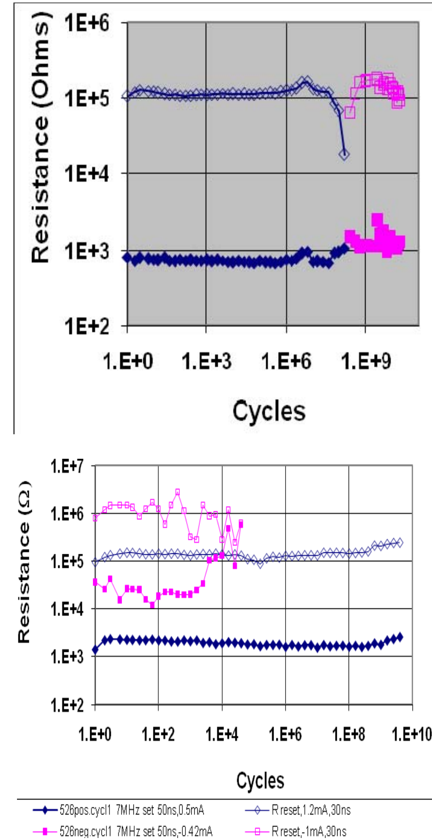


Fig.13. Reset resistance increase and cycling restoration by application of a single reset pulse of opposite polarity (negative). Cycling with only positive pulses followed with cycling continuation with only the negative ones.

Yet another way of restoring degrading reset resistance is to apply one or several pulses of opposite polarity to a device that started to reduce Rrs. Initial programming parameters were also restored. Cycle-life of this device with initial programming pulses amplitude and polarity was increased by another two decades [19]. Fig. 13 presents the data. Similar results were recently reported in [11]. On one hand the effect has a signature of electrical migration on the other hand with positive polarity cycling it takes ~ 10^8 cycles to reduce Rrs but application of only one reset pulse of negative polarity restores Rrs and helps the device to prolong its cycle-life for another 2 – 3 decades. The effect was observed on devices with different alloys and contact materials.

The method for reset resistance increase and cycling window restoration by application of a refreshing pulse: single reset pulse of opposite polarity (negative) was developed for phase-change memory devices [21]. As is

seen from Fig. 12b negative-pulse polarity cycling is very poor for no apparent reason.

Express-cycle method of PCM technology evaluation

Due to low temperatures of vitrification and crystallization specific for chalcogenide alloys standard methods of high temperature annealing are not applicable to PCM. Low temperature express method for the estimation of the cycle-life of chalcogenide based memory devices was based on results reported in this section.

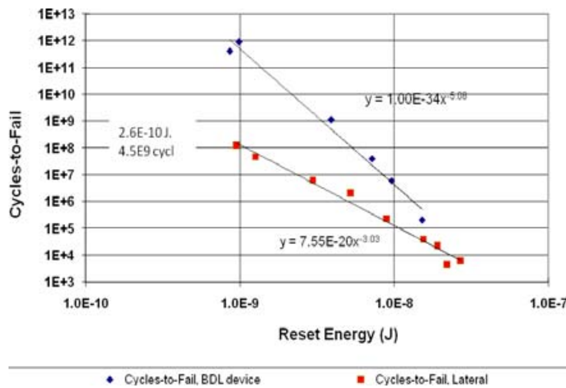


Fig. 14. Stress-Cycle Variable Energy Reset. No Set. Comparative Stress-Cycle Test of Break-Down Layer (BDL) and Lateral Devices (LD). Extrapolation of reset pulse energy to value expected for BDL device (~ 17 pJ) yields cycle-life of 10^{21}, for LCD expected reset energy is ~ 250 pJ and cycle-life is 5 10^9.

As it was mentioned above for the cycle-life failure mode which we discuss in this section the presence of set pulse preceding every reset pulse is not necessary. Cycle-life is the same with using set-reset pulses or only reset-reset… pulses. Also during experiments it was noticed that cycle-life strongly depends on the energy of reset pulse. These facts were used in designing the method for express-comparison of different alloys, contacts, isolation and configuration of devices [23,28]. Fig. 14 presents a comparison of dependence of cycle-life on reset pulse energy for BDL and for LC devices. The data could be fitted to the power law and the extrapolation to the normal operation reset pulse energy allowed to estimate the corresponding cycle-life. For BDL normal working reset pulse energy at room temperature is ~ 17 pJ and expected life is ~ 10^{21} reset pulses. Extrapolation of reset pulse energy to value expected reset energy for LCD ~ 250 pJ yields cycle-life ~ 5 10^9 resets. The difference could be associated with more aggressive interaction of chalcogenide alloy with metal contacts.

2.4.3 Failure to set and to reset. Multiple contacts.

When both set and reset pulses fail to program the device and Rset = Rrs at intermediate resistance value (Fig.15a). This failure mode is neither fundamental nor associated with the loss of write speed but has interesting features. From the shape of IV (Fig.15c) and RI (Fig.15b) of failed devices it was found that this type of failure was due to splitting of the initially uniform device into two or more parallel ones. Note typical multiple switching. Possible reason: partial oxidation of electrical contact. Device with multiple contacts which are switched in parallel could be easily distinguished from devices with the dead zone of programming by the shapes of RI and IV.

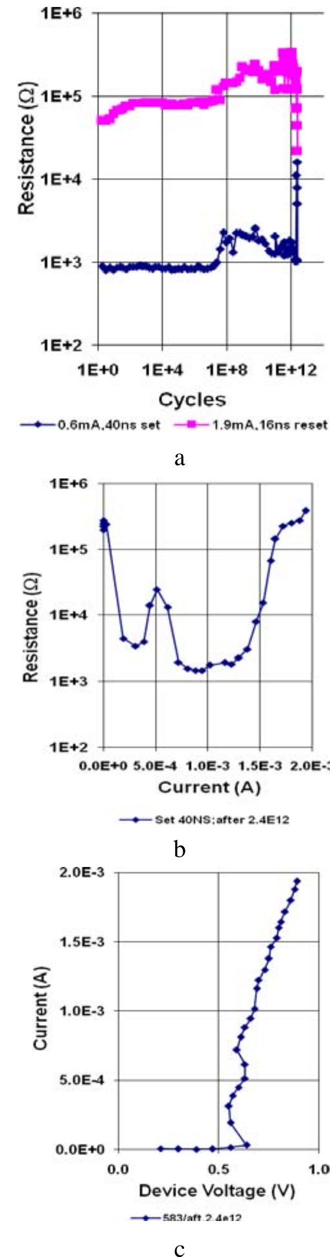


Fig.15. Splitting of PCM device during cycling. a) Device failed both to set and reset after 2E12 cycles; b) Failed device IV shows three switching events; c) RI with NO fixed eset pulse demonstrates 2 – 3 hump curve. Breakdown layer device with Carbon contacts.

Typical RI for this case taken with only set pulse without using fixed reset pulse does show two or more “humps” which is never the case for the device with “dead zone”(Fig.9). Also the difference in IV shape is very noticeable. Dead zone device has only one switching (Fig.9) meanwhile multiple contacts device could be distinguished by the presence of multiple switching on IV (Fig.15c).

2.4.4 Failure modes of multistate memory devices

Single failure mechanism: the loss of the set and reset programming speed is common in both binary and multistate chalcogenide-based devices; yet there are additional features, which are dangerous only for multistate devices. Those include:

- Changing the shape of RI curve with time or during cycling (Fig 16a);
- Hysteresis of RI when programming with fixed set or fixed reset pulses (Fig.16b)
- Drift of programmed resistance with time: $\mathbf{R=R_o (t/t_o)^d}$, where t_o is the time scale and R_o is the resistance at time $t = t_o$. With t_o = 1sec, the drift exponent dependence on initial programmed resistance is presented on Fig.16c [22].

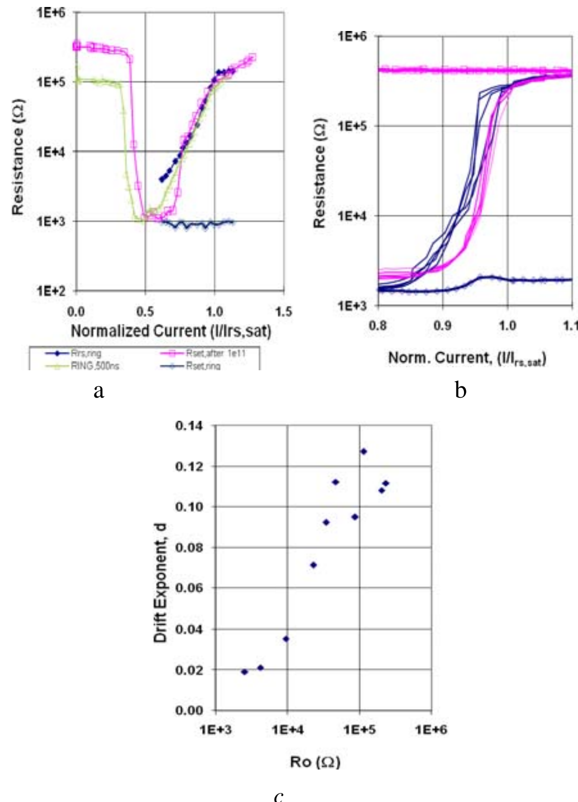


Fig.16. Failure modes specific for multistate PCM. Resistance-current plot for a ring-device with “soft RI” before and after cycling (a). RI’s Hysteresis (b). Drift exponent with different initial programmed resistance (c).

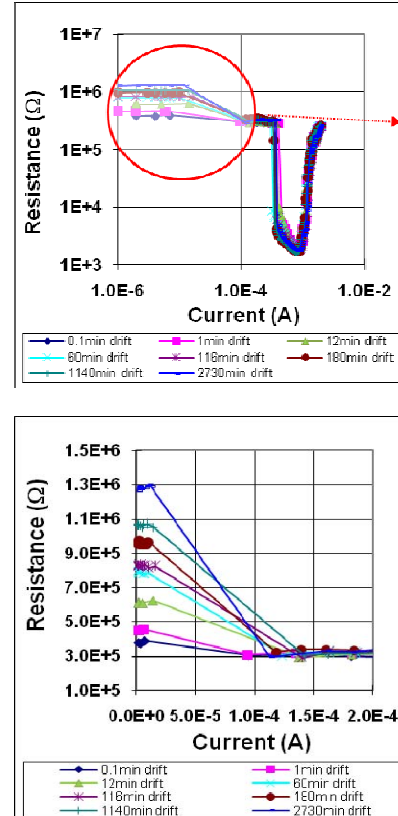


Fig.17. Drift recovery with low-current switching pulse.

New concept of drift was introduced in [22]. According to this concept the reason for drift is a mechanical stress caused by electrical switching preceding programming. These types of stresses have been reported in chalcogenides. The method was developed to remedy problem with the same phenomena that has caused it i.e. with switching at very low current. Ironically only this way to restart drift and to return the device to pre-drifted resistance value has been discovered and tested so far: it was low current switching [24,27]. The method is illustrated by Fig.17. All other proposed mechanisms of drift [26] describe and model it in great details but so far failed to produce a method for drift elimination.

3. Conclusions

- Higher reset speed of OUM devices is possible when lateral heat losses of a bottom contact and a chalcogenide material adjacent to bottom contact are minimized.
- Ability of amorphous Carbon to undergo a unidirectional change of resistivity only along the current path helps to effectively thermally isolate the device. The benefit of isotropic heat conduction, much higher normal to the surface than lateral makes

Carbon desirable for bottom electrode contacts.

- Top electrode contact material should be chosen based on the conductivity of a memory alloy adjacent to it to minimize low-field interface resistance, Vh, and set pulse width.
- Single fundamental failure mechanism: the loss of the set and/or reset programming speed is common for chalcogenides based PCM.

Improving reliability of multistate devices is possible by "softening" of RI by optimizing device geometry, the shape of programming pulse and the read pulse.

Choice of safe range of Rset, Rrs and Irs, of set pulse width and its shape improves PCM devices reliability without sacrificing yield;

Increasing of either reset pulse width (2 times from 20ns to 40ns with the same amplitude) or its amplitude (with the same or even lower pulse width), could restore desired value of Rrs.

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