Silicon light-emitting device for high speed analog-to-digital conversion

ZHENGPING ZHANG[a], KAIKAI XU[b,*], JUN YUAN[a], YUXIN WANG[a], KINGSLEY A. OGUDO[c,d], CARLOS VIANA[d], JEAN-LUC POLLEUX[d], QI YU[b], LUKAS W. SNYMAN[c], YONGLU WANG[a], RONGBIN HU[a]

[a]*Science and Technology on Analog Integrated Circuits Laboratory, Chongqing, China 400060*
[b]*State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, Sichuan, China 610054*
[c]*Department of Electrical Engineering, University of South Africa, Pretoria, South Africa 0001*
[d]*University Paris-Est, ESYCOM, ESIEE Paris, Le Cnam, UPEM, Cite Descartes, Noisy-Le-Grand-Cedex, France 93162*

Silicon Photonics is an emerging field of research and technology, where nano-silicon can play a fundamental role. Visible light emitted from reverse-biased p-n junctions at highly localized regions, where avalanche breakdown occurs, can be used to realize a visible electro-optical sources in silicon by means of light-emitting diodes (Si-LEDs) is reviewed by characterizing the spectral distribution. Regarding applications, a monolithic optoelectronic integrated circuit (OEIC) for on-chip optical interconnection based on standard CMOS technology is discussed. Although there are some of the present challenges with regard to the realization of suitable electro-optical elements for diverse integrated circuit applications, the type of silicon light source can be further developed into be a Si-based optical short-distance on-chip optical interconnect applications. Utilizing silicon electro-optic modulator, monolithic construction of photonics/electronics processing devices used in analog-to-digital conversion, and applications of it to ADCs, the state-of-art photonic technologies for Analog-to-Digital converters (ADCs) is presented.

1. Introduction

Silicon is the most widely studied material in the history of civilization. In fact, the present-day information age has dawned with an electronics revolution brought about by the maturity of silicon-based microelectronics. The growth of the silicon industry follows the no-famous Moore's law, which states that the number of transistors in an integrated circuit chip doubles every 18 months. However, during the last decade there has been an indication of the decline of Moore's law. There are doubts whether in future silicon-based integrated circuits (ICs) will deliver the same advantages and increased functionalities over time as in the past.

The p-n junction is the vital component of most semiconductor devices. In this chapter the concept of a light emitting p-n junction is developed and characterized. Many studies in the past have correlated breakdown occurring in silicon p-n junctions with impact ionization and with material and structure parameters, especially some radiative recombination occurs while electron-hole pairs are produced during avalanche breakdown. Both the electrons and the holes can be heated by the electric field. The radiative transition between hot carriers emits photons larger than the energy gap. Hence, the luminescence during avalanche breakdown is characterized by a broad emission spectrum that extends to the energy of ~3.36 eV (i.e., with the shortest wavelength of ~369.05 nm), which represents the energy separating the hottest electron from

the hottest hole. It is noted that ~3.36 eV is equal to $3E_g$ and the energy for impact ionization by a hot carrier is about $1.5E_g$. Substantial progress has been made in the field of silicon p-n junctions emitting visible light when operating in reverse-avalanche mode. The silicon-based light-emitting device (Si-LED), which is actually a simple p-n junction that is fully compatible with standard CMOS technology, is a potential light source that can monolithically integrated with the silicon-dioxide waveguide, photo-detector and receiver circuit on a single silicon chip. The wide spread use of SOI for PMIC and RF applications has added to the potential applications of Si-LEDs.

The weakest point of silicon is that proper light emitters and modulators can not be realized due to its indirect band gap. On the other hand, there is a steady advance in the field of photonics. Although discrete devices using the compound semiconductor materials and their alloys show very good performance, the levels of integration and performance are far below what has already been achieved in electronic integration on the same substrate. It is natural to expect that OEIC will provide the same advantages, that is, low cost due to batch fabrication, high functionality, scaling for denser integration, and so on, as provided by silicon ICs. Instead, if OEIC could grow on silicon and integrate with electronic ICs by using the same production facilities, the benefits to be accrued need no further elaboration. Si-based systems will then be used in all fields of electronics,

computers, and communication [1]. Therefore, Si-based photonics remains an active area of research and over the last 10-15 years some significant milestones have been achieved [2].

Another important area of application of silicon photonics is in very large-scale integrated (VLSI) circuits. The metallic interconnects, mainly Cu, produce delay due to resistor-capacitor (RC) time constants, which far exceed the transit time delay associated with the individual transistors. If the increase in speed is to be maintained at the same rate for the next-generation ICs, the interconnect bottleneck must be properly addressed. Optics is believed to be the right solution for the problem [3].

2. Two- and multi-terminal cmos/bicmos silicon led

Silicon photonics has become one of the most promising photonics integration platforms in the last decade. This is mainly due to the combination of a very high index contrast and the availability of silicon CMOS fabrication technology, which allows the use of electronics fabrication facilities to make photonic circuitry. Unfortunately, the indirect band-gap of silicon leads to low efficiency. The rate of electron-hole recombination in silicon material is too low to produce emitted photons in forward biased silicon p-n junctions, but light emission observed from reverse biased silicon p-n junctions under avalanche breakdown was reported in 1955 by Newman [4].

Ref. [5] shows a planar n^+p shallow-junction structure that is fabricated using a standard 1.2-μm CMOS process with no adaptations of the process at all. Excellent uniformity has been obtained for large area devices. Furthermore, it is demonstrated that the light levels and intensity levels generated from the devices are indeed useful for on-chip electro-optical coupling and for chip-to-environment electro-optical coupling.

In addition to the study of silicon diode LED in which the light emission is due to the avalanche breakdown of the silicon p-n junction, a novel gate-controlled diode MOS-like multi-terminal device is described where both the light intensity and spatial light pattern of the device are controlled by an insulated MOS gate voltage.

Indeed, a metal-oxide-semiconductor field-effect-transistor (MOSFET) consists of two identical gate-controlled diodes (i.e., "p^+ Source/Drain to n-Substrate", in a PMOSFET device) [6]. Since source and drain are grounded (i.e., $V_d = V_s = 0$ V), the reverse bias of the two p-n junctions is defined by the substrate voltage V_{sub} which is a fixed value. By changing the gate voltage V_g, the channel layer in the PMOSFET device can be categorized by the following three types [7].

a) Inversion layer

The gate voltage V_g varies while the substrate voltage V_{sub} is fixed. As shown in Fig. 1(a), the channel layer is a p-type inversion layer if $V_g < V_{sub}$. In addition, the concentration of the surface channel layer decreases with the increase in V_g.
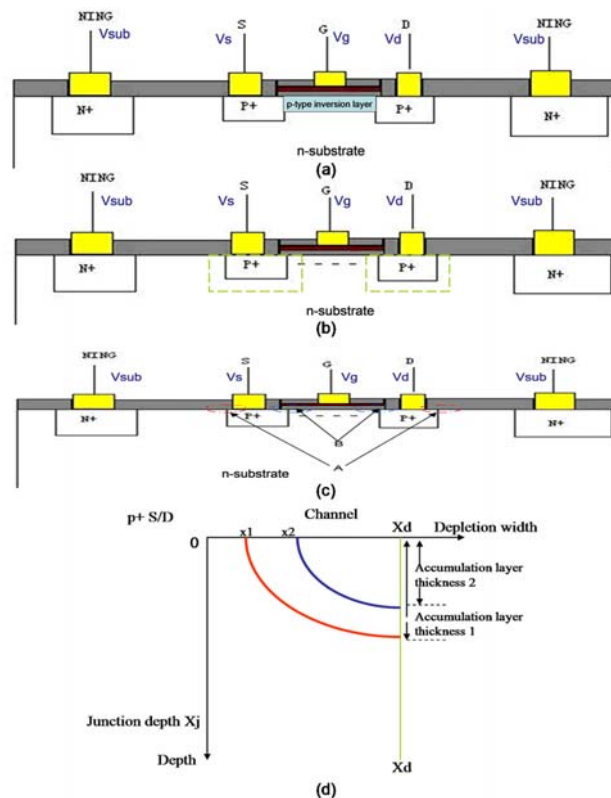

Fig. 1. The characterization of the channel layer: (a) inversion; (b) depletion; (c) accumulation; (d) depletion region width near the channel surface. NING denotes the terminal for the n^+ guard ring region.

b) Depletion layer

If the gate voltage V_g is high enough to be approximately equal to the substrate voltage V_{sub}, the p-type inversion layer will disappear in the channel and be replaced by the n-type substrate. As shown in Fig. 1(b), the depletion width of channel surface should be comparable to the depletion width of the "p$^+$ Source/Drain to n-Substrate" junction diode.

c)Accumulation layer

If $V_g > V_{sub} > 0$, electrons will move toward the channel surface. The greater V_{gsub} (i.e., $V_g - V_{sub}$) is, the stronger an n$^+$ accumulation layer will be generated near the surface channel. It is well known that the concentration of the layer is exponentially monotonic with a maximum at the channel's surface and a minimum that is equal to the substrate concentration at the bottom of the channel layer. The depletion width has the minimum at point B in Fig. 1(c) and the maximal depletion width equals the depletion width of the "p$^+$ Source/Drain to n-Substrate" junction, which is point A in Fig. 1(c). Fig. 1(d) provides more characterizations referring to point B which actually is the transition between the p$^+$ Source/Drain region and the channel layer underneath the gate. If $V_g = V_{sub}$, depletion width is unchanged as to be X_d (i.e., the depletion width of "p$^+$ Source/Drain to n-Substrate" junction in thermal equilibrium). If $V_g > V_{sub}$, the depletion width at the transition will decrease from X_d to x_2 because of the accumulation layer (n-type) with a thickness 2. If $V_g \gg V_{sub}$, the depletion width at the joint will continue to decrease from x2 to x1 and the thickness of accumulation layer will increase to thickness 1. Furthermore, $x_1 < x_2$ means that gate voltage V_g is proportional to the concentration of the surface channel.

Indeed, the accumulation layer the thickness is just a few tens of nanometers. For the MOS structure in the accumulation mode, the relationship between the gate voltage and the accumulation layer's concentration and thickness are analyzed below. A derivation of the accumulation layer thickness as a function of substrate doping concentration will show that the layer is very small and hence can be considered as a surface charge. The distribution of the charge as a function of depth, x, can be found using Poisson's equation [8]

$$\frac{d^2\Phi(x)}{dx^2} = -\frac{\rho}{\varepsilon_{si}} = -\frac{q}{\varepsilon_{si}}\left(p - n + N_d - N_a\right) \quad (1)$$

with

$$p(x) = p_{p0}\exp\left(-\frac{q\Phi(x)}{kT}\right) = N_a\exp\left(-\frac{q\Phi(x)}{kT}\right) \quad (2)$$

and

$$n(x) = n_{p0}\exp\left(\frac{q\Phi(x)}{kT}\right) = \frac{n_i^2}{N_a}\exp\left(\frac{q\Phi(x)}{kT}\right) \quad (3)$$

where p_{p0} is the equilibrium hole concentration in the p-type material, n_{p0} is the equilibrium electron concentration in the same material, and $\Phi(x)$ is the potential in the silicon as a function of depth. T is the carrier's temperature. Far from the surface of the silicon the potential is equal to zero: $\Phi(x \to \infty) = 0$, which will be used as a boundary condition for Eq. (1).

In the hole accumulation layer formed in p-type substrate shown in Fig. 1(c) on can assume that $n \ll p$ and $N_d \ll N_a$, thus Eq. (1) can be rewritten as

$$\frac{d^2\Phi(x)}{dx^2} = -\frac{\rho}{\varepsilon_{si}}N_a\left[\exp\left(-\frac{q\Phi(x)}{kT}\right) - 1\right] \quad (4)$$

where ε_{si}, the permittivity of silicon. From a numerical calculation, it is finally find that the thickness of the accumulation layer, x_{acc}, can be found using the condition that $\Phi(x = x_{acc}) = 0$;

$$x_{acc} = \sqrt{2}L_D\cos^{-1}\left(\exp\left(\frac{q\Phi_s}{2kT}\right)\right) \quad (5)$$

The thickness of the accumulation layer, x_{acc}, can thus vary between 0 and $\frac{\sqrt{2}}{2}\pi L_D$, depending on the accumulation charge. L_D denotes the Debye length.

Due to the increase in the concentration of accumulation layer and the decrease in the depletion width near the surface channel, the breakdown voltage *BV* of the "p$^+$ Source/Drain to n-Substrate" junction decreases with the increase in gate voltage V_g. Moreover, if the accumulation layer is approximated treated to consist of numerous n-type thin layers that are individually with their own concentrations, the PMOSFET being in the operating condition mentioned above is a combination of Zener breakdown p-n junctions and avalanche breakdown p-n junctions.

On the other hand, the mixture of Zener breakdown and avalanche breakdown (i.e., a transition from avalanche to tunneling) could be the major reason for the reduction in *BV* of the two parallel-connected p-n junctions (i.e., the "p$^+$ Source/Drain to n-Substrate" junction shown in Fig. 1) because it is known that the Zener breakdown voltage is usually much lower that the avalanche breakdown voltage. More specifically, at large positive gate voltages, a strong accumulation layer occurs and the surface electron concentration shields the electric field within the peripheral junction depletion region from the gate, reducing the effect of the gate voltage on avalanche breakdown in the "p$^+$ Source/Drain to n-Substrate" junction of the MOS-like device.

As discussed previously, a higher gate voltage V_g can induce the lower breakdown voltage *BV* of the two p-n junctions (i.e., the "p$^+$ Source/Drain to n-Substrate" junction in the PMOSFET device). Next, the reverse current I_{sub} flowing through the p-n junctions with breakdown mechanisms will increase with gate voltage V_g while the substrate voltage V_{sub} (i.e., the reverse bias of the two p-n junctions) is a fixed value [9]. Since the optical emission power is linear with the reverse current I_{sub}, increasing the gate voltage V_g is a significant method to realize electro-optic modulation in the three-terminal gate-controlled based MOS-like device [10-12].

It is noted that the Si-diode LED (i.e., the p-n junction is reverse-biased to avalanche breakdown) is a two-terminal device and the Si gate-controlled-diode LED (i.e., the reverse-biased p-n junction with varying the gate voltage) is a three-terminal device. In particular, a silicon light-emitting device (Si-LED) with the structure of a Si-PMOSFET device that is fully compatible with the standard Si-CMOS process technology experimentally demonstrates that the reverse current I_{sub} is always linearly proportional to optical emission power whether the Si-PMOSFET device acts as a two-terminal device (i.e., p-n junction diode, the "p$^+$ Source/Drain to n-Substrate" junction with floating the gate, Si-diode LED) or acts as a three-terminal device (i.e., gate-controlled diode, the "p$^+$ Source/Drain to n-Substrate" junction in the course of varying the gate voltage, Si gate-controlled diode LED). The optical power measured from the device is divided by the photon energy to obtain the number of collected photons, and then the external quantum efficiency is defined as the ratio of the number of collected photons to the number of injected electrons. Such linearity implies that control of the increasing current is a significant way to enhance the quantum efficiency of this light source device no matter what the physical structure (i.e., two or three terminals) of the device is.

3. Characterization of the optical properties

Assuming the classic Bremsstrahlung model is approximately applicable, the origin of optical radiation observed in the reverse-biased silicon p-n junction could be explained by the Coulomb interaction between impact ionized carriers and charged centers in the depletion region. The charged center, also known as quantum dot, is an artificial atom in fact even if it has a mass that is approximately equal to one atom. Beside the properties of atoms such as having discrete energy levels and shell structure, the artificial atom, quantum dot, including tenability and comparability of level spacing, Coulomb scattering, and thermal energy is more advanced than the natural atom by allowing transport measurement [13].

Since the number of carriers is proportional to the number of emitted photons, the number of light spots increases with the reverse current rather than individual spots growing brighter.
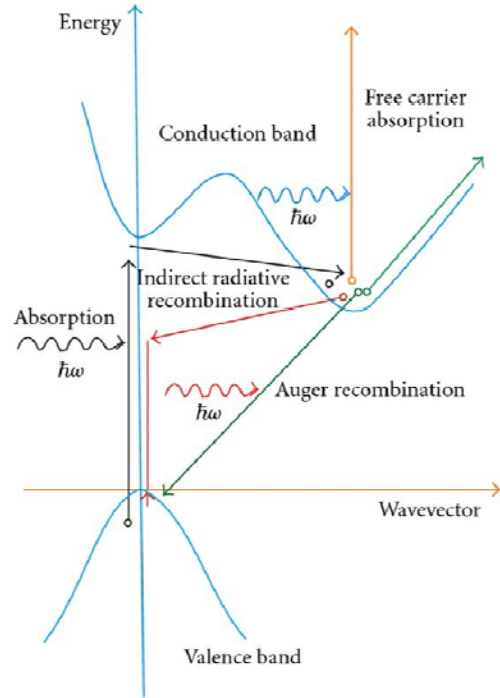

Fig. 2. Band structure of bulk Si with the various possible transitions for an electron-hole pair: radiative recombination, Auger recombination, and free - carrier absorption.

It is concluded that the avalanching current is carried through the junction by these localized emitting spots (i.e., quantum dots). Despite a great deal of theoretical and experimental work to clarify the mechanism of the strong visible luminescence from reverse-biased silicon p-n junctions, it still remains unclear because of this complication. Overall, the major mechanism is drawn in Fig. 2 and can be interpreted by the three different transitional processes below [14]:

a) Intra-band direct transition

Most hot carriers do not find suitable transition partners with the same vector in *k*-space for photon radiation transition. As a substitute, phonon radiation is the most possible result for getting back to a low energy state. The output light power per unit optical frequency is expressed as

$$I(v)_{Intraband} = C_1 (hv)^{3.5 \frac{1 - 3/\alpha}{2 + 3/\alpha}} \exp\left[-b(1.41 hv - E_0) \right] (6)$$

where C_1 is a constant, b is function of mean-free path, E_0 is the threshold energy for ionization, and α is a positive value that is related to the electric field and mean-free paths of ionized electrons and emitted photons [15].

b)   Intra-band indirect transition

This transition only occurs by the intervention of phonon assistance, in which phonons are radiated mostly by intra-band direct transition. Since the transition is the well-known Bremsstrahlung radiation (i.e., the scattering of an electron by an external field, accompanied by the emission of a photon), the output light power per unit optical frequency can be written as

$$I(v)_{Bremsstrahlung} = C_2 \exp\left(\frac{hv}{kT_e}\right) \qquad (7)$$

where C_2 is a constant, k is the Boltzmann's constant, and T_e is the effective temperature [16]. The optical radiation is induced by the inelastic collision (i.e., inelastic x-ray scattering) between carriers (e.g., electron and hole) and charged centers (e.g., artificial atom). The probability of finding a carrier in state E_B is

$$P(E_B) = \frac{\exp(-E_{ave}E_n)}{\sum_n \exp(-E_{ave}E_n)} \qquad (8)$$

which is known as canonical or Maxwell-Boltzmann distribution. Assuming the electric and magnetic fields each represents one degree of freedom, the average energy E_{ave} will be equal to kT_e.

c)   Inter-band transition

Under most situations, inter-band composition is the most effective process of photon emission. It must satisfy many conditions, such as same vector in k-space, direct transition of hot carriers. Commonly, the transverse momentum of a wave vector is written as

$$k(L_{e-c}) = \sqrt{\frac{2m_e}{\hbar}(PE - E_e)} \qquad (9)$$

where L_{e-c} is the distance from the electron energy to the center of band, m_e is the effective mass of electron, PE is the potential energy of the Si-SiO$_2$ barrier, and E_e is the energy of incoming electron. Further, the detailed form of $PE - E_e$ is given by

$$PE - E_e = \frac{(0.5E_g)^2 - (qE_y L_{e-c})^2}{E_g} \qquad (10)$$

where E_g is the bandgap energy of silicon and E_y is a vertical field induced by the gate-to-source/drain voltage drop.

It should be mentioned that silicon is a material with indirect bandgap. For indirect gap materials, the wave

vector dependence is essential in order to get a sharp peak in the emission spectrum of exciton molecules [17]. Accordingly, the output light power per unit optical frequency can be written as [18]

$$I(v)_{Interband} = I(v)_{Emission} - I(v)_{Absorption} \qquad (11)$$

Correspondingly, the electroluminescence spectra captured from the Si-PMOSFET device operating as Si gate-controlled diode LED by the optical spectrometer is given in Fig. 3. There is a distinct emission peak at 625 nm in the emitting wavelength range of 400 to 900 nm, and the light intensity increases with the gate voltage V_g. No obvious phenomenon of spectral shifting is observed with different operating voltages and currents.
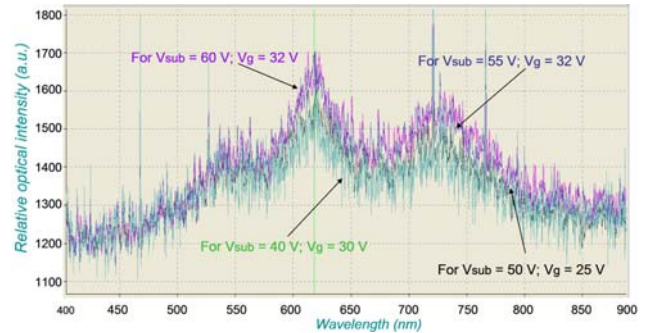

Fig. 3. Spectrum of the light emitted from the Si-PMOSFET device, fabricated by standard VLSI technology, on the same Si chip.

Ref. [19] proposed that intra-band transition, specifically Bremsstrahlung of hot carriers at charge centers. Ref. [20] associated emission with wavelength longer than 539 nm with intra-band transitions. Ref. [21] proposed intra-band hole transition near $k = 0$ to explain low energy spectra, but can not fit the emitting wavelength longer than 620 nm. It is concluded that:

1.   Photons with emitting wavelength longer than 620 nm are attributed to indirect inter-band process in high-field carrier populations.

2.   Bremsstrahlung radiation appears to dominate at intermediate range of 539 to 620 nm.

3.   The mechanism can be treated as near-direct inter-band transition for emitting wavelength shorter than 539 nm.

Fig. 3 also presents that very week electroluminescence almost hidden on noise especially for wavelength 539 nm is noise very strong. The result is attributed to the total internal reflections, scattering, and electromagnetic absorption from the via plugs and metal interconnects. In addition, the spectral characteristics of the electro-absorption peaks associated with phonon-assisted processes are strongly affected by the magnitude of the applied electric field over the range of 10^4 to 10^6 V/cm for avalanche breakdown, but the electro-absorption spectrum is unchanged in relative magnitude and peak position by a change in temperature, and the absolute

spectra positions follow the bandgap dependence on temperature [22].

4. Opto-coupler application silicon electro-optic modulation in ADC role

Photonics has many attributes that can optimize the performance of high speed ADCs. Fig. 4 shows the schematic of such a photonic-assisted ADC conversion system. After photo-detection, the received signal due to the modulated pulse train is fed, in turn, to an electronic quantizer for digitization. Through the way of incorporating photonics into the ADC, a remote ultra-stable microwave oscillator can drive the mode-locked laser and clock several electronic ADC quantizer via RF-photonic links.

Here, it is summarized that the multi-GHz sampling rates offered by a stable pico-second pulse train will enable the direct sampling of high frequency analog input-signals, especially reducing the number of mixer-stages that are needed to down-convert high frequency signals before digitization [23]. The photonic ADC presented above was made with discrete components in a laboratory setting, similarly to most other photonic ADCs demonstrated to date. However, to be a viable alternative to electronic ADCs, a photonic ADC must be integrated on a chip. Integration enables robustness, miniaturization, potential low-cost mass production, and promises to improve power efficiency and signal integrity by eliminating interconnects between separate chips. A major benefit of the approach pursued in this work is that it allows integration, and a full photonic ADC can potentially be implemented on a single chip using silicon photonics technology, as envisaged below.
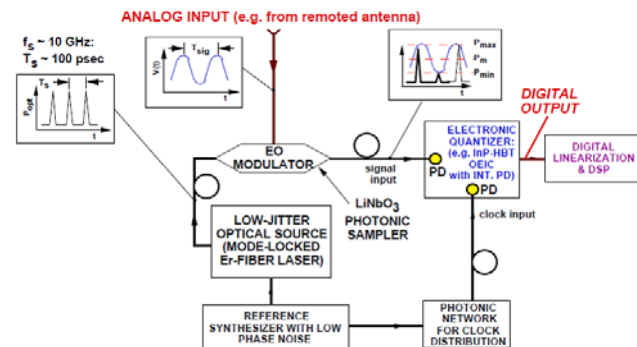

Fig. 4. Schematic of photonic analog-to-digital converter.

Since Si is the material of choice in contemporary microelectronics, using the silicon CMOS process as the platform to fabricate a broadband electro-optic modulation device is highly expected. It is noted that the p-n junctions will be more sensitive when operate in forward-bias, but have greater bandwidth under reverse-bias. The study concentrates on the case of reverse-bias, since the ADC requires a much better bandwidth [24], in particular visible light is emitted due to avalanche breakdown process

occurring in the reverse-biased silicon p-n junctions. For instance, light modulation as high as 20 GHz was observed in avalanche breakdown mode, and this speed is much higher than that of forward-biased silicon p-n junctions [25].

Since the intrinsic modulation speed of a silicon modulator based on the free carrier dispersion effect is determined by how fast the free carriers are injected, different modulator device configurations are with different dynamics mechanisms. A silicon device with the MOS-like structure can realize light intensity modulation by the insulated-gate terminal. As shown in Fig. 5, the device operating with p^+n junction biased to a fixed value and with varying gate voltage V_g is defined as Si gate-controlled diode LED.

From Fig. 5(a), it is also obtained that the electric ac input goes into the gate-source/drain port and the optical ac output is extracted at the drain-source port. The DC response of the modulator is tested by varying the DC bias voltage (i.e., the gate voltage V_g) while the p-n junction reverse-bias remains at the same value. Fig. 5(b) shows the measured normalized light intensity as a function of the applied voltage. The linearity of the modulation curve shown in Fig. 5(b) provides the evidence of low distortion.
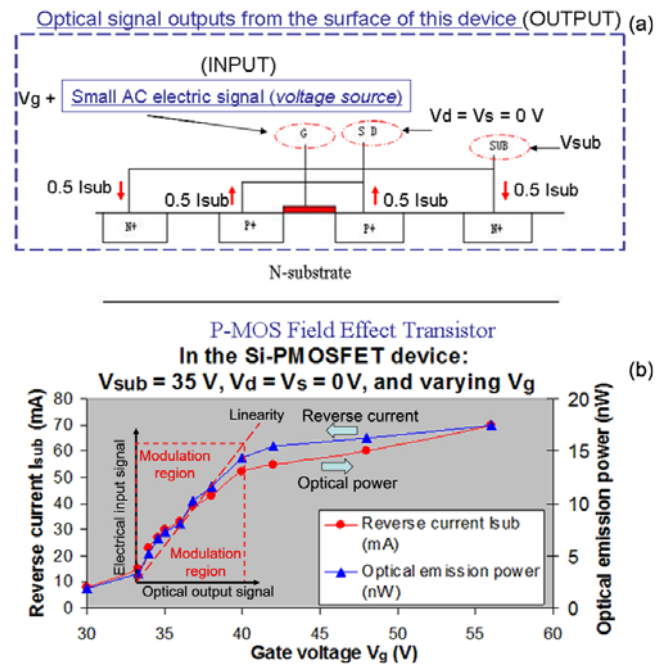

Fig. 5. Characteristics of Si MOS-like LED: (a) V_g , a DC source, is the gate voltage. V_{sub} , a dc source, is the reverse bias across the "p^+ S/D to n-sub" junction. (b) V_g is varied to realize optical modulation in the three-terminal device. The transfer function between the electric input and the optical output is determined by the slope of the modulation curve.

The main features of switching transitions of Si gate-controlled diode LED is characterized, and a model is developed to explain the modulation speed. To model the

modulation speed, numerical simulation are performed by solving Poisson and carrier continuity equations. A small-signal equivalent circuit model is applied for the analysis of expected modulation speed as a result of parasitic capacitances [26]. The upper limit derived value for the expected maximum modulation of the device could be in the range of a few hundred GHz [27]. The Si gate-controlled diode LED could be a potential replacement of conventional Electro-Optic (EO) modulator shown in Fig. 4. The high-speed silicon electro-optic modulator that can transfer the electric signal into the optical domain is an important component of the sampling system.

In Fig. 5, an etched crevice of 0.4 μm in the first TEOS layer is filled up with silicon nitride as both SiN_x offers high refractive index of 2.2-2.4 against a background of available SiO_2 as cladding or background refractive index layers in CMOS silicon, followed by further chemical vapor deposition (CVD) deposited tetraethyl orthosilicate (TEOS) oxide over-layer [28]. Hence, a high refractive index core of n = 2.4 are formed with a surrounding index of n = 1.46 at 750 to 850 nm. The RF coupling between the source shown in Fig. 5 and the detector in the on-chip optical micro-links could be analyzed with an Agilent 40 GHz vector network analyzer (VNA) series 8510 (50 MHz~40 GHz). Fig. 6 shows the final coupling results for an optical link fabricated with well aligned Si-Ge Avalanche LEDs as light emitting source, and optical waveguide of the type in Fig. 5 and standard Si-Ge detector as realized by Rosales *et al.* [29]. On the detector side, a Si-Ge Heterojunction Bipolar Transistor (HBT) is selected with a width of 5μm and a length of 1.2 μm. The analyses show clearly higher forward S_{21} than reverse S_{12} for most of the frequency range as investigated in Fig. 7. This clearly indicates that some optical propagation occurs along the waveguide that is well decoupled from the parasitic substrate and oxide coupling effects. Further experiments are under way to validate this potential as well as for Si-Ge forward bias configurations [30].

Fig. 6. Schematic presentations showing the basic design of the waveguides of the optical links, using silicon avalanche - based LED, silicon - based waveguide and Si-Ge based detectors.

In order to overcome the disadvantage of transmission loss occurred by the waveguide, the increased efficiency of Si LED in standard silicon complementary metal oxide semiconductor technology is further analyzed by

investigating the physical mechanisms incurring the photon generation by silicon junction under reverse bias [31]. Both the external quantum conversion efficiency and the internal conversion efficiency could be improved by means of further innovative design and processing procedures without deviating too far from the existing technological routes, such as the carrier energy and momentum engineering design [32] and the MOS-structure based high-field emission design [33].
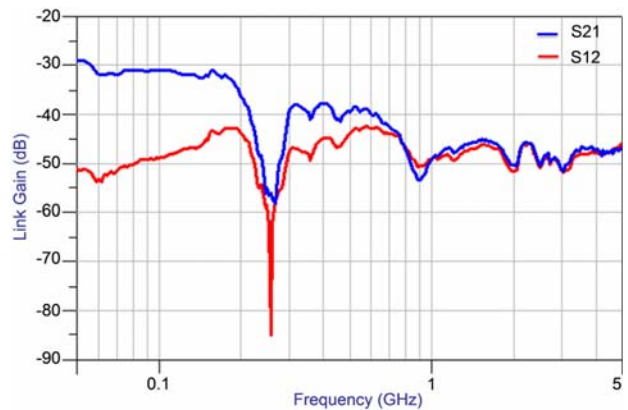

Fig. 7. RF coupling results for the realized on-chip micro-optical links.

5. Conclusions

A Si-LED with the MOS-like structure that is fully compatible with standard CMOS process technology is studied. The Si-LED could emit optical radiation in a broad band in the 400 to 900 nm range. Coupling between the elements as well as electro-optical coupling between an element and an optical fiber is also successfully presented. The study of the Si-LED potentially enables diverse on-chip electro-optical coupling and interfacing applications. The topic of high speed analog-to-digital conversion with silicon photonics is also discussed.

Academy of Sciences (IOS, CAS) for the unforgettable encouragement and support.

References

[1] Z. Zhang, B. Huang, Z. Zhang, C. Cheng, H. Liu, H. Li, H. Chen, Opt. Commun. **367**, 206 (2016).

[2] M. Deen, P. Basu, Silicon Photonics: Fundamentals and Devices, First Edition, John Wiley & Sons, Ltd., (2012).

[3] I. Young, K. Bergman, A. Krishnamoorthy, V. Stojanovic, IEEE J. of Select. Topics Quantum Electron. **19**(2), 0200302 (2014).

[4] R. Newman, Phy. Rev. **100**(2), 700 (1955).

[5] L. Snyman, H. Aharoni, M. du Plessis, A. Biber, J. Marais, D. Niekerk, Opt. Eng. **41**(12), 3230 (2002).

[6] Y. Taur, T. Ning, Fundamentals of Modern VLSI Devices, 2nd ed, Cambridge University Press, New York, 2009, pp. 135.

[7] K. Xu, N. Ning, K. Ogudo, J. Polleux, Q. Yu, L. Snyman, J. Polleux, Proc SPIE **9667**, 966702-1-10, (2015).

[8] J. Colinge, C. Colinge, Physics of Semiconductor Devices, Kluwer Academic Publishers, Norwell, MA, 2002, pp. 171

[9] K. Xu, G. Li, J. Appl. Phys. **113**(10), 103106 (2013).

[10] M. du Plessis, H. Aharoni, L. Snyman, Sens. Actuator A. Phys. **80**(3), 242 (2000).

[11] M. du Plessis, H. Aharoni, L. Snyman, Physica Status Solidi A **201**(10), 2225 (2004).

[12] K. Xu, H. Liu, Q. Yu, Z. Wen, G. Li, J. Optoelectron. Adv. M. **17**(11-12), 1680 (2015).

[13] M. Kastner, Phys. Today **46**(1), 24 (1993).

[14] L. Pavesi, Advances in Optical Technologies **2008**, 1 (2008).

[15] N. Akil, S. Kerns, D. Kerns Jr., A. Hoffmann, J. Charles, Appl. Phys. Lett. **73**(7), 2 (1998).

[16] A. Lacaita, F. Zappa, S. Bigliasrdi, M. Manfredi, IEEE Trans. Electron Devices **40**(2), 577 (1993).

[17] K. Cho, Opt. Commun. **8**(4), 412 (1973).

[18] D. Gautam, W. Khokle, Solid State Electron. **31**(6), 1119 (1988).

[19] T. Figielsky, A. Torun, Prof. Int. Conf. Phys. Semiconductors (Exeter, UK), p. 853, (1962).

[20] A. Chynoweth and K. McKay, Phys. Rev. **102**(2), 369 (1956).

[21] P. Wolff, J. Phys. Chem. Solids. **16**, 184 (1960).

[22] P. Wendland, M. Chester, Phys. Rev. **140**(4A), A 1384 (1965).

[23] K. Xu, S. Wu, Z. Zhang, Q. Yu, X. Huang, Y. Wang, J. Polleux, 20th OptoElectronics and Communications Conference, 2015, pp. 1-3,

[24] T. Dittrich, V. Timoshenko, J. Rappich, L. Tsybeskov, J. Appl. Phys. **90**(5), 2310 (2001).

[25] A. Chatterjee, B. Bhuva, R. Schrimpf, IEEE Electron Device Lett. **25**(9), 628 (2004).

[26] K. Xu, S. Liu, J. Zhao, W. Sun, G. Li, Opt. Eng. **54**(5), 057104 (2015).

[27] K. Xu, H. Liu, Z. Zhang, Appl. Opt. **54**(21), 6420 (2015).

[28] L. Snyman, J. Polleux, K. Ogudo, C. Viana, S. Wahl, Proc. SPIE, **8990**, 89900L-1–12, (2014).

[29] M. Rosales, J. Polleux, C. Algani, 8th IEEE International Conference on Group IV Photonics, pp. 14 (2011).

[30] K. Ogudo, L. Snyman, J. Polleux, C. Viana, Z. Tegegne, D. Schmieder, Proc. SPIE, **8991**, 899108-1–16 (2014).

[31] K. Xu, Z. Zhang, Z. Zhang, J. Nanophoton. **10**(1), 016002 (2016).

[32] K. Xu, K. Ogudo, J. Polleux, Z. Ma. Z. Li, Q. Yu, G. Li, L. Snyman, LEUKOS, the journal of the Illuminating Engineering Society, **12**(4), 203 (2016).

[33] K. Xu, S. Liu, W. Sun, Z. Ma, Z. Li, Q. Yu, G. Li, IEEE J. Select. Topics Quantum Electron. **22**(6), 2000508 (2016).

[*]Corresponding author: kaikaix@uestc.edu.cn