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Temperature dependence of electrical characteristics of Cu/n-Si Shottky barrier diodes formed by electrodeposition

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Electroplating technique is especially interesting due to its low cost and high quality of deposits being extensively used in industry. In this work, Cu film is electrodeposited on n-type Si (100) substrate using constant current mode. The electrical properties of Cu/n-Si were investigated at several temperatures. The current-voltage analysis based on the thermionic emission theory has revealed an abnormal decrease of apparent barrier height and increase of ideality factor at low temperatures.

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Keywords: Electrodeposition, Schottky barrier, Temperature dependence

1. Introduction

Interfaces between thin metal layers and semiconductors are used in optical detectors, solar cells [1] and chemical sensors [2-3]. The transport properties of such Schottky diodes and the dependence of the transport parameters on preparation are of essential importance for the device performance. Metal-semiconductor interfaces may be characterized by photoelectrical and current-voltage (*I-V*) measurements [4-5].

The metallization of semiconductor surfaces is still mostly performed in vacuum by evaporation or sputtering. The process itself is of great technological importance of Schottky barriers and ohmic contacts in electronic devices. As an alternative to the deposition from the vapor phase, many metals can be electrodeposited onto semiconductors from solution. By varying the overpotential or the composition of the electrolyte, it is possible to influence the growth mode and the structure of the deposit. Therefore it is necessary to understand in detail the mechanisms of nucleation and growth as well as the structural properties of electrodeposits.

Because of a replacement of aluminum by copper in the silicon metallization process [6], the electrochemical deposition of metals, particularly of copper, on silicon has received increased interest in recent years. Despite its great industrial importance, relatively little work is reported in the literature on the fundamental aspects of electroplating on semiconductor substrates [7-8]. So far, most of the work about metal deposition onto semiconductors was performed with classical electrochemical methods.

Previously we reported on $C-V$ measurement results and of the profile representing the impurity distribution in the of a Cu/Si MS junction formed by electrodeposition [9]. In the present paper we report of an experimental study of the $I-V$ of a Cu/Si MS junction formed by electrodeposition of copper on n- Si (100) from a copper sulphate bath.

2. Experimental

One-sided polished n-Si (100) samples, phosphorus-doped, 1-20 Ωcm (N_D =10^{15}cm^{-3}) were used as substrate. They were cleaned following cleaning procedure [10], which means degreasing in 2-propanol under reflux for 2 h and then boiling alternating for 15 min in basic and acidic H_2O_2 solutions. Prior to each experiment the substrates were etched for 1 min in 20% HF (Merck, VLSI Selectipur) to remove the oxide layer. Ohmic contacts were formed by vacuum evaporation of an Au layer on the back of the wafers after the etching procedure.

Copper was deposited from an electrolyte containing 0.2 M $CuSO_4{\cdot}5H_2O$ + 0.5 M H_3BO_3 (pH=2.0). The electrochemical experiments were carried out in a conventional three-electrode cell connected to a potentiostat. A saturated calomel electrode (SCE) and a platinum sheet served as reference and counter electrode, respectively. All potentials are reported versus SCE. The current-voltage (*I-V*) measurements were performed using a Keithley 2400 voltage source were carried out at several temperatures. All measurements were controlled by a computer via an IEEE – 488 standard interface so that the data collecting, processing and plotting could be accomplished automatically.

3. Result and discussion

The electrical characterizations of the device were achieved through I-V measurements at several temperatures. The formation of a Schottky barrier between a Cu layer and n-doped Si (100) at room temperature is shown in Fig. 1.

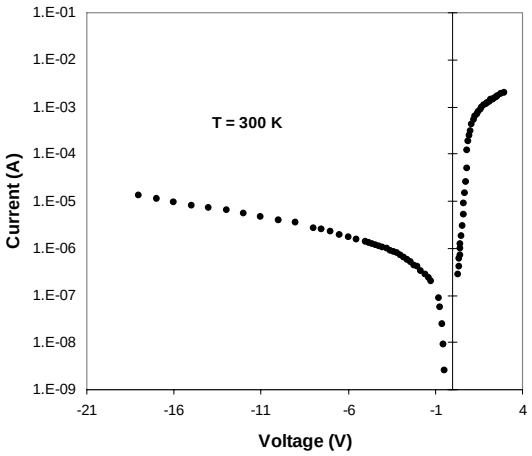

Fig. 1. The experimental forward and reverse bias current versus voltage characteristics in a semilog scale of Cu/ n-Si Schottky barrier diodes at room temperature.

The reverse and forward currents of diodes demonstrate that the rectifying properties and the rectification coefficient was 108.7. The current through a Schottky barrier diode at a forward bias *V*, based on the thermionic emission theory, is given by the relation [11],

$$J = J_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \quad (1)$$

where J_0 is the saturation current density is given by

$$J_0 = A^* T^2 \exp\left(-\frac{q\phi_{b0}}{kT}\right) \quad (2)$$

where q is the electron charge, V is the forward bias voltage, k is the Boltzmann constant, T is the absolute temperature, A is the effective diode area, $A^* = 4\pi q m^* k^2 / h^3$ is the effective Richardson constant of 110 A/cm^{2}K^2 for n-type Si, ϕ_{b0} is the zero bias apparent barrier height (BH) and n is the ideality factor. The saturation current density J_0 was derived by extrapolation of the linear forward part to the axis and it was found to be 5.42×10^{-4} A cm^{-2}, in agreement with the reverse bias current. The ideality factor is calculated from slope of the linear region of the forward bias $\ln J$ -V plot and can be written from Eq.(1) as:

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln J)}\right) \quad (3)$$

The zero-bias barrier height ϕ_{b0} is given by:

$$\phi_{b0} = \frac{kT}{q}\ln\left(\frac{A^* T^2}{J_0}\right) \quad (4)$$

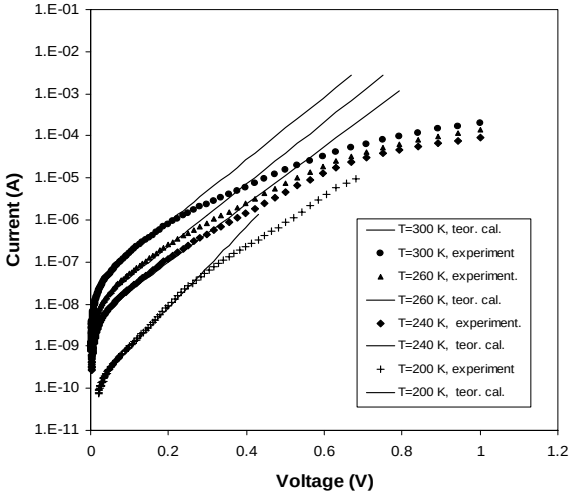

Fig. 2. The semilog forward bias current-voltage ($I-V$) characteristics of Cu/n-Si Schottky barrier diodes at several temperatures.

The comparison was theoretically calculated (eq. 1) and experimental current-voltage characteristics in the forward bias region for several temperatures are shown in Fig. 2. The experimental values of ϕ_{b0} and n, were determined from intercepts and slopes of the forward-bias $\ln J$ versus V plot at each temperature (Fig. 2) respectively. The experimental values of ϕ_{b0} and n for the device range from 0.785 eV and 2.82 (at 300 K) to 0,587 eV and 3.74 (at 200 K), respectively. The values of n and ϕ_{b0} obtained depending on the temperature are given in Fig.3. The experimental value of n increased with a decrease in temperature and the experimental value of ϕ_{b0} decreased with a decrease in temperature as can seen in Fig. 3.

Since current transport across the MS interface is a temperature activated process, electrons at low temperatures are able to surmount the lower barriers and therefore current transport will be dominated by current flowing through patches of the lower Schottky barrier height (SBH) and a larger ideality factor. As the temperature increases, more and more electrons have sufficient energy to surmount the higher barrier. As a result, the dominant barrier height will increase with the temperature and bias voltage.

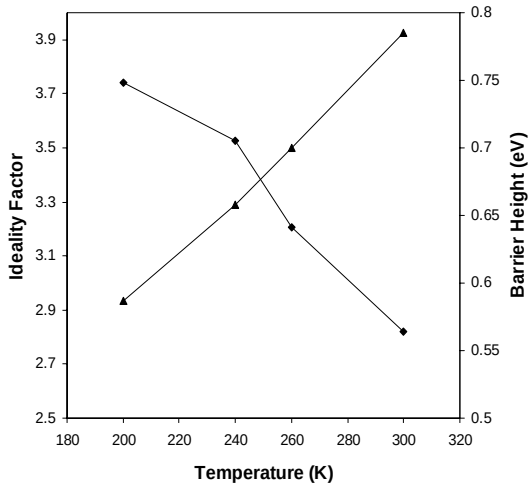

Fig. 3. Temperature dependence of the ideality factor and the zero-bias apparent barrier height for Cu/n-Si Schottky barrier diodes.

According to [12], the ideality factor of an inhomogeneous Schottky barrier diode (SBD) with a distribution of low SBHs may increase with a decrease in temperature. The Schottky barrier consists of laterally inhomogeneous patches of different barrier heights. Schmisdrof et al. [13] used Tung's theoretical approach and they found a linear correlation between the experimental zero bias SBHs and the ideality factors. We prepared a plot of the experimental barrier height versus the ideality factor (Fig. 4). As can be seen from Fig. 4, there is linear relationship between the experimental effective barrier heights and the ideality factors of the Schottky contact that was explained by lateral inhomogeneities of the barrier heights in Schottky diodes [14].

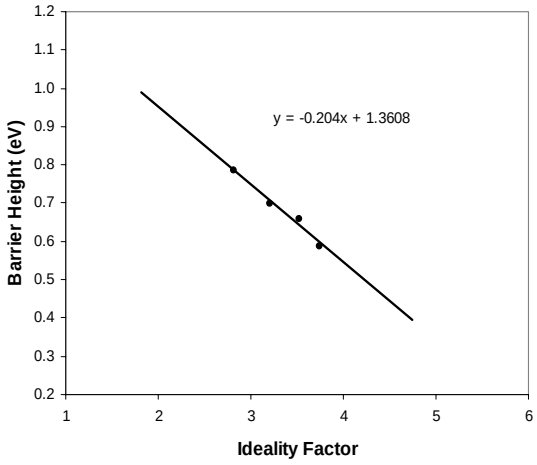

Fig. 4. Zero-bias apparent barrier height versus the ideality factor of a typical Cu/n-Si Schottky barrier diodes.

At high currents, there is forever a deviation which has been clearly shown to depend on the interface states density and series resistance, associated with bulk material Si and the ohmic back contact, when the applied voltage is sufficiently large. The ideality factor and the series resistance were evaluated using a method developed by Cheung et al. [15]. The Cheung's method is achived by using the functions;

$$\frac{dV}{d(\ln I)} = n\frac{kT}{q} + R_S I \tag{5}$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{6}$$

and

$$H(I) = IR_S + n\phi_{b0} \tag{7}$$

where ϕ_{b0} is the real barrier height extracted from the lower-voltage part of forward $I-V$ characteristics. The $dV/d(\ln(I))$ plot is a straight line region where dominates the series resistance. In the plot of $dV/d(\ln(I))$ versus I, its slope gives the series resistance while its intercept with the y - axis gives the ideality factor. The ideality factor, n, is extracted from $dV/d(\ln(I))$ plot within voltage range where influence of series resistance is significant. Using so obtained value of ideality factor, n, the Schottky barrier height is estimated from plot of a function $H(I)$ given in Eq. 6.

As can be seen from Fig. 5, there is approximately the straight line which intercepts y - axis at the point equal to $n\phi_{b0}$.

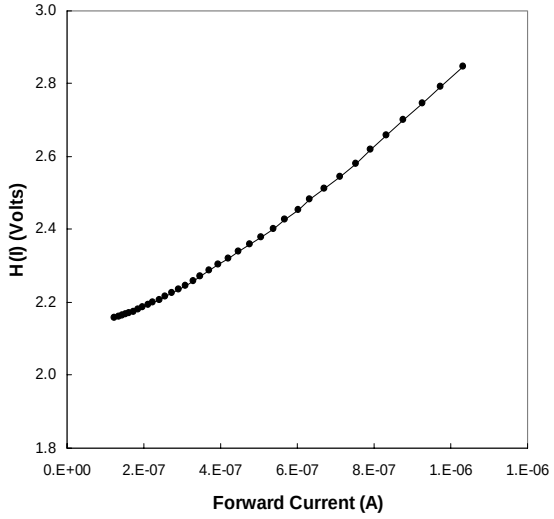

Fig. 5. Experimental $H(I)$ vs. I curve of Cu/n-Si Schottky barrier diodes at room temperature.

4. Conclusions

In this work we investigated the main electrical properties of the Schottky diodes formed by electrodeposition of copper on n- Si (100) from 0.2 M $CuSO_4 5H_2O$ + 0.5 M H_3BO_3 (pH=2.0) solution, through the barrier heights, the ideality factors by using current-voltage ($I-V$) characteristics. Electrical measurements have been carried out at several temperatures. The non-ideal forward bias ($I-V$) behavior observed in the Cu/ n-Si Schottky barrier diodes were attributed to a change in the metal- semiconductor barrier height due to the interface states and the interfacial layer.

Acknowledgement

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