The effects of the interfacial layer with interface states on controlling the electronic properties of Au/n-GaAs Schottky diode

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The electrical characteristics and interface state density properties of Au/insulator/n-GaAs (MIS metal–insulator–semiconductor) diodes with insulator layers having different thickness have been analyzed by current–voltage and capacitance–voltage techniques at room temperature. The barrier height and ideality factor values for MIS Schottky diodes were found to be 0.66 eV, 1.67 and 0.86 eV, 3.75, respectively. The diodes show a non-ideal I–V behavior with the ideality factor greater than unity. This behavior is attributed to the interfacial insulator layer and the interface states. The obtained results show that the insulator layer modifies the electrical parameters such as interface state density, series resistance and reduces the reverse bias leakage current by more than two orders of magnitude. In addition, the interface distribution profiles (D_{it}) were extracted from the *I-V* measurements by taking into account the bias dependence of the effective barrier height for the Schottky diode. The energy distribution curves of the interface states of each sample were determined. The interface state density N_{ss} of the diodes was changed from 4.7×10^{12} eV^{-1} cm^{-2} in (E_c-0.647) eV to 6.35×10^{14} eV^{-1} cm^{-2} in (E_c-0.619) eV for the initial sample AuD1 MIS diode and from 2.67×10^{15} eV^{-1} cm^{-2} in (E_c-0.850) eV to 1.01×10^{15} $eV^{-1}.cm^{-2}$ in (E_c-0.756) eV for AuD2 MIS diode.

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1. Introduction

For many years, metal-Semiconductor (MS) structures have been extensively studied because of their technological importance in the electronics industry. It is well known that many Schottky barrier diodes show deviation from the ideal current-voltage (*I-V*) characteristics predicted by the thermionic-emission theory [1-2]. The values of diode parameters are influenced by the interface states, series resistance and interfacial layer and etc.,[1,3-4]. The performance and reliability of a Metal-Insulator-Semiconductor (MIS) contact are highly influenced by the interface quality between the deposited metal and semiconductor surface. In order to understand the conduction mechanism of the MIS diodes (SBDs), many attempts have been made. The first studies on the interfacial insulator layer, between metal and semiconductor in Schottky diodes were made by Cowley and Sze [4] who obtained their estimations from an analysis of the Schottky barrier heights with different metallization as a function of metal work function. Card and Rhoderick [5] estimated the interface state density located at the insulator (SiO_2)/semiconductor (Si) interface and examined effects of the interface states on the ideality factor of the forward bias I–V characteristics. There are many effects which cause deviation of the ideal behaviour for electrical characteristics. These include the effects of insulator layer between metal and semiconductor; interface state (D_{it}), series resistance (R_s) and formation of barrier height [6-10]. The analysis of the current-voltage (*I-V*) characteristics of Schottky barriers on the basis of thermionic emission diffusion (TED) theory reveals non-ideal behaviour [11-13]. Explanation of the possible origin of such anomalies have been proposed by taking into account the interface state density distribution [14], quantum-mechanical tunnelling [15,16,17], image-force lowering [15] and most recently the lateral distribution of Barrier Height (BH) inhomogeneities [11,18,19]. In addition, a Gaussian distribution of the BH over the contact area has been assumed to describe the inhomogeneities as an other way too [11,20]. Owing to recent developments on GaAs devices, much information is available about metal contacts on Gallium Arsenide. The stability and reproducibility of contact properties and the formation of a high-quality Schottky barrier height (SBH) are essential prerequisites for device development [21–25].

In present work, the electrical properties of Au/n-GaAs Schottky diodes with different interfacial layer thickness have been investigated using current-voltage (I-V) and capacitance-voltage (C-V) characteristics. Finally,

it has been concluded that the different insulator layer thickness varies the diode parameters by influencing the space charge region of the Au/n-GaAs Schottky junction.

2. Experimental details

Schottky barrier diodes were fabricated on n-type GaAs (Si-doped) substrate with (100) orientation and a doping concentration of 2.6x10^{16} cm^{-3}. The substrate was sequentially cleaned with chloroform, acetone, methanol and then rinsed in deionised water. The native oxide on the surface was etched in sequence with acid solutions $(H_2SO_4 : H_2O_2 : H_2O = 3:1:1)$ for 60 seconds, and $(HCl : H_2O = 1:1)$ for another 60 seconds. Following a rinse in de-ionized water of 18 MΩ, the wafer was dried with high-purity nitrogen and inserted into the deposition chamber immediately after the etching process. Low resistance ohmic contact on the back side of the sample was formed by evaporating of indium at a pressure of $2x10^{-5}$ torr, followed by annealing at 375 ^0C for 5 minutes in nitrogen atmosphere. Then, the above procedures were also used to clean the front surface. After dividing to two pieces of the sample having ohmic contacts, to form the insulator layer on the clean front surface of one of the substrates, it is exposed to clean room air for about one day (sample AuD1). For the second piece (sample AuD2), e*x situ* annealing has been carried out at the 400 ^oC for 5 minutes in oxygen flow. The thickness of the insulator layer so obtained was in the range of $\approx$50-100 ^{0}A across the full substrate surface (polished surface not having ohmic contact,), and was uniform. To form the Schottky barriers, finally, circular dots with a diameter of approximately 2.0 mm of Au were deposited on the surfaces with different insulator layer thickness substrates by vacuum evaporation technique through a molybdenum mask at $\approx 2.0x10^{-5}$ torr pressure Thus, the samples with different insulator layer thickness were obtained. Current-voltage and capacitance-voltage measurements of the devices were made using a computer controlled Keithley 6517A electrometer and a 4200 SCS semiconductor characterization system, respectively, at room temperature.

3. Results and discussion

3.1 Current-voltage characteristics

Fig.1 shows forward-reverse current-voltage characteristics of the Au/n-GaAs MIS Schottky diodes at room temperature. As seen in Fig.1, the diodes show a good rectifying behavior. The current–voltage characteristics of a metal–insulator–semiconductor (MIS) diode can be analyzed by the following relation [1, 3]

$$I = I_0 \exp\left(\frac{q(V - IR_s)}{nkT}\right)\left[1 - \exp\left(-\frac{q(V - IR_s)}{kT}\right)\right] \quad (1)$$

Where q is the electronic charge, V is the voltage, Rs is the series resistance, n is the iedality factor and I_o is the saturation current is given by

$$I_0 = AA^*T^2 \exp(-\alpha\chi^{1/2}\delta)\exp\left(-\frac{q\Phi_b}{kT}\right) \quad (2)$$

where A^* is the effective Richardson constant and 8.16 AK^{-2}cm^{-2}, k is the Boltzmann constant, T is the absolute temperature, Φ_b is the zero-bias current-barrier height (apparent barrier height), n is the ideality factor, exp($-\alpha\chi^{1/2}\delta$) is transmission coefficient across the thin interfacial layer, $\alpha = (4\pi / h)(2m^*)^{1/2}$ is a constant, *h* is a planck constant, m* is the effective mass of the electrons (0.067m$_0$) [26-29], δ is the thickness of the interfacial layer, χ is the effective tunnelling barrier of the interfacial layer and calculated as 0.450 eV. $\alpha\chi^{1/2}\delta$ is the hole tunnelling factor and obtained as 6.95. Eq. (2) is valid only for forward biases V >3kT/q, since the reverse current contribution (due to holes tunnelling from the metal into the semiconductor) has been neglected. δ the thickness of the interfacial layer, in which holes move through tunnel was calculated as 130 ^{0}A.

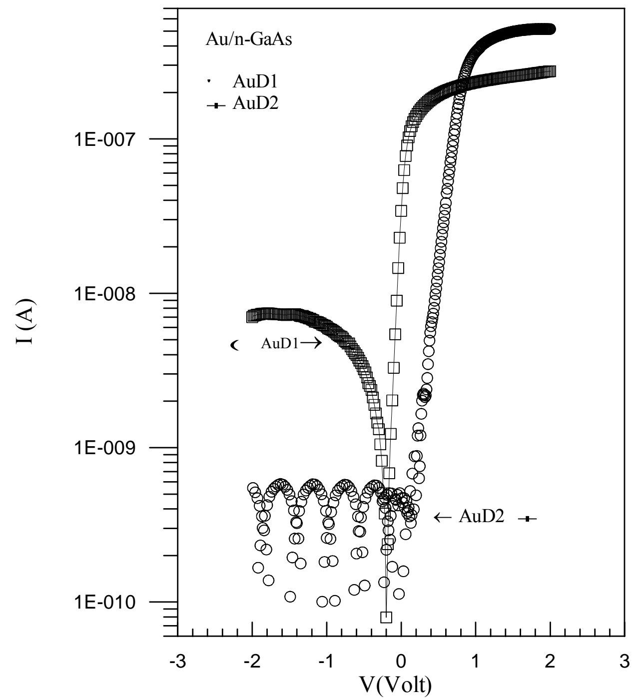

Fig. 1. Semi-logarithmic reverse and forward bias current-voltage characteristics of AuD1 and AuD2 MIS Schottky diodes, at room temperature.

From Eq. (1), the ideality factor n can be written as

$$n = \frac{q}{kT}\left(\frac{dV}{dIn(I)}\right) \tag{3}$$

The extrapolation of *I-V* curves to zero-bias yields the value of saturation current as $3.55\text{x}10^{-8}$ and $8.35\text{x}10^{-11}$ A for AuD1 and AuD2 MIS devices, respectively. Thus, the presence of an intentionally grown insulator layer reduces the value of the saturation current by three orders of magnitude, indicating an increasing in the BH. The values of Φ_b and n were determined from the intercept and the slopes of the forward bias $In(I)$ versus voltage (*V*) plot according to *TE* theory, respectively. The Φ_b and the *n* values for the initial and second sample MIS Schottky diodes were obtained from the forward-bias *I-V* characteristics at room temperature as 0.66 eV; 1.67 and 0.86 eV; 3.75, respectively. The obtained barrier height for the Au/n-GaAs/In Schottky diode is in agrement with the previously published results [30-32]. The increase in barrier height is ascribed to negative charges at the interface. These negative charges probably arise due to electron traps localized at the GaAs surface and associated with vacancies created near the surface during the growth of the interfacial insulator layer. The obtained ideality factors (1.67, 3.75) show that Au/n-GaAs structure has a metal-insulator-semiconductor structure. The I-V characteristics deviate from linearity due to the series resistance and interfacial layer. Thus, the series resistance is effective parameter in I-V characteristics of the diode and it can not be ignored. Therefore, we used Norde method [33] to calculate Φ_b, n and series resistance values of the diodes. In Norde method, the following function is used as,

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\left(\frac{I(V)}{A^* A T^2}\right) \tag{4}$$

where γ is the integer (dimensionless) greater than n. I(V) is the current obtained from the I–V characteristic. The plots of F(V) vs voltage for the diodes are shown in Fig.2. The F(V) gives a minimum point and thus, the barrier height is calculated by the relation,

$$\Phi_b = F(V_0) + \frac{V}{\gamma} - \frac{kT}{q} \tag{5}$$

where $F(V_o)$ is the minimum point of F(V) function. The barrier height values for AuD1 and AuD2 MIS Schottky diodes have been obtained from the F(V)–V characteristics at room temperature as 0.67 and 0.81 eV, respectively. There is a agreement with the values of barrier height obtained from the forward bias ln*I-V* function. The series resistance is determined as

$$R_s = \frac{kT(\delta - n)}{qI_o} \tag{6}$$

The R_s value determined using Eq. 6 for AuD1 and AuD2 MIS Schottky diodes were found to be 178 kΩ and 2.7 MΩ. This shows that insulator layer affects a non-linear region of forward bias *I–V* curve of the diode and increases resistance of the Au/n-GaAs structure.

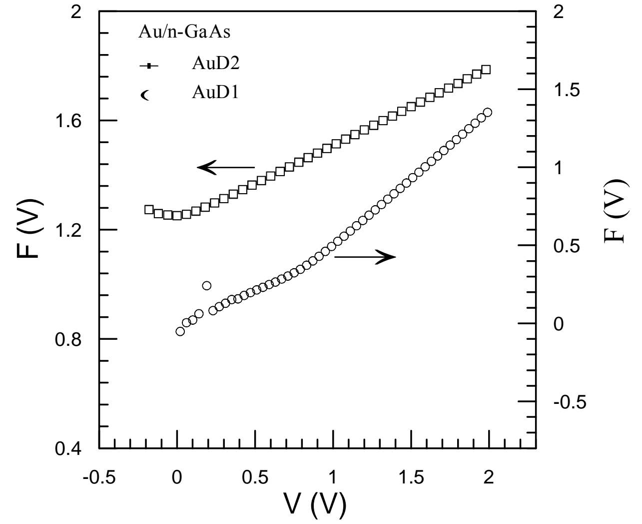

Fig. 2. Plot of F(V) vs voltage of AuD1 and AuD2 MIS Schottky barrier diodes

3.2 Capacitance-voltage characteristics and interface state density properties of the Au/n-GaAs Schottky diode

If the time constant is too long to permit the charge to move in and out of the states in response to an applied signal, the charge at the interface states cannot follow the alternating current (a.c.) signal. This will occur in C-V measurements carried out at sufficiently high frequencies. At low frequencies, the interface states respond to the alternating signal [3,34,35]. Thus, in MIS Schottky diodes, the depletion layer capacitance can be expressed as [36]

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_r - kT/q)}{q\varepsilon_s \varepsilon_o A^2 N_d} \tag{7}$$

where, V_{bi} is the built-in voltage determined from the extrapolation of the $C^{-2} - V$ plot to the voltage axis, V_r is the reverse voltage, *A* is the area of the diode, ε_s is the static dielectric constant equal to 13.1 for n-GaAs [21-23], $\varepsilon_o = 8.85\text{x}10^{-14}$ F/cm and N_d is the donor concentration. The N_d is related to the slope of C^{-2} vs. *V* curve and can be obtained from the expression given below

$$N_d = \frac{2}{q\varepsilon_s \varepsilon_o A^2}\left[\frac{1}{d(C^{-2})/dV}\right] \tag{8}$$

The BH deduced from capacitance is obtained from

$$\Phi_b^{C-V} = V_{bi} C_2 + \frac{kT}{q} \ln\frac{N_c}{N_d} \tag{9}$$

where C_2 is a constant and N_c (=4.3x10^{17} cm^{-3}) is the effective density of states in the conduction band for n-GaAs at 300 K [21-23]. Figs. 3-4 show the reverse bias $C^{-2}-V$ plots for AuD1 and AuD2 MIS Schottky diodes at room temperature in the range of -1.5 to +4.0 Volts. The reverse bias $C^{-2}-V$ plots show a non-linear curve. The non-linear behaviour of the curves can results from a non-uniform doping and interface states. The V_{bi} and N_d values are obtained from the intercepts and the slopes of the extrapolated C^{-2}-V lines with the V_r axis, respectively. Then, the values of Φ_b^{C-V} were calculated by using Eq. (9). The values for the BH deduced from the *C-V* data are also 1.06 and 1.18 eV for AuD1 and AuD2 MIS Schottky diodes, respectively. As can be seen, the barrier height value of the reverse bias C^{-2}-V plot for the AuD2 MIS diode is larger than that of the value obtained for the AuD1 MIS diode. Consequently, it is clear that the different barrier heights could be due to modified-interface chemistry [37]. Thus, it can be said that the pinning position of Fermi level may strongly depend on details of the surface preparation and conditions between the metal and semiconductor. On the other hand, the values of the BHs extracted from the C-V curves are higher than those derived from the I–V measurements as expected. This difference is explained due to an interface layer or trap states in the substrate, the effect of the image force and the barrier inhomogeneities. Furthermore, for the differences in barrier height values, some general reasons have been mentioned in the literature, such as surface contamination at the interface, deep impurity levels, an intervening insulating layer, quantum mechanical tunnelling, image-force lowering and edge leakage currents [1,4,14]. There have also been some reports showing that the discrepancy between BHs measured by different techniques might be associated with the instrumentation problems; namely, the way to determine true space-charge capacitance from *C–V* data or a large series resistance, which could affect the value determined from *I–V* data [14,38].

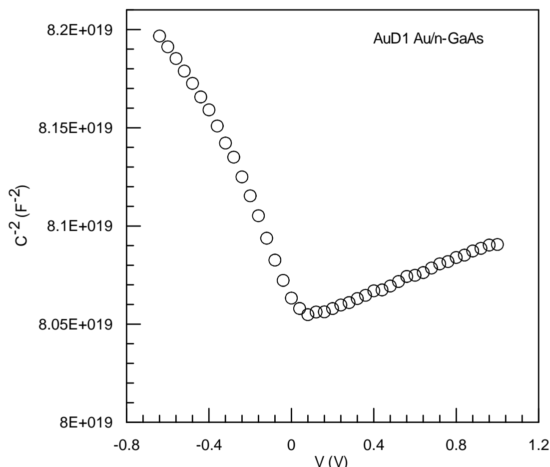

Fig. 3. The reverse bias C^{-2}-V characteristic of AuD1 Schottky barrier diode at room temperature.

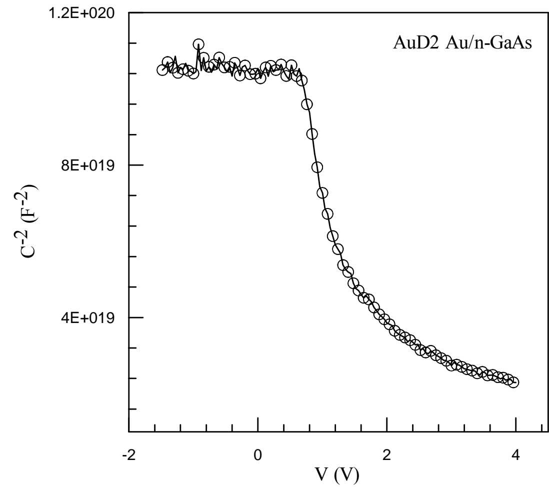

Fig. 4. The reverse bias C^{-2}-V characteristic of AuD2 MIS Schottky barrier diode at room temperature.

In the case of the interface layer, interface states and fixed surface charge affect the reverse bias and forward bias characteristics of Schottky devices, which causes a deviatation from ideal Schottky diode characteristics. Therefore, it can be said that the performance and reliability of Schottky devices depend on the interface layer and fixed surface charge. The interface states play an important role in the determination of metal/semiconductor structures. The density of the interface states can be calculated from the current-voltage measurements. For the MIS diode having interfaces N_{ss}, the ideality factor is higher than unity. Now, let us calculate the density distribution of the interface states from the *I-V* measurements of AuD1 and AuD2 MIS diodes. The barrier height of the SBDs is strongly dependent on the electric field in the depletion region, and thus also on the applied bias. The effective barrier Φ_e is assumed to be bias-dependent due to the presence of an interfacial layer and interface states located at the interfacial layer-semiconductor interface and defined as [5]

$$\Phi_e = \Phi_b + \left(\frac{d\Phi_e}{d\mathrm{V}}\right)\mathrm{V} = \Phi_b + \beta\mathrm{V} \tag{10}$$

where β is a constant. The Φ_e is a parameter that includes the effects of both interface states in equilibrium with the semiconductor [5]. For MIS Schottky diodes having interface states N_{ss} in equilibrium with semiconductor, the ideality factor n becomes greater than unity, as proposed by Card and Rhoderick [5], and is given by

$$\mathrm{n} = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}\right] \tag{11}$$

The N_{ss} is expressed by Card and Rhoderick [5] for MIS structure in equilibrium as;

$$N_{ss} = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_s}{W_D}\right] \quad (12)$$

Where δ is the thickness of interfacial insulator layer, W_D is the width of the space charge region, ε_i and ε_s are the permittivity of the interfacial insulator layer and the semiconductor, respectively. Furthermore, in n-type semiconductors, the energy of interface states E_{SS} with respect to the conduction band edge, E_c, at the semiconductor surface, is given by [39]

$$E_c - E_{ss} = q(\Phi_e - V). \quad (13)$$

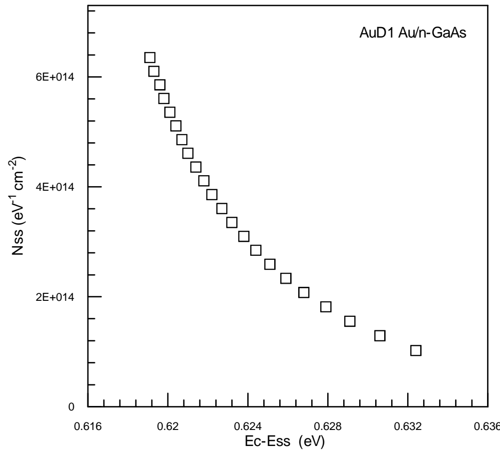

Fig. 5. The energy distribution curve of the interface states for AuD1 Schottky barrier diode

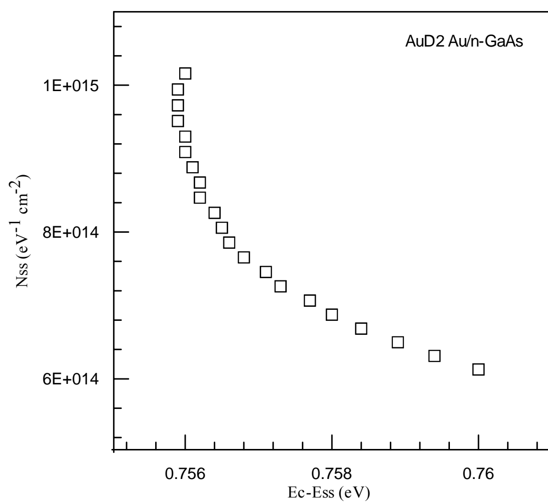

Fig. 6. The energy distribution curve of the interface states for AuD2 MIS Schottky barrier diode.

Thus, the energy distribution of the interface states in equilibrium with the semiconductor as a function of *V* may be determined by means of Eqs. (12) and (13) by taking into account the bias dependence of the ideality factor and BH. Figs. 5-6 show the curves of interface state density distribution determined from the downward concave curvature region of the experimental semilog forward bias current *I-V* characteristics of AuD1 and AuD2 MIS Schottky barrier diodes, respectively. As seen in Figs. 5-6, the exponential growth of the interface state densities from midgap towards the bottom of the conduction band is very apparent. The interface state densities N_{ss} of the diodes were changed from $4.7x10^{12}$ $eV^{-1}.cm^{-2}$ in (*E*c-0.647) eV to $6.35x10^{14}$ $eV^{-1}.cm^{-2}$ in (*E*c-0.619) eV for the AuD1 MIS and from $2.67x10^{15}$ $eV^{-1}.cm^{-2}$ in (*E*c-0.850) eV to $1.01x10^{15}$ $eV^{-1}.cm^{-2}$ in (*E*c-0.756) eV for the AuD2 MIS diode. The values of interface state density $(N_{ss})_{min}$ ($=1.99x10^{12}$ $eV^{-1}cm^{-2}$) are reasonable for metal/GaAs SBDs [40-41]. Experimental results show that, at any specific energy, the value of N_{ss} of AuD1 MIS SBD is less about one order compared to that of AuD2 MIS SBD. The interface states and interfacial layer between the metal/semiconductor structures play an important role in the determination of the characteristic parameters of the devices.

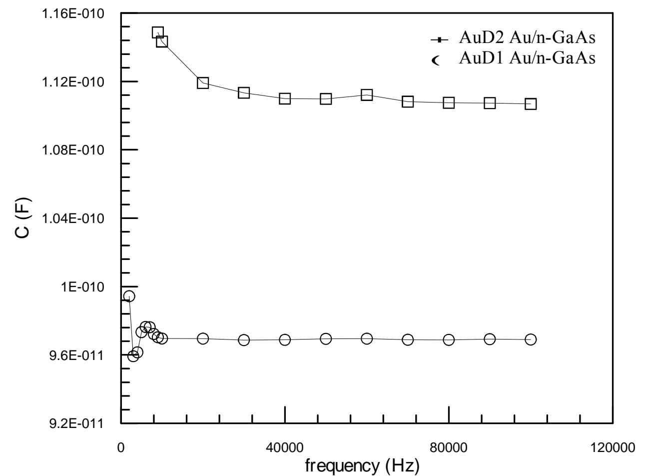

Fig. 7. The plot of capacitance vs. frequency of AuD1 and AuD2 MIS Schottky barrier diodes at 0.2 V.

Fig. 7 shows the capacitance-voltage plots of AuD1 and AuD2 MIS diodes at 0.2 V. As seen in Fig.7, the capacitance increases with decreasing frequency and at high frequencies, became almost constant. At low frequency, the capacitance measured is dominated by the depletion capacitance of the Schottky diode, which is bias-dependent and frequency-independent. The values of the capacitance at the high frequency region are only space-charge capacitance. As the frequency is increased, the total diode capacitance is affected not only by the depletion capacitance, but also by the bulk resistance and the dispersion capacitance, which is frequency-dependent and associated with hole or electron emission from slowly responding deep impurity levels [3].

4. Conclusions

The electrical properties of AuD1 and AuD2 MIS Schottky barrier diodes have been investigated by means of I-V and C-V measurements at room temperatures. The n value becomes quite higher than unity for MIS diode is attributed to the presence of a thin interfacial insulator layer between the metal and semiconductor. It was found that the introduction of a thin insulator layer between metal and n-GaAs reduced leakage current and increased barrier height. Our experimental results suggest that the interfacial layer lead to the formation of the tunnelling component of the current through the barrier. It is concluded that the interfacial insulator layer and interface states are responsible for the non-ideal behaviour of I–V characteristics. The values of N_{ss}, saturation current, and, barrier height are dependent on the thickness of the interfacial insulator layer. As the thickness of the interfacial insulator layer increases, the inreased density of surface states can not offer the possibility of improving the operation of GaAs based optoelectronic devices and for fabricating GaAs metal-insulator-semiconductor field effect transistors (MIS-FETS's). Finally, it can be said that the thickness of the interfacial insulator layer in controlling the electronic properties of Au/n-type GaAs Schottky diode is important parameter.

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