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The electrical characteristics of Cu/CuS/p-Si/Al structure

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Cu/CuS/*p*-Si/Al structure formed using CuS thin film on p-Si substrate. CuS thin film has been grown with using Successive Ionic Layer Adsorption and Reaction (SILAR) method. The Cu/CuS/*p*-Si/Al structure has demonstrated clearly rectifying behavior by the current-voltage (I-V) curves studied at room temperature. The characteristic parameters such as barrier height, ideality factor and series resistance of Cu/CuS/*p*-Si/Al structure have been calculated from the forward bias *I-V* and reverse bias C^{-2}-V characteristics. The ideality factor and barrier height have been obtained as n=1.63 and Φ_b=0.69 eV by applying a thermo-ionic emission theory. At high current densities in the forward direction, the series resistance effect has been observed. The values of R_s obtained from *dV/d(lnI) – I* and *H(I) – I* plots are near to each others (R_s=340.33 □ and R_s=346.24 □, respectively). In the same way, the barrier height calculated from C^{-2}-V characteristics have been varied from 0.523 to 0.601 eV. Furthermore, the density distribution of interface states of the multilayer device has been obtained from the semi-log forward bias *I-V* characteristics. It has been seen that the N_{ss} has almost an exponential rise with bias voltage from top of the valance band toward to mid gap.

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1. Introduction

As an important material with unique electronic, optical and chemical properties, copper mono sulfide (CuS) is a promising material with potential applications in many fields [1]. The cooper sulfide thin films have recently received considerable attention due to numerous technological applications in achievement of solar cells [2-4], in photo thermal conversion of solar energy, as selective radiation filters on architectural windows [5]. For growth of CuS thin films, many chemical growth techniques have been used. SILAR method is one of these. This method is easy, inexpensive and provide at atmosphere pressure and room temperature growth.

It is known that there are many reports on metal-semiconductor (MS), metal-interfacial layer-semiconductor (Multilayer) structures. Understanding of Schottky-barrier formation according to the interface layer is very interesting and attractive subject. Surface and interface properties of this structure play an important role in the electrical performance of metal-semiconductor Schottky diodes and multilayer structures with small dimensions. The performance of these devices especially depends on the formation of interfacial layer between metal and semiconductor, the interface states located between semiconductor-interfacial layer, series resistance and inhomogeneous barrier heights [6].

The barrier height is likely as a function of the interface atomic structure and the atomic in homogeneities at the MS interface which is caused by grain boundaries, multiple phases, facets, defects and a mixture of different phases [7].

One of the liquid phase methods for deposition of thin films is SILAR-method. The SILAR method was developed by Nicolau [8] for the deposition of zinc and cadmium chalcogenides thin films about 25 years ago. In this method, thin films are fabricated by alternate dipping into two solutions of each precursor ion for compound semiconductors. Therefore, the control of the film thickness becomes feasible by changing the number of the dipping cycles. Furthermore, atomically controlled multilayer thin films or super lattices can be fabricated by changing precursor solutions. Since the SILAR method depends only on immersing the substrate into the solutions, the deposition of films on large area can be achieved at low cost. [9].

In the literature, there are many reports about preparation of sandwich or multilayer structures. But, up to now, there has been no report on preparation of these structures by means of SILAR method. In this work, the Cu/CuS/p-Si/Al multilayer structure has been prepared by means of SILAR method and the characteristic parameters of this structure have been reported.

2. Experimental procedure

In this study, *p*-Si wafer (with (100) orientation, 400 μm thickness and 1-10 Ω-cm resistively) was used and then, the *p*-Si wafer was chemically cleaned by using the RCA cleaning procedure (i.e. 10 min boil in NH_3+H_2O_2+6H_2O followed by a 10 min HCl+ H_2O_2+6H_2O at 60°C) before making contacts. The ohmic contact was made by evaporating Al on the back of the substrate, then, was annealed at 580°C for 3 min in N_2 atmosphere. The native oxide on the front surface of the *p*-Si substrate was removed with using HF+10H_2O solution.

Finally, it was rinsed in de-ionised water for 30 s and was dried. After ohmic contact made, the ohmic contact side and the edges of the p-Si semiconductor substrate was covered by wax so that the polished and cleaned front side of the sample was exposed to apply the cationic precursor solution ($CuCl_2$). For the deposition of CuS thin film, a well-cleaned p-type Si substrate was immersed in the cationic precursor solution ($CuCl_2$) for 20 s, causing copper ions to be adsorbed on the surface of the p-type Si substrate. This substrate was immersed in doubly distilled water for 50 sec to prevent for irregular precipitation. The substrate was then immersed in the anionic precursor solution (Na_2S) for 20 s. Sulfide ions reacted with the adsorbed copper ions on the p-type Si substrate. The substrate was then immersed again in double-distilled water for 50 s. Thus, one cycle of CuS film deposition is completed. This process was repeated as 40 cycle for get homogeneous thin film. Then, the Cu dots with diameter of about 1.0 mm (the diode area = 7.85×10^{-3} cm^2) was evaporated on CuS thin film. In this way, the Cu/CuS/p-Si/Al structure was obtained. The current-voltage and capacitance-voltage characteristics of this structure were measured by using a HP 4140B picoampermeter and a HP model 4192A LF impedance analyzer, respectively, at room temperature and in the dark.

3. Results and discussion

The current-voltage relation in respect to the thermo-ionic emission theory in the presence of interfacial layer is given by [10];

$$I = AA^*T^2 \exp\left(\frac{-q\Phi_b}{kT}\right)\left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right] \quad (1)$$

where A is the effective area of diode, A^* is the effective Richardson constant of 32 A cm^{-2} K^{-2} for p-type-Si [10]; Φ_b is the barrier height; T is the temperature; q is the elementary charge; k is Boltzmann constant; R_s is the series resistance and n is the ideality factor. The n is 1 for an ideal diode. However, n has usually a value greater than unity. High values of n can be attributed to the presence of the interfacial layer and a wide distribution of low barrier height patches (or barrier in homogeneities), and to the bias voltage dependence of the barrier height [11-12]. The saturation current I_0 is denoted by [10];

$$I_0 = AA^*T^2 \exp\left(\frac{-q\Phi_b}{kT}\right) \quad (2)$$

I_0 is obtained by extrapolation of the forward or reverse bias current-voltage curve to zero applied voltage. The slope of linear portion of the *ln*(*I-V)* curve gives the ideality factor and the ideality factor can be express as below [10]:

$$n = \frac{q}{kT}\ln\left(\frac{dV}{d\ln I}\right) \quad (3)$$

The barrier height (Φ_b) is determined from the extrapolated I_o and is given as below [10];

$$\Phi_b = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_o}\right) \quad (4)$$

Fig. 1 presents the semi-log forward and reverses bias *I-V* characteristics of the Cu/CuS/p-Si/Al structure. The values of the ideality factor, saturation current and barrier height were calculated from the slope of the linear region of the forward bias *ln(I)-V* plot as to be $n=1.63$, $I_o=2.34\times10^{-7}A$ *and* $\Phi_b=0.69$ *eV* respectively at room temperature, by using Eqs.3 and 4. It is seen that the structure is not an ideal. In real metal-semiconductor contacts, deviation from ideal behavior is frequently observed and the *I–V* curves cannot be fit by equation (1). This non-ideal situation can be explained with thin interfacial layer and particular distribution of the interface states [13], the image force effect, recombination-generation and tunneling may be other reason of ideality factor value greater than unit [10]**.** The series resistance, leakage current, the presence of other transport mechanisms [10], the presence of a CuS thin interface layer [14] and inhomogeneous barrier heights [15,16] can be the most important causes of non ideal behavior. At high currents, there is a deviation of linear behavior due to series resistance, interfacial layer and interface states. On the other hand, there is absolute a saturation behavior at reverse current.

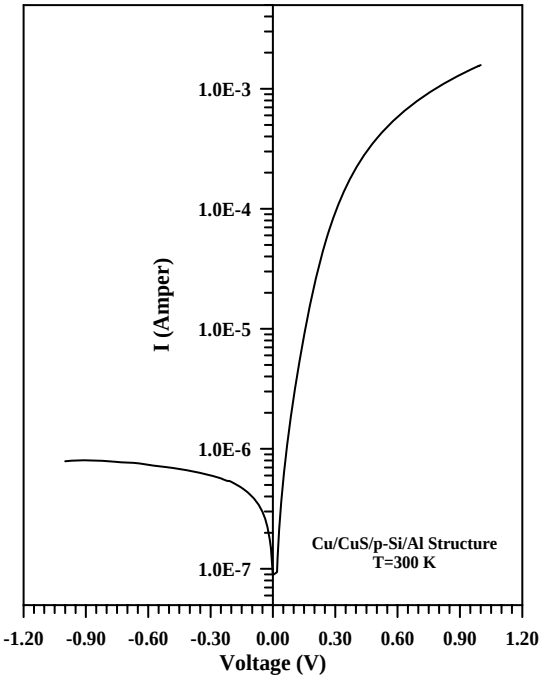

Fig. 1 The forward and reverse bias current-voltage characteristics of Cu/CuS/p-Si/Al MIS diode.

Usually the forward bias *I-V* characteristics are linear in the semi logarithmic scale at low voltages but deviate considerably from linearity due to the effect of parameters such as R_s and N_{ss} when the applied voltage is sufficiently large. The series resistance is significant in the downward curvature (non-linear region) of the forward bias I-V characteristics. The concavity of the forward bias I–V characteristics increases with increasing the series resistance value. The lower interface states density and the series resistance, the greater range over which the I-V curve yields at straight line. As the linear range of the forward I-V plots is reduced, the accuracy of the determination of barrier height and ideality factor becomes poorer. The barrier height, as well as the other diode parameters as the ideality factor *n* and the series resistance R_s can be calculated by means of a method developed by Cheung in the high current range where the I-V characteristics is not linear [17-18]. Cheung ′s functions can be written as follow [18];

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right) \tag{5}$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{6}$$

and

$$H(I) = IR_s + n\Phi_b \tag{7}$$

Where Φ_b is the barrier height obtained from data of downward curvature region in the forward bias *I-V* characteristics. Equation (5) should give a straight line for the data of downward curvature region in the forward bias *I-V* characteristics. The slope of the linear part of the *dV/d(lnI)* versus *I* will give R_s and its y-axis intercept will give *nq/kT*. Using the *n* value determined from equation (5) and the data of downward curvature region in the forward bias *I-V* characteristics in equation (6), a plot of *H(I)* versus *I* according to equation (6) will also give a straight line with y-axis intercept equal to $n\Phi_b$. The slope of this plot also provides a second determination of R_s that can be used to check the consistency of Cheung ′s approach. These plots are shown in Fig.2. The n, Φ_b, R_S parameters have been obtained from Eq.(5) as *n*=2.29, R_s=340.34 Ω and using Eq.(7) obtained as R_S=346.24 Ω, Φ_b=0.66 eV.

According to the these results, we can say that the series resistance values (Rs; *340.33Ω from dV/d(lnI)-I and 346.24 Ω from H(I)-I*) calculated from Cheung's functions are in good agreement with each other. However, it can be clearly seen that there is relatively a high difference between the values of the ideality factor obtained from the downward curvature regions of forward bias *I-V* plots and from the linear regions of the same characteristics.

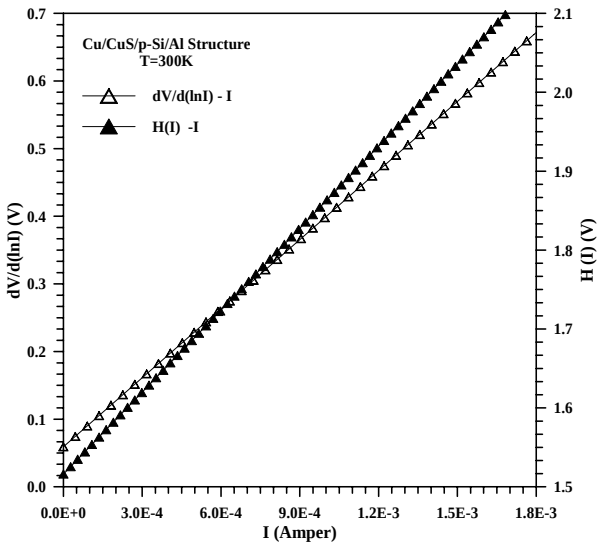

Fig. 2 Experimental dV/d(lnI) – I and H(I) - I curves of Cu/CuS/p-Si/Al MIS diode.

The reason of this difference can be attributed to the existence of effects such as the series resistance and the bias dependence of the barrier height according to the voltage drop across the interfacial layer and change of the interface states with bias in this concave region of the *I-V* plot [10]. According to these results, the series resistances can not be responsible for this non-ideal behavior of the *I-V* characteristics. On the other hand, interface state densities are also responsible from this concave region.

The *C–V* measurement is another method to determine the barrier height of devices by plotting C^{-2}-*V* for reverse bias. In metal-semiconductor contacts the depletion layer capacitance is given as follows [19],

$$C^{-2} = \frac{2(V_d + V)}{\varepsilon_s \varepsilon_0 q A^2 N_a} \tag{8}$$

where V_d is the diffusion potential at zero bias which is determined from the extrapolation of the linear $1/C^2$-*V* plot to the *V* axis, *A* is the effective area of the diode and ε_s is the dielectric constant of the semiconductor, N_a is the concentration of ionized acceptors and it is written as [19]:

$$N_a = N_v \exp(V_p / kT) \tag{9}$$

where V_p is the potential difference between the Fermi energy level (E_f) and the top of the valance band in the neutral region of *p-Si*, which is directly equal to E_f, N_v ($1.04\text{x}10^{19}$ cm^{-3}) is density of states in the valence band at T=300 K [10].

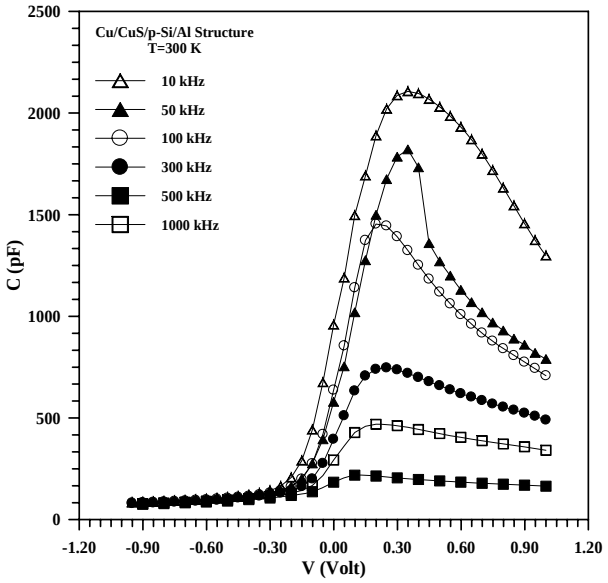

Fig. 3 The forward and reverse bias C-V characteristics of the Cu/CuS/p-Si/Al MIS structure at various frequencies.

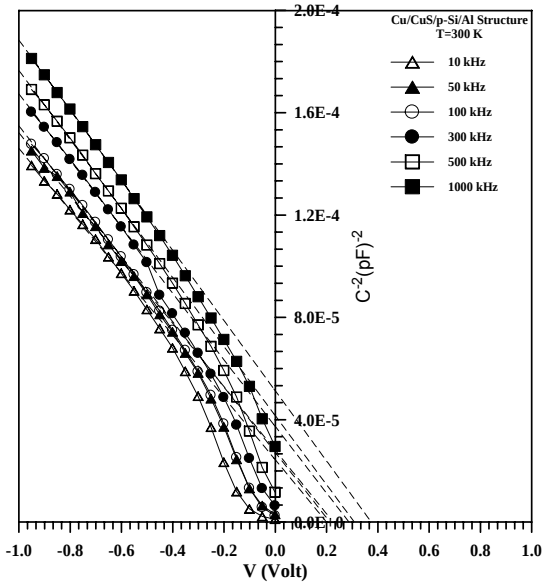

Fig. 4 The reverse-bias C^{-2}-V characteristics of the Cu/CuS/p-Si/Al MIS structure at various frequencies.

Fig. 3 shows the forward and reverse bias *C-V* characteristics at five different frequencies of the Cu/CuS/*p-Si* structure. The peak values of capacitance at low frequencies have increased. The dependence of the depletion capacitance of a metal-semiconductor contact upon frequency can also arise due to the presence of deep lying impurities in the depletion region [20]. Also, it is observed that the low-frequency capacitance more rapidly increases with the applied bias than high-frequency capacitance. This observation may be attributed to the capacitive response of interface states to the measurement frequency. In general, at sufficiently high frequencies (f≥500 kHz) the interface states do not contribute to the capacitance [21]. The C^{-2}-*V* plots, which are carried out in the frequency range of 50 kHz-1000 kHz are presented in Fig. 4. As can be seen from Fig. 4, the C^{-2}-*V* plots are linear in a wide voltage region even at moderate frequencies. The slope and intercept voltage of the C^{-2}-*V* plot is a function of interface layer and the doping of the semiconductor [22-24]. The curvature concave downward in the -0.3 V to 0.0 V range for each frequency in C^{-2}-*V* plot indicates the existence of interface states which are in equilibrium with the semiconductor.

The value of the barrier height Φ_b can be calculated by the following equation, using *C-V* measurements [10],

$$\phi_b = V_p + V_d \tag{10}$$

The V_p value can be calculated by using N_a and N_v. For the Cu/CuS/*p-Si/Al* structure, the N_a and Φ_b values calculated from the slopes of the C^{-2}-*V* plots are dependent on frequencies (see Table 1). As can be seen in Table 1, the barrier height calculated from C^{-2}-V characteristics have varied from 0.523 to 0,601 eV as a function of frequency. Such behavior of C^{-2}-*V* plots can be entirely explained on the basis of the assumption that only some of the interface states follow the applied ac signal at low frequencies. Especially at high frequencies (f ≥ 1 MHz), the peak values of *C-V* plots shows clearly a decreasing. It can also be seen that the barrier heights, obtained from *I–V* measurements are bigger than those obtained from *C–V* measurements. According to Werner and Guttler [25], spatial inhomogeneities at the metal-semiconductor interface can also cause such differences. Another possibility may be the transport mechanism in these devices which is not purely due to thermionic emission. For this structure, the barrier height obtained from *I–V* measurement is sensitive to voltage or electric field, whereas the barrier height obtained from *C–V* is not.

Table 1. The parameters obtained from reverse bias C^{-2}-V characteristics of the Cu/CuS/p-Si/Al structure as a function of frequency.

Frequency (kHz)	V_d (eV)	N_a (cm^{-3})	V_n (eV)	ϕ_b (eV)
50	0.226	$9.8\ 10^{13}$	0.297	0.523
100	0.213	$9.6\ 10^{13}$	0.299	0.512
300	0.287	$9.4\ 10^{13}$	0.300	0.587
500	0.308	$1.1\ 10^{14}$	0.300	0.608
1000	0.300	$8.9\ 10^{13}$	0.301	0.601

The values of carrier concentrations obtained from the reverse bias C^{-2}-V characteristics of the Cu/CuS/p-Si/Al structure have been given in Table 1. The doping concentrations N_a were found to be between $8.9\ 10^{13}$ cm^{-3}–$1.1\ 10^{14}$ cm^{-3}**.** The average N_a value calculated from C^{-2}-V plot is about as $1.02\ x10^{14}$ cm^{-3}. On the other hand, N_a is calculated as $1.3x10^{15}$ cm^{-3} by using the resistivity of p-Si. The change in slope in thee plots of Fig. 4 could be interpreted though, as a change in the spatial distribution of thus acceptor ions at equation (9).

The non-linearity of I-V characteristics of the Cu/CuS/p-Si/A. structure at high bias values have showed presence of interface states, in which at equilibrium with the semiconductor [10]. Nuvertheless, this multilayer structure exhibit excellent rectification characteristics with a relatively low leakage current density. In this study, the interface state at the CuS/p-Si interface in the Si band-gap has been determined from the downward concave curvature of the forward bias *I-V* plots in Fig.1. In the downward concave-curvature region, the ideality factor, n, is rather controlled by the interface states and the series resistance. The energy distribution of the interface states thus can be determined from data of this region of the semi-log forward bias I-V. The curve obtained by taking into account the bias dependence of the ideality factor and barrier height is given in Fig. 5. Furthermore, in p-type semiconductors, the energy of the interface states E_{ss} with respect to the top of the valance band at the surface of semiconductor is given by [10]

$$E_{ss} - E_v = q(\Phi_e - V) \qquad (9)$$

The profile of interface states (N_{ss}) as a function of (E_{ss}-E_v) is determined by using Eq. 9 and shown in Fig. 5. As can be seen in Fig. 5, the exponential increase in the interface state density exist from the top of valance band towards to midgap is very apparent. These surface states at the CuS/*p-Si* interface can be viewed as electronic states generated by unsaturated dangling bonds of the surface atoms. It is now well accepted that these states deeply affect electronic process taking place at the interface. Minimum value of interface state density is evaluated as $7.51x10^{16}$ $m^{-2}.eV^{-1}$ at about 0.61 eV. Maximum value of interface state density is evaluated as $4.38x10^{17}$ $m^{-2}.eV^{-1}$ at about 0.46 eV.

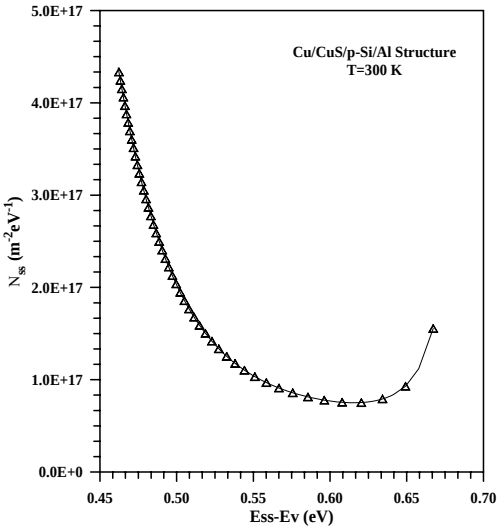

Fig .5 The energy distribution curves of the interface states obtained from the forward bias I-V characteristics of Cu/CuS/p-Si/Al MIS diode as a function of (E_c-E_{ss}).

4. Conclusion

In this study, we prepared Cu/CuS/p-Si/Al multilayer structure by using SILAR method and investigated the electrical characteristics of this structure with *I-V* and *C-V* measurements. There are many growth techniques for thin film growths but according to the other methods, SILAR method is simple, fast, sensitive, cheap and easy to prepare interfacial layer for multilayer structure. According to our results, we can say that the CuS interfacial layer grown with SILAR method can be confidently used at the Cu/CuS/p-Si/Al multilayer structures.

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