The influence of the SiO_2 gate insulator thickness to the performance and Bias-voltage stress stability of ZnO thin-film-transistors

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Top-contact thin film transistors using radio frequency sputtering ZnO and SiO_2 films as channel layer and gate insulator are fabricated in this work. The performance of ZnO-TFTs with different thickness SiO_2 dielectrics are compared. The experiment results show that the SiO_2 dielectric thickness plays an important role on enhancing both the field effect mobility and bias stability of the devices. The device with 150 nm thick SiO_2 insulator has much better performances: its mobility reaches 6.1cm^2/V.S, subthreshold swing is 1.6 V/Dec, bias-voltage stress induced ΔV_{th} is 3V.. Comparison of 150 nm thickness with 200 nm thickness and 300 nm thickness SiO_2 insulator based devices shows that the field effect mobility improved by 250% and 150% and sub-threshold swing decreased by 60% and 25%, respectively, while bias-voltage stress instability reduced from 6V and 9.4V to 3V. The improved performance can be attributed to that the thinner insulator has larger capacitance and contains smaller amounts of total trap centers compared with the thicker dielectrics.

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1. Introduction

Transparent electronics have potential opportunities to create next generation optoelectronic devices and invisible computing.[1] ZnO is one of the most interesting II–IV compound semiconductors with a wide direct band gap of 3.34 eV, transparency in the visible range and high carrier mobility. Based on these characteristics, TFTs using ZnO as an active channel layer are being intensely explored.[1–5] For ZnO-TFTs, both the active layers and insulators play very important roles on the performance of the devices. In order to obtain higher performance ZnO-TFTs, much effort have to be paid to improve the ZnO and dielectric layers fabrication process. Therefore, much work has been done to optimize ZnO active layer fabrication process.[6-9] However, investigations about the influence of insulator fabrication parameters on the TFT performance are very few.

In the present work, SiO_2 films were deposited by using radio frequency (RF) magnetron sputtering with different thickness of 150, 200 and 300 nm. The electrical properties of the SiO_2 films and the influence of SiO_2 thickness on the performances and Bias-voltage stability have been investigated. The experiment results show the 150 nm thickness insulator based device shows the best performance such as: field effect mobility of 6.1 cm^2/V.s, on/off ratio of 1.1x10^7, subthreshold voltage of 1.6 V/dec particularly a much small threshold voltage shift of 3 V after a 15 V gate voltage stressed for 1 hour.

2. Experimental detail

Three kinds of TFTs with different OPP SiO_2 films as the gate insulators are constructed (as shown in fig. 1a). The devices are fabricated by using ITO-glasses as the substrates and gate electrodes. Initially, different thickness SiO_2 films (150 nm, 200 nm and 300 nm) are deposited on the cleaned ITO glass substrate (Corning 1737) by RF magnetron sputtering at room temperature using a Si target. The deposition conditions for SiO_2 films were: total sputtering pressure of ~0.5 Pa, gas mixing ratio of Ar: O_2 =70:30 and input power of ~100 W. The ZnO layers were deposited at room temperature using a ZnO target (99.99%, 3 in.) at lower input power of 40 W, gas mixing ratio of Ar:O_2 (96/4), and total pressure of 1 Pa. After deposition of ZnO layer, about 200 nm Al was deposited by vacuum evaporation to form the source and drain electrodes through a shadow-mask with the channel width (W) of 500 μm and channel length (L) of 130 μm. The thickness of the film was measured by the alpha step (Dektak 3st). The electrical characteristics of ZnO-TFTs and SiO_2 dielectrics were measured using Agilent E3647A Dual output DC power supply and Keithley 6485 Picoammeter and related software.

3. Result and discussion

Fig. 1(b) shows the current to voltage characteristics of the SiO_2 capacitor with ITO and Al as the electrodes, the electrode area is 30 mm^2. From the figure we can see

that the leakage current is only 5.6×10-9 A for the 300 nm sputtering SiO_2 films, even the electric field strength reach to 2 MV/cm.

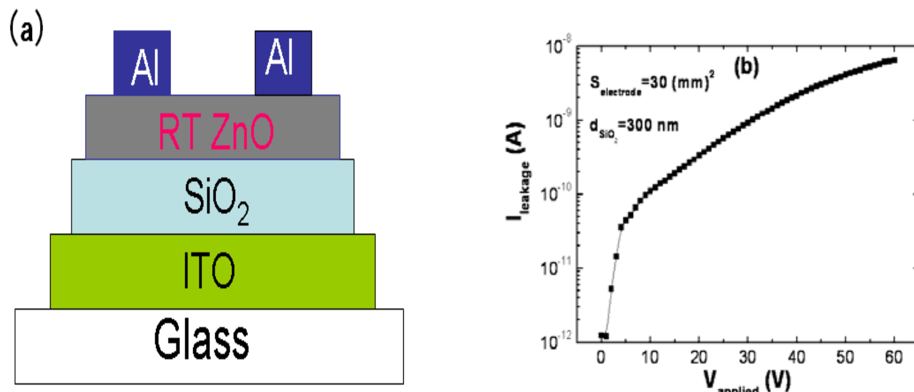

Fig..1. The schematic structure of SiO_2-based ZnO-TFT (a) the leakage current of the sputtering SiO_2 films (b)

Fig. 2 shows the I_{DS}-V_{DS} curves of the ZnO-TFTs with different thickness SiO_2 insulators for the gate voltage (V_G) from 0 V to 45 V. It is shown that all the devices have n-channel, since electrons are generated by the positive V_{GS}. For all the output characteristics, the lack of current crowd at the low V_{DS} regions, indicate a good contact between the source/drain electrodes and active layers. From fig. 2 we can see that the on-state current is $1.5x10^{-4}$ A for Device a while these values for Device b and c are only $1x10^{-4}$ and $2.5x10^{-5}$ A, respectively.

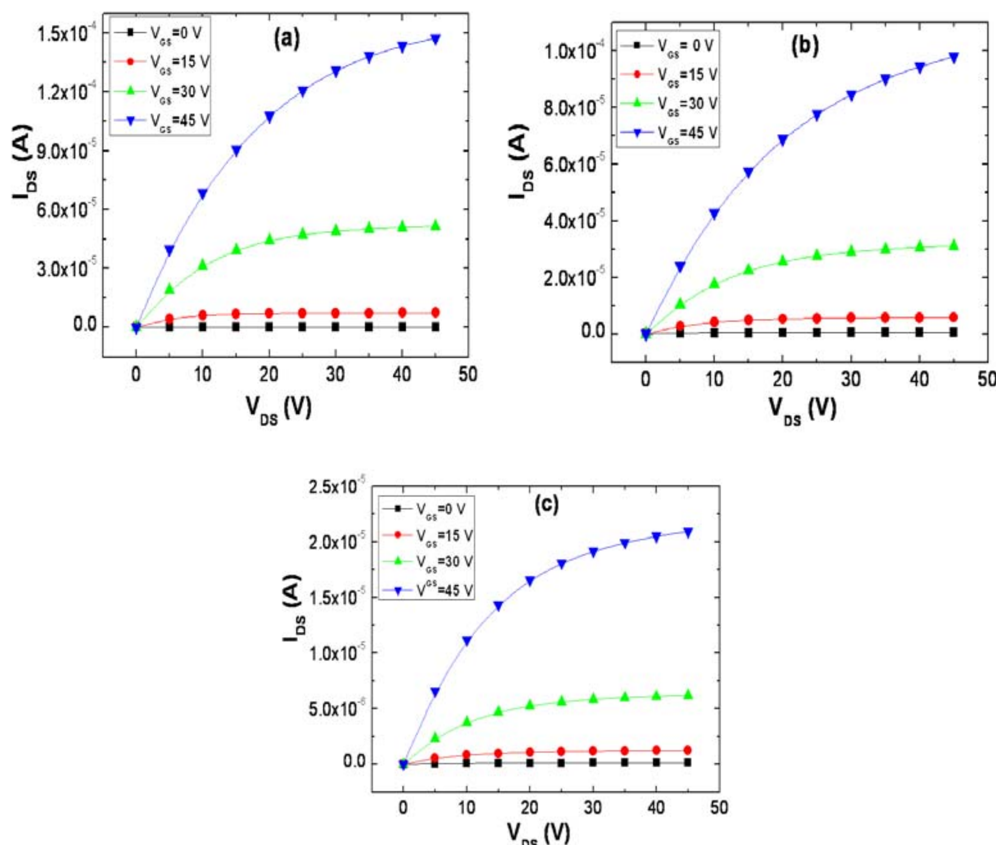

Fig. 2. The drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) curves for the different thickness SiO_2 insulator ZnO-TFTs. (a) 150 nm (b) 200 nm (c) 300 nm

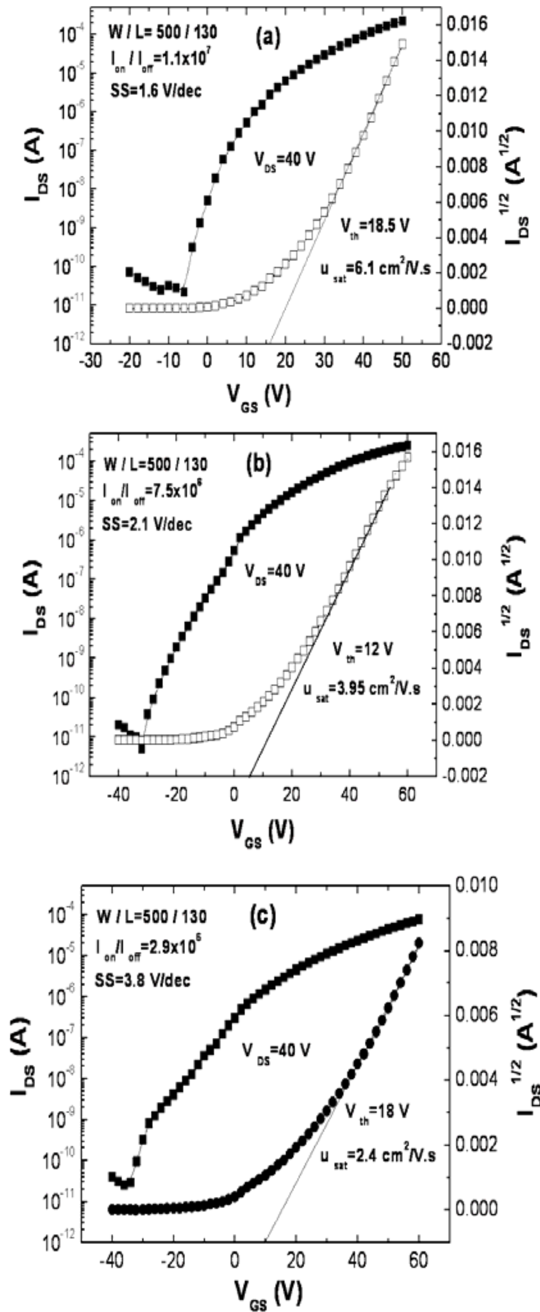

Fig. 3. Corresponding transfer characteristics (I_{DS} versus Vg) and the $I_{DS}^{1/2}$-V_G curves for the ZnO-TFTs with different thickness SiO_2 insulator at a fixed V_{DS} = 40 V s. (a) 150 nm (b) 200 nm (c) 300 nm.

Fig.3 shows the corresponding transfer characteristics of I_{DS} versus V_{GS} and the $I_{DS}^{1/2}$-V_G curves for the ZnO-TFTs *at a fixed V_{DS} = 40 V*. The off-state current are 2.1×10^{-11}, 4.5×10^{-12} and 2.8×10^{-11} A respectively. The on/off ratio for the 150, 200 and 300 nm SiO_2 insulator based devices are 1.1×10^7, 5×10^7 and 2.9×10^6, respectively.

From the $I_{DS}^{1/2}$-V_G curves as shown in Fig.3, the channel mobility (μ_{sat}) and threshold voltage (V_{th}) can be extracted by fitting straight lines into the plots of the square root of drain current vs. gate-source voltage, according to the expression:

$$I_{DS} = \frac{C_i W}{2L}(V_{GS} - V_{TH})^2 \quad V_{DS}>V_{GS}-V_{TH} \qquad (1)$$

where C_i is the capacitance per unit area of the insulator layer (C_i for Device a, b and c is 20, 15 and 10 nF/cm^2, respectively), W and L are the channel width and length, V_{DS} and V_{GS} are the drain-source voltage and gate-source voltage, respectively. The calculated channel mobility is 6.1, 3.95 and 2.4 cm^2/V·s for the 150, 200 and 300 nm thickness SiO_2 dielectric based ZnO-TFTs, respectively. It is that with the insulator thickness decrease the field effect mobility for the devices shows a increase trend.

The sub-threshold voltage swing (SS) defined as the voltage required increasing the drain current by a factor of 10. From the transfer characteristics we can also determine the gate voltage swing, SS, through the relation:

$$SS = \frac{dV_{GS}}{d(LogI_{DS})} \qquad (2)$$

Here, we extracted the values of 1.6 V/dec, 2.1 V/dec and 3.8 V/dec for Device a, b and c under analysis. From *SS* we can infer the maximum density of surface states at the semiconductor/dielectric interface as:[11]

$$N_{\max}^{SS} = [\frac{SLog(e)}{(kT/q)} - 1]\frac{C_i}{q} \qquad (3)$$

and taking into account the value of C_i, N^{SS}max of 3.1×10^{12} cm^{-2}, 3×10^{12} cm^{-2} and 3.3×10^{12} cm^{-2} are calculated for devices a, b, c, respectively. These results indicate that with the decrease of the insulator thickness the SS value decrease accordingly and the nearly same N^{SS}max values indicate a similar semiconductor/dielectric interface for the three devices. It can be seen that with the decreasing the thickness of SiO_2, the mobility increase, while N^{ss}_{max} have no obviously change. This phenomenon indicates that the increase of mobility is due to larger capacitance with thinner dielectric, which formed larger induced current,

rather than due to the interface improvement.

Other than the improvements mentioned above, the most important result of this study is that the bias stability of the devices was remarkably enhanced by choosing proper thickness insulator.

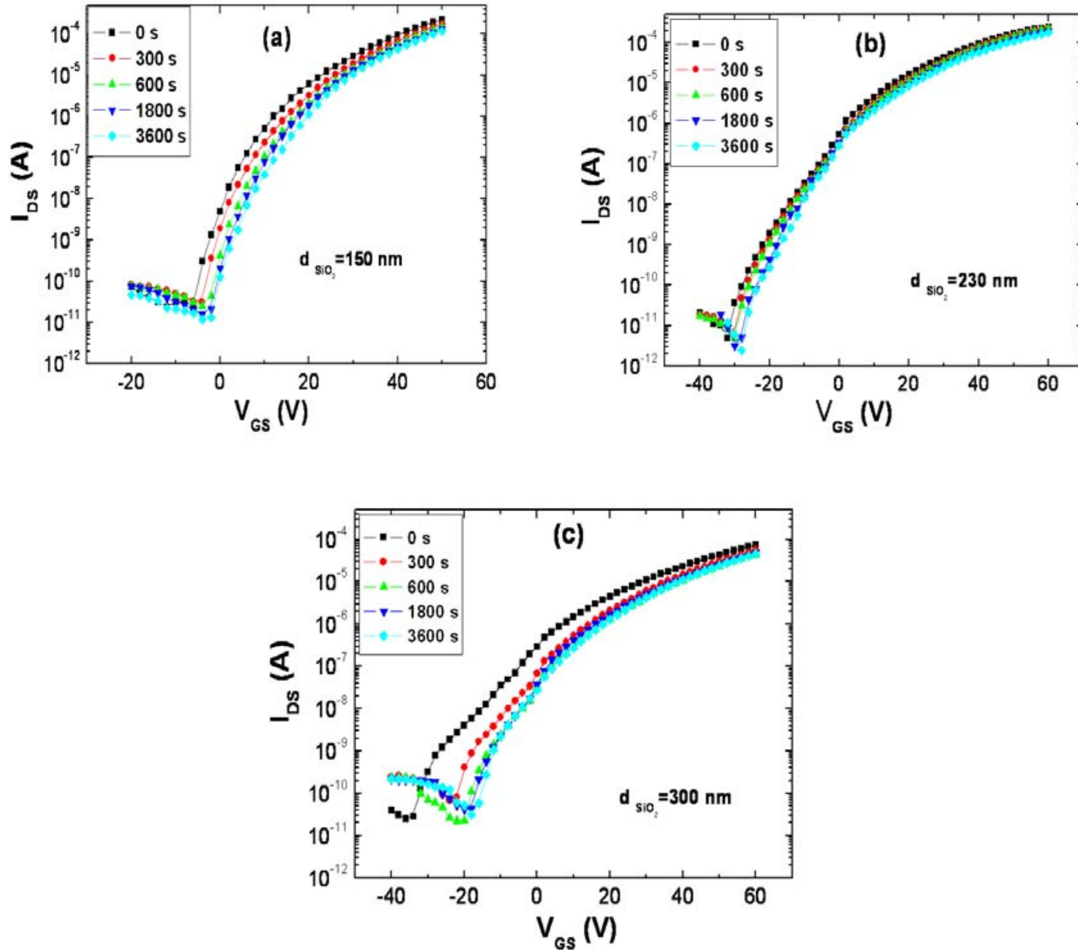

Fig. 4. The transfer curves of different OPP SiO_2 based ZnO-TFTs, the gate bias of 15, 23 and 30 V were applied to device a, b and c for an hour, respectively, at room temperature in atmosphere. (a) 150 nm (b) 200 nm and (c) 300 nm.

In order to maintain a similar electric field strength, bias voltages of 15, 23 and 30 V were used to stress the devices that with a insulator thickness of 150, 200 and 300 nm, respectively. From figure 4 we can see that, all the transfer curves show a positive shift by the positive gate voltage stress. The saturation mobility (μ_{sat}) and SS value before the stress were nearly not changed for all the three devices. Such phenomenon results from negative charge being trapped at the insulator/channel interface or getting injected into the gate dielectric. Due to the negative trapped charge screening the applied gate voltage, thus a larger positive voltage is required for the device to turn on and reach saturation.

Fig. 5 shows the time dependences of the threshold voltage shift for the different thickness SiO_2 insulator based ZnO-TFTs. All the devices show a logarithmic time-dependent threshold voltage shift, indicative of charge trapping as a dominant cause of instability. [12] The threshold voltage shift

$$\Delta Vth = Q(t)/\ Cox, \tag{4}$$

where Q(t)is the total charge that get trapped at the channel /dielectric interface or in the dielectric for any given time t, Cox is the capacitance per unit area of the gate dielectric .the total trapped charge can be obtained by integrating over time and thickness of the gate dielectric in which traps are present.

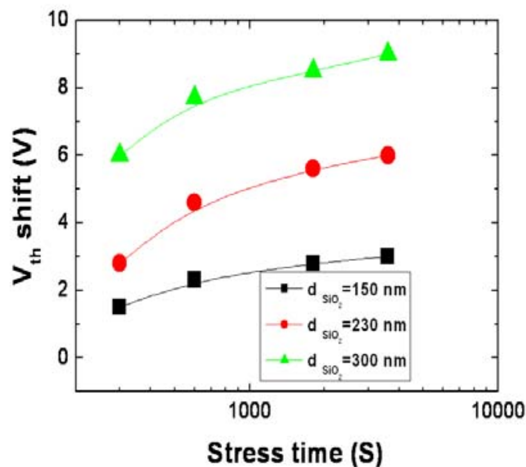

Fig. 5. Time dependent ΔV_{th} under gate voltage stress for different thickness SiO_2 based ZnO-TFTs.

Assuming Ntr is the density of traps in the dielectric, $\omega(x)=\omega(0)\exp(-x/\lambda)$ is the tunneling probability, λ is the tunneling constant, which is proportional to the applied voltage and dielectric parameter. The ΔVth can be expressed as

$$\Delta V_{th} = R_0 \log(t/t_0) \quad (5)$$

R_0 is decay rate constant which is proportional to the product of Ntr (cm^{-3}) and λ(cm). The relation (5) shows a logarithmic time dependence of the threshold voltage shift

In our experiments, the threshold voltage shift for the 150, 200 and 300 nm OPP insulator based devices is 3 V, 6 V and 9.4 V, respectively. The thinner the SiO_2 film is, the smaller the ΔVth is. This phenomenon can be explained by using Formula (4), For a thinner dielectric, its total trapped charge Q(t) is smaller than that of the thicker films, while its capacitance Cox is larger than that of thick dielectric, resulting in a smaller threshold voltage shift. Which is the main reason for the better bias stability of the 150 nm thickness insulator based ZnO-TFT.

Overall, the 150 nm thickness SiO_2 dielectric based ZnO-TFT has the best performance with an on/off ratio of 1.1×10^7, field effect mobility of 6.1 cm^2/V.s and sub-threshold swing of 1.6 V/dec. Other than these improvements, the Vth shift also decreases from 9.4 V to 3 V when the insulator thickness was reduced from 300 nm to 150 nm. The experiment results indicate that the insulator thickness play a much important role on the overall performance of the ZnO-TFTs. The improved performance can be attributed to that the thinner insulator contains much fewer trap centers compared with the thicker dielectrics.

4. Conclusions

In summary, top-contact TFTs using ZnO as channel layer and RF magnetron sputtering SiO_2 as gate dielectrics were fabricated. The effect of insulator thickness on the ZnO-TFTs performances was investigated. As the insulator get thinner, electrical properties of the ZnO-TFTs improved obviously. The device with best performance is obtained with 150 nm thickness SiO_2 dielectric. Comparison of 150 nm thickness with 200 nm thickness and 300 nm thickness SiO_2 insulator based devices shows that the field effect mobility improved by 250% and 150% and sub-threshold swing decreased by 60% and 25%, respectively. The improved performance can be attributed to that the thinner insulator contains small amount of trap centers compared with the thicker dielectrics.

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