Three dimensional numerical modeling and simulation of a nano SOI MOSFET photodetector

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This paper deals with three dimensional numerical modeling of an optically controlled nano SOI MOSFET photodetector for OEIC photoreceiver design. The exact potential potential profile of the device under illuminated condition has been computed numerically by solving 3D Poisson's equation using Liebmann's iteration method.The electric field profile and mobility of the carriers have also been studied extensively under illuminated condition to have an in depth analysis. The drain characteristics and transfer characteristics are also presented in this paper. The results show that the device characteristics are strongly influenced by incident optical radiation. The model enables one to estimate various parameters which determine the potential use of this device for photo detection in OEIC photoreceivers.

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1. Introduction

The full integration of photonic elements into the silicon-based electronics of the optical communications infrastructure has become one of the major focuses of opto- electronics industry. In the context of optical integration, a photo-detector based on a MOSFET structure would represent a highly practical and uniquely scalable opto-electronic component. Therefore silicon based photodetectors have received wide spread attention. The main role of a photo detector is to interpret the information contained in the optical signal. The photodetector should have some desirable qualities such as high response in the emission wave length range of the optical source being used, a minimum addition of noise to the system, a fast response speed to handle the sufficient data rate, insensitive to variations in temperature and should be compatible with the physical dimensions of the optical fiber in order to process an optical signal which is weakened and distorted when it emerges from the end of the fiber. Optical receivers use conventional photodetectors in discrete form in conjunction with other signal processing units realized with discrete active components [1]. The speed of such photodetectors is seriously limited by the parasitic inductances and capacitances introduced by the interconnections of various stages. The overall performance of the optical receiver can be greatly improved by monolithically integrating the electronic and other optoelectronic components in the same chip known as OEIC. The SOI MOSFET structure which has a better sensitivity and responsivity can very well act as a high speed photodetector for their possible use in optical receivers of future generation optical communication systems. SOI MOSFET is generally preferred because of the following reasons. i) All individual devices are separated by fabricating it on the insulator. ii) At a fixed operating voltage, circuit speed is up to 30% faster than bulk counterparts. iii) Reduced power consumption upto 80%. iv) Operating voltage levels can be reduced while maintaining circuit speed advantage over bulk silicon v) It can operate at temperatures as high as 350º C, compared to bulk or epi circuits. vi). It is less sensitive to alpha-particle soft errors & other radiation-induced effects.

The theoretical models developed by many researchers showed that the device characteristics were strongly influenced by incident optical radiation. The optically gated FET structures have been found to have better sensitivity as compared to their conventional counter part and several works were reported. Most of the works done to date on fully and partially depleted SOI MOSFET's based photodetectors used the drain current variation subsequent to light absorption as a measure of photon densities. A three dimensional numerical modeling of a nano MISFET photodetector and GaAs MESFET photodetector were reported[1,2,3].W.Zhang, Mansun Chan have analyzed the performance of floating Gate/Body Tied NMOS Photo-Detector on SOI Substrate[4,5]. G. Masini and L. Colace proved that Germanium films on Silicon provide a practical method for the fabrication of photo-detectors on conventional CMOS chips [6,7]. S. Sahni and E. Yablonovitch [8] demonstrated a novel Ge photo-detector based on a transistor design that utilizes secondary photo-

conductivity. They discussed the creation of charge separation when a Infra -red light was incident on the Ge due to the large valence band offset between Si and Ge. The excess photo-holes in the Ge can attract additional electrons in the Si channel and modulate its conductance. In Ref [9,10] three-dimensional phototransistors in 3D silicon-on-insulator technology is discussed. The authors have shown that SOI can be used for low light intensities. L. Harik et.al [11] presented a method to measure light intensity in a floating body partially depleted SOI MOSFET. The photo-generated charge density in the MOSFET is converted into a charge pumping frequency needed to maintain the drain current at a constant value.

In this paper, we have developed 3D numerical model of a SOI MOSFET as a photodetector for the OEIC applications. The 3D Poisson's equation has been solved numerically to obtain various device parameters such as field profile, mobility of the carriers, potential profile photocurrent, transcondutance and responsivity under the illuminated condition .The Liebmann's iteration method is used because of the following advantages [12]. i) Arbitrary choice of initial values ii) very low error rate iii)established convergence iv) unconditionally stable.

1.1 Photo response of SOI MOSFET

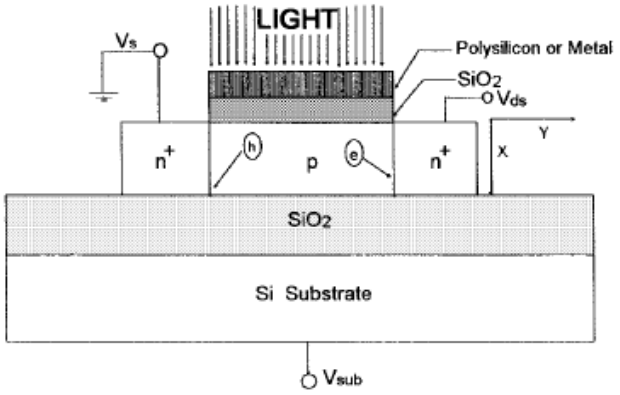

Fig. 1 Schematic diagram of SOI MOSFET under illumination.

The schematic structure of an illuminated SOI MOSFET is shown in Fig. 1 along with the coordinates. The illumination is incident on the device at a perpendicular direction to the surface of the transparent/semi-transparent metal gate. The intensity of illumination is uniform along the direction parallel to the surface. Thus, the generation rate varies only in the vertical x direction and decreased exponentially. The excess carries generated also vary along x direction and is uniform in y direction. The illumination causes production of excess electron hole pairs (E–H pairs) in the silicon film. The holes move toward the source and electrons move toward the drain under the influence of drain source voltage. A photo voltage (V_{op}) across the source film junction is developed increasing the effective gate voltage. The doping concentration of the film is considered to be non uniform and assumed a Gaussian distribution type [13]. In sub-threshold and linear regimes with small drain to source voltage, the drain current is small and the Poisson's equation alone is sufficient [14] to describe the device properties. At low drain source voltages the potential $\psi(x,y)$ can be approximated by a simple parabolic function [15].

There are several methods to make photo detectors on SOI substrate. A floating gate MOSFET on SOI substrate, operating in its lateral bipolar mode, is photon sensitive. The gate-body terminal is left floating so that the potential can be modulated by illumination. The depletion region induced by the floating gate separates the optically generated electron–hole pairs in the direction perpendicular to the current. This increases the body potential and induces positive charges to the gate due to the gate/body tie. It results in further turn on of the NMOSFET and extra optical current. One step further, the SOI MOSFET gate and body can be tied together. The positive feedback between the body and gate enables this device have a high responsivity [4]. A similar device can be found on the bulk CMOS technology: the gate-well tied PMOSFET.

A photo detector using MOSFET with quantum channels is also get prominence importance in recent days [12]. It comprises a quantum channel formed on an activated SOI wafer, a gate oxide film covering said quantum channel; a gate formed so as to control carrier current at said quantum channel; a source and a drain formed at both ends of said channel area; and metal layers connected with said gate, said source and said drain. Thus, the photo detector according to the present invention can obtain more excellent photocurrent characteristics compared with the existing SOI MOSFET device by forming quantum channels on the SOI MOSFET. The MOSFET with quantum channels according to the present invention can be used as a good photo detector maintaining advantages of the existing MOSFET such as ease in integration and high speed.

2. Modeling of SOI MOSFET

To obtain the potential field profile, the 3D Poisson's Equation is numerically solved by considering the entire channel length to be divided in to large number of strips. Thus we will obtain the potential at every point in the channel.

$$\frac{\partial^2\psi(x,y,z)}{\partial x^2}+\frac{\partial^2\psi(x,y,z)}{\partial y^2}+\frac{\partial^2\psi(x,y,z)}{\partial z^2}=\frac{-q(N_A+\Delta n)}{\varepsilon_{si}} \qquad (1)$$

where N_A is the doping concentration and $\psi(x,y,z)$ is the potential at a particular point.

Boundary conditions with respect to the thickness of the oxide layer are given by,

$$\psi(0,y,z)-\frac{t_{oxf}}{\varepsilon_{ox}}\left[\varepsilon_{si}\left|\frac{\partial\psi(x,y,z)}{\partial x}\right|_{x=0}-Q_{it}^{f}\right]=V_{gf}-V_{fb}^{f} \qquad (2)$$

$$\psi(t_s, y, z) - \frac{t_{oxb}}{\varepsilon_{ox}}\left[\varepsilon_{si}\left|\frac{\partial\psi(x,y,z)}{\partial x}\right|_{x=t_s} + Q_{it}^{b}\right] = V_{gb} - V_{fb}^{b} \qquad (3)$$

Boundary conditions with respect to length of the channel is given by,

$$\psi(x,0,z) = V_{bi} + V_{op} \qquad (4)$$

$$\psi(x, L_{eff}, z) = V_{bi} + V_{ds} + V_{op} \qquad (5)$$

Boundary conditions with respect to width of the channel is given by,

$$\psi(x,y,0) - \frac{t_{oxw}}{\varepsilon_{ox}}\left[\varepsilon_{si}\left|\frac{\partial\psi(x,y,z)}{\partial z}\right|_{z=0} - Q_{it}^{f}\right] = V_{gf} - V_{fb}^{f} \qquad (6)$$

$$\psi(x,y,W) + \frac{t_{oxw}}{\varepsilon_{ox}}\left[\varepsilon_{si}\left|\frac{\partial\psi(x,y,z)}{\partial z}\right|_{z=W} + Q_{it}^{f}\right] = V_{gf} - V_{fb}^{f} \qquad (7)$$

The boundary conditions given by (2) and (3) indicate that the potential applied at the front (back) gate is the sum of the potential at the front (back) Si–SiO_2 interface and the drop across the front (back) gate oxide. In (2) and (3), V_{gf} and V_{gb} are the flat band voltages and Q_{it}^{f} and Q_{it}^{b} are the interface trapped charges associated with the front and back gates respectively, and ε_{si} and ε_{ox} are the permittivity for silicon and silicon dioxide, respectively. Equations (4) and (5) represent the boundary conditions at the source and drain ends of the channel, V_{bi} being the built-in potential of the n^+ -p junctions and V_{ds} is the drain-to-source applied voltage. Equations (6) and (7) indicate that the potential applied at the front gate is the sum of the surface potential at the edge of the transistor and the drop across the sidewall oxide.

In order to obtain the surface potential as a function of x and y, eqn.1 has been solved using the boundary conditions 2 to 7. The potential at the surface end of the gate is the sum of built-in-voltage and applied drain voltage. The effective gate voltage at the semiconductor-insulator interface is the difference between V_G and $V_{FB,}$ where V_{FB} is the flat band voltage of the device and an electric field at the edge of the depletion region is zero.The excess carriers generated per unit volume (Δn) in the semiconductor due to the incident optical power is given by,

$$\Delta n = \frac{\sqrt{1 + \dfrac{4\tau_l P_{opt}(1-R_m)(1-R_i)(1-R_s)(1-e^{-\alpha W_m})}{W_m h\gamma n_i}} - 1}{\dfrac{2P_{opt}(1-R_m)(1-R_i)(1-R_s)(1-e^{-\alpha W_m})}{W_m h\gamma n_i}} \qquad (8)$$

where W_m is the maximum width of the depletion layer , τ_l is the mean life time of minority carriers in illuminated condition, P_{opt} is incident optical power density, h is Planck's constant, γ is operating frequency, α is absorption coefficient of semiconductor, $R_{m,}$ R_i, R_s are the reflection coefficients at metal gate entrance, gate-insulator interface and insulator-semiconductor interface respectively.

The maximum width of the depletion layer is given by,

$$W_m = \left[4\varepsilon_s \ln(N_A/n_i)/q\beta N_A\right]^{\frac{1}{2}} \qquad (9)$$

where n_i is the intrinsic carrier concentration, q is the charge of an electron and β=q/kT , k being the Boltzman's constant and T is the absolute temperature.

The mean life time of the minority carriers in the illuminated condition, τ_l can be written as ,

$$\tau_l = \left(n_i/(n_i + \Delta n)\right)\tau \qquad (10)$$

Where, τ is the life time of the carriers for the intrinsic semiconductor.

3. Computational techniques

In order to analyze the performance of SOI MOSFET photodetector, the basic 3D Poisson's equation (1) is solved using Liebmann's iteration method to determine the surface potential for fixed value of gate voltage and assumed value of the drain voltage. The numerically estimated value of the surface potential is utilized to determine the charge per unit area in the inversion region. The drain current has been calculated from equation (18). The voltage profile and the electric field distribution in the channel have been estimated for accurate calculation of the drain to source current. The voltage profile in the channel is obtained by calculating the differential change in the voltage across the channel and is assumed to be very small (1mV) at the source end and low field mobility has been used to begin the numerical computation from the source end. The field dependant mobility has been computed by estimating the electric field at any point (x, y, z). The field in the channel has been calculated by numerical simulation. By calculating the electric field profile and potential field we can find out the drain to source current.

Algorithm:

Step 1. Assign gate length, channel length, device width and gate oxide thickness of SOI MOSFET.

Step 2: Divide the x, y and z axes into 20 grids each.

Step 2. Apply suitable bias voltages.

Step 3. Determine numerically the surface potential by solving the 3D Poisson's equation using Leibmann's iteration method .

Step 4: Obtain the electric field and mobility profiles.

Step 5: Also obtain the transfer characteristics, drain characteristics and compute transconductance.

3.1 Potential profile

The voltage profile in the channel is obtained by dividing the channel region into several meshes and then calculating the differential change in voltage across the channel. The numerically estimated surface potential value is used to determine the electric field and mobility profile.

$$\psi(x,y,z)=\psi(x-1,y,z)+\psi(x+1,y,z)+\psi(x,y-1,z)+\psi(x,y+1,z)+\psi(x,y,z-1)+\psi(x,y,z+1)-\left(\left(q\left(N_a+\Delta n\right)/\varepsilon_{si}\right)/6\right) \quad (11)$$

3.2 Electric field

From the potential values obtained from the numerical solution we can find out the electric field. The electric field equations in x, y and z directions are given by,

$$E_x=\frac{\psi(i+1,j,l)-\psi(i-1,j,l)}{\frac{2L}{m_x}} \quad (12)$$

$$E_y=\frac{\psi(i,j+1,l)-\psi(i,j-1,l)}{\frac{2W}{m_y}} \quad (13)$$

$$E_z=\frac{\psi(i,j,l+1)-\psi(i,j,l-1)}{\frac{2t_s}{m_z}} \quad (14)$$

where m_x, m_y and m_z are the separation of grid line along x, y, z directions, $\psi(i,j,l)$ is the surface potential, L, W, t_s are the gate length, device width & oxide thickness respectively.

3.3 Field dependant mobility of charge carriers

Now we can find out the mobility of charge carriers from the electric field values. The mobility in x, y, z directions is given by,

$$\mu_x=E_x\varepsilon_{si}\varepsilon_{ox} \quad (15)$$

$$\mu_y=E_y\varepsilon_{si}\varepsilon_{ox} \quad (16)$$

$$\mu_z=E_z\varepsilon_{si}\,\varepsilon_{ox} \quad (17)$$

3.4 Drain to source current i_{ds}

The drain current is dependant on the electric field and potential profile. The drain – source current I_{ds} can be obtained from the continuity equation. I_{ds} is obtained as,

$$I_{ds}=\frac{\varepsilon_{ox}}{d_{ox}}Z\mu_x\left(V_{gs}-V_{th}-V(x)\right)E_x \quad (18)$$

where ε_{ox} & d_{ox} are the permittivity & thickness of oxide layer respectively, μ_{ox} & E_x represents the mobility & electric field along the length of channel. V_{gs} denotes gate to source voltage, V_{th} represents threshold voltage and V_x is the surface potential.

3.5 Transconductance

Transconductance, G_m, is a measure of the sensitivity of drain current to changes in gate-source bias. Transconductance is influenced by gate width, which increases in proportion to the active area as cell density increases. Channel length also affects trans-conductance. Transconductance is inversely proportional to applied gate voltage, thus as input voltage increased trans-conductance will get reduced. The trans-conductance is defined as,

$$G_m=I_{ds}/V_{gs} \quad (19)$$

where I_{ds} is drain to source current and V_{gs} is gate to source voltage

4. Results and discussion

Computations have been carried out for the SOI MOSFET under dark and illuminated conditions to check its use as a high speed photodetector. The device parameters used for the modeling and numerical simulation are given in the table below.

Table 1. Parameters & values used in modeling.

Parameters	Value
Gate Length L	100nm
Device Width W	80nm
Oxide Layer Thickness t_s	30nm
Intrinsic carrier concentration,n_i	$1.2*10^{13}/m^3$
Acceptor concentration,N_A	$10^{21}/m^3$
Front gate oxide thickness t_{oxf}	3nm
Back gate oxide thickness t_{oxb}	400nm
Side wall oxide thickness t_{oxw}	15nm
Absorption coefficient a	$10^6/m$
Critical field E_c	$1.65*10^6$ V/m
Low field mobility μ_0	$0.2m^2/V$

Calculations have been carried out for a fully depleted small geometry SOI MOSFET. The effects of surface states on the electrical and optical characteristics of the device have also been considered. The thickness of the

oxide layer has been assumed to be 30nm and doping concentration of semiconductor has been taken to be $10^{23}/cm^3$. The optical absorption coefficient has been assumed to be $10^6/m$ at operating wavelength 1μm. The minority carrier life time has been taken to be 0.5μs.The trap density has been assumed to be distributed uniformly in the forbidden energy gap.

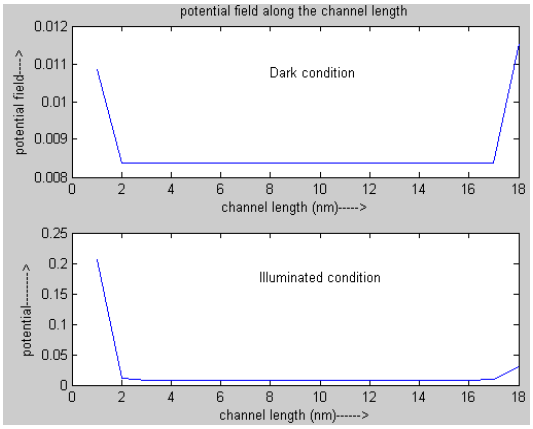

Fig.2 Potential distribution along channel length for both dark & illuminated condition.

Fig. 2 shows a two dimensional view of the potential distribution along the length of the channel under dark and illuminated conditions. It is found that the surface potential decreases linearly near the source end and increases linearly near drain end. .This is due the fact that the high electric field near the drain causes the conductivity rapidly. Due to this it is expected that the electric field near the drain end reaches the critical field for high drain voltage and hence causes the velocity saturation.

It is observed that the illuminated potential is slightly higher than that of the potential under dark condition due to the excess generated electron hole pairs.

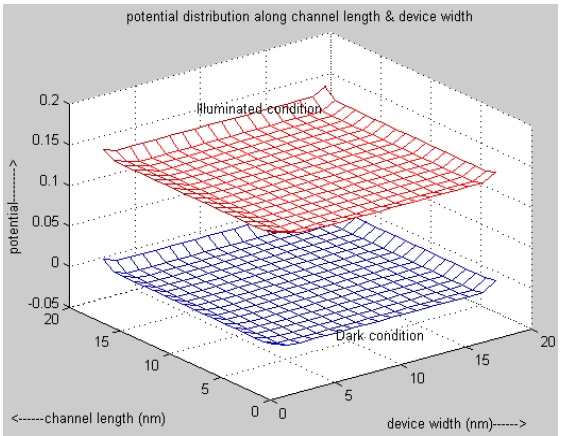

Fig.3. Potential along the length & width of the channel.

Fig. 3 shows the three dimensional view of the potential profile along the channel length and device width under both dark and illuminated conditions. The device exhibits the similar kind of characteristics along the length and width of the channel. In both the dimensions it can be seen that the potential reaches abruptly higher near the drain end due to the high electric field near the drain end which causes a rapid conduction. The effect of potential under illuminated condition is also observed.

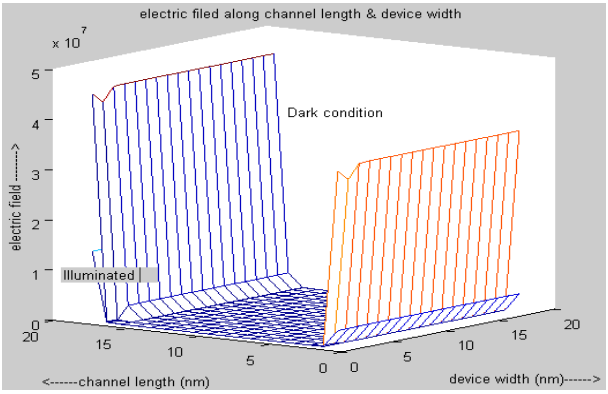

Fig. 4 Electric field along the length & width of the channel.

Fig. 4 shows the distribution of electric field along the channel length and width under dark and illuminated conditions. It is seen that the electric field along the length of the channel (E_x) is more dominant than electric field along the width of the device (E_y). The electric field increases rapidly near the drain end as seen in the Fig.4. This is due to the fact that the carrier density near the drain end experiences a rapid decrease in surface concentration which calls for a rapid increase in the electric field to maintain the constant drain current.

It is seen that the electric field near the drain end in the illuminated condition is less compared to the value of the dark. As a result a high drain voltage is needed to attain saturation in the illuminated condition. It is well known that, when an optical signal is illuminated on the device more and more electron hole pairs are generated. As the charge carriers are more crowded under illuminated condition, their mobility gets reduced in all three directions. It can be seen from equations (15), (16), (17) that the electric field is directly proportional to mobility. Therefore the field in all three directions gets reduced due to the decrease in mobility.

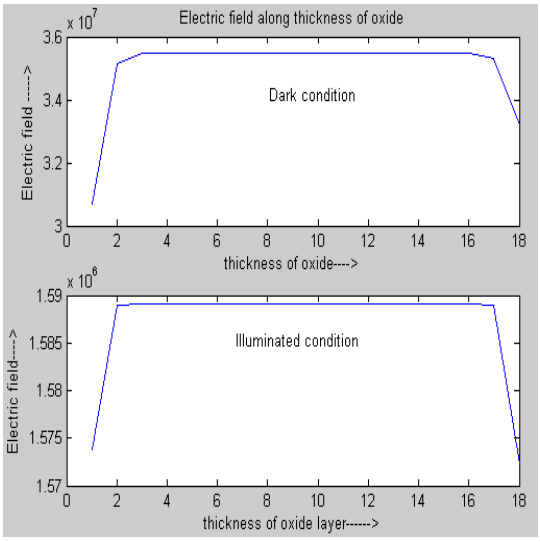

Fig. 5. Electric field distribution along oxide thickness.

Fig. 5 shows the two dimensional view of electric field along the thickness of oxide layer. It can be seen that E_z rapidly decreases near the drain end as opposite to that of E_x. this is due to the fact that as V_{gs} is applied, the electron acquires more energy to move along the length of the channel i.e., in x direction than along the other two directions. The electric field in y direction and z direction will follow the same characteristics.

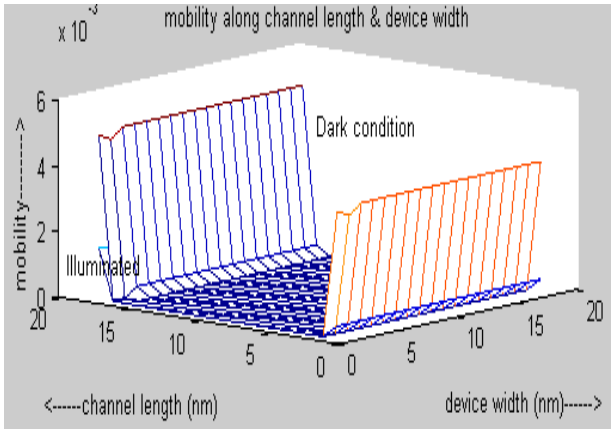

Fig. 6. Mobility profile along channel length & device width.

Fig. 6 and Fig. 7 show the distributions of mobility in all the three directions for both dark and illuminated conditions. As mobility is directly proportional to electric field ($\mu=\varepsilon E$), the shape of the mobility curves under x, y and z directions are similar to that of E_x, E_y and E_z. So the shape of the mobility curve along the channel length and device width is same as that of the electric field curve along channel length and device width. The mobility has a drastic increase near the drain end. In the illuminated case the mobility gets reduced due to decrease in electric field.

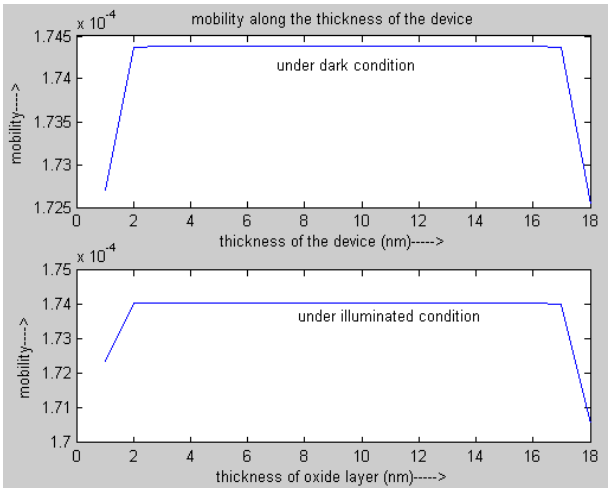

Fig. 7. Mobility distribution along oxide thickness under both dark & illuminated condition.

It is seen that the mobility gets reduced under illuminated condition in comparison with the mobility under dark condition. As more charge carriers are generated under illuminated condition, their mobility gets affected as there is not much free space for their movement. The value of mobility (velocity per unit electric field) is influenced by several factors. The mechanisms of conduction through the valence and conduction bands are different, and so the mobility associated with electrons and holes are different. The value for electrons is more than twice that for holes at low values of doping. As the density of dopants increases, more scattering occurs during conduction. Mobility therefore decreases as doping increases. At low temperatures, electrons and holes gain more energy than the lattice with increasing T, therefore mobility increases. At high temperatures, lattice scattering dominates, and thus mobility falls.

Fig. 8 shows the comparison of drain characteristics for both dark condition and illuminated condition under constant V_{gs} =0.4V. As applied drain voltage increases, the drain current also increases for fixed gate voltage. The channel width is mainly determined by applied gate – source voltage. The charge carriers pass through the channel and thereby conduction is said to take place. When drain voltage increases further, more charge carriers try to pass through the channel due to which drain current increases. But the charge carriers can utilize only the channel width that is created earlier. That is the reason the drain current saturates after a certain limit even if drain voltage is increased further. In the illuminated condition, we know that the potential get increased as compared with dark condition. Due to this fact the drain current is also get increased.

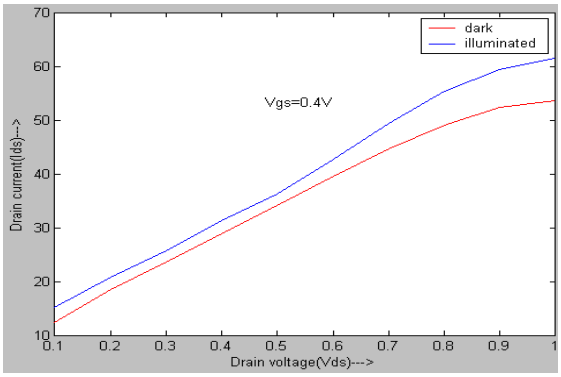

Fig. 8. Drain characteristics under dark & illuminated condition.

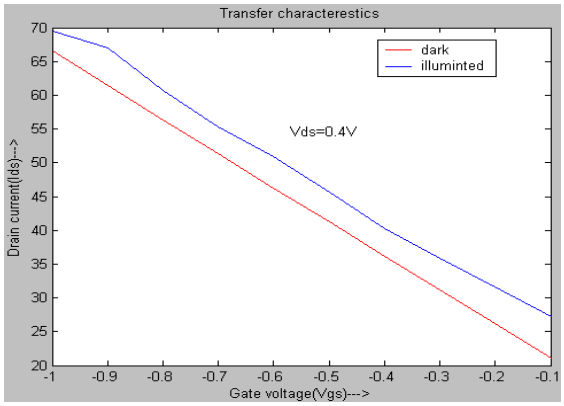

Fig. 9. Transfer characteristics under dark & illuminated condition.

Fig. 9 shows the comparison of transfer characteristics for both dark and illuminated condition under constant gate voltage (V_{ds}=0.4V). As the applied gate to source voltage increases, the drain current also increases for fixed drain voltage. This is due to the fact that the excess carriers are generated in the channel. When the drain voltage increases, the drain current also increases rapidly.

Comparison of the Trans-conductance Vs a gate voltage characteristic is also obtained and is shown in Fig. 10.

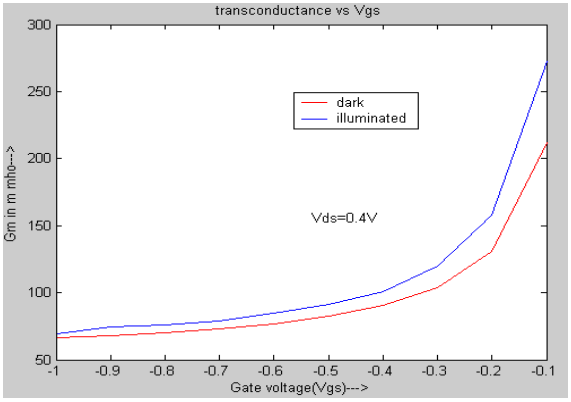

Fig. 10. Trans conductance Vs gate voltage characteristics.

Transconductance, G_m, is a measure of the sensitivity of drain current to changes in gate-source bias. The trans-conductance is defined as $G_m=I_{ds}/V_{gs}$. This parameter is normally quoted for a V_{gs} that gives a drain current equal to about one half of the maximum current rating value and for a V_{ds} that ensures operation in the constant current region. Transconductance is influenced by gate width, which increases in proportion to the active area as cell density increases. Channel length also affects trans-conductance. Transconductance is inversely proportional to applied gate voltage, thus as input voltage increased trans-conductance will get reduced.

5. Conclusion

Photoresponse characteristics of a three dimensional numerical model of nano SOI MOSFET photodetector was presented for suitability in the OEIC receiver application. The effect of various internal device parameters such as electric filed, mobility of the carriers in the presence of illumination, potential distribution of the carriers have also been studied extensively through numerical simulation. The drain current and transfer characteristics of the nano MISFET photodetector have also been calculated numerically. Transconductance of the 3D photo SOI MOSFET has also been determined.

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